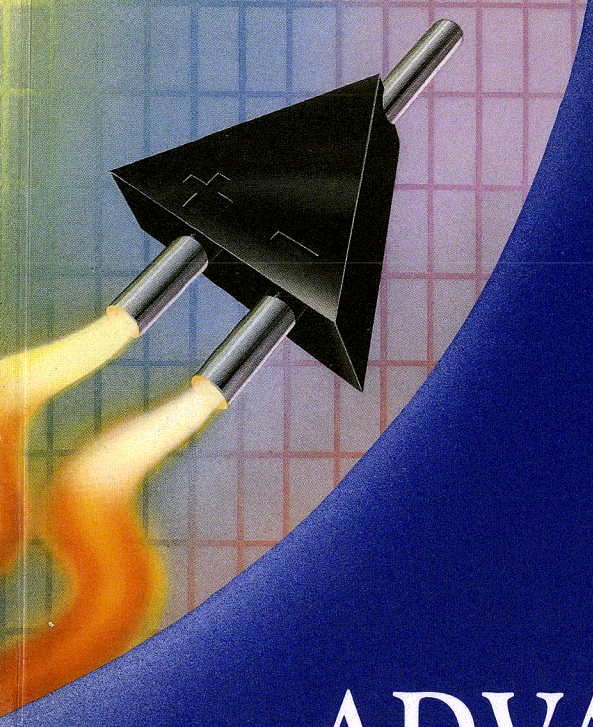

ADVANCED LINEAR

FOR PRECISION DESIGNS OF THE 90's

TEXAS INSTRUMENTS

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TEXAS INSTRUMENTS

ADVANCED LINEAR PRODUCTS
1991 DESIGN SEMINAR

Written by members of the Technical Staff, Linear Products Division
Texas Instruments

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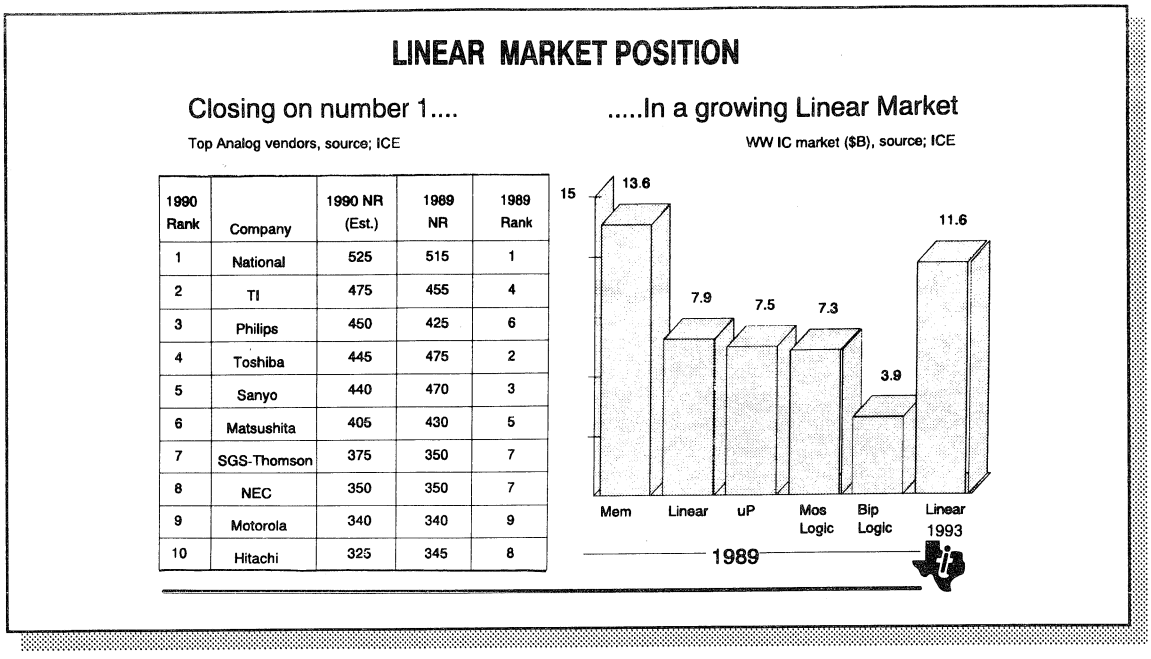
CONTENTS

SECTION 1. INTRODUCTION

INTRODUCTION INDEX



1990 Rank	Company	1990 NR (Est.)	1989 NR	1989 Rank
1	National	525	515	1
2	TI	475	455	4
3	Philips	450	425	6
4	Toshiba	445	475	2
5	Sanyo	440	470	3
6	Matsushita	405	430	5
7	SGS-Thomson	375	350	7
8	NEC	350	350	7
9	Motorola	340	340	9
10	Hitachi	325	345	8

Figure 1 - Linear Market Position

Before choosing your Linear system component, you should chose your Linear component vendor. Teas Instruments' credentials in this area are demonstrated by the leadership position we have achieved over the last decade.

In 1989 the worldwide market for Linear components was $8B, 2nd only to memories in significance. By 1993 this will grow to around $12B. Since the late seventies TI has been investing heavily in new products and production capacity to serve our clients in this huge marketplace. We have been steadily gaining ground, so that today we are closing on the leadership position.

This has been accomplished by the pursuit of market driven strategies, and significant investments in new product developments and capacity.

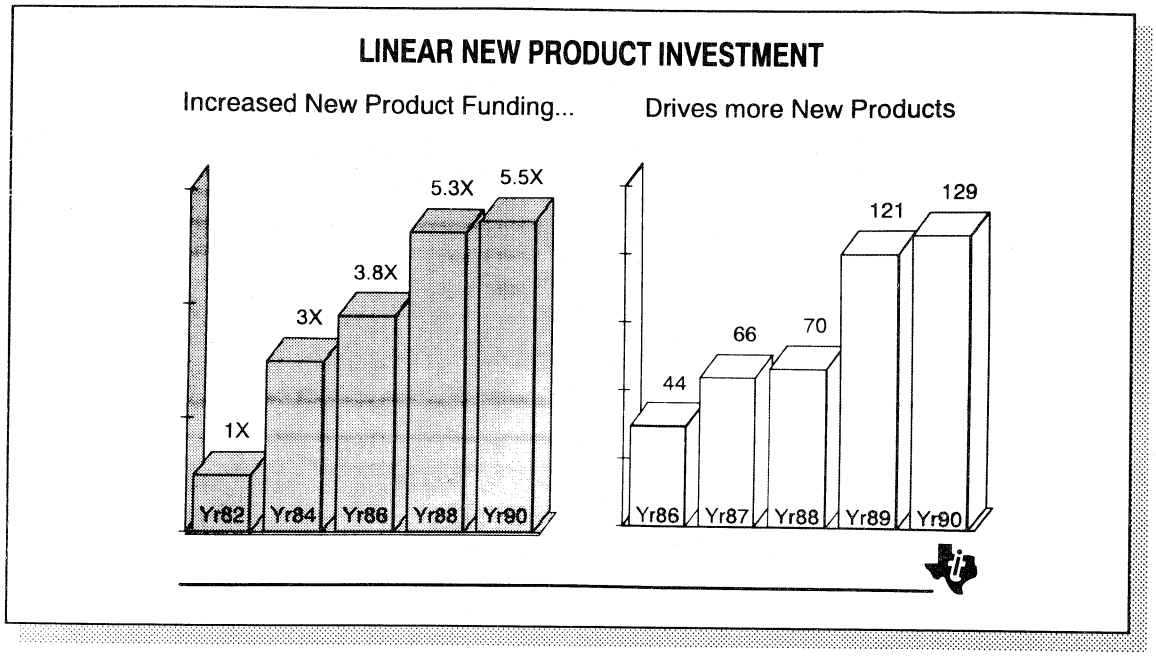


Figure 2 - Linear New Product Investment

In 1990, TI introduced 129 new Linear products. This is nearly triple the number of new products introduced in a 12 month period from that of just five years ago. This was achieved through a five-fold increase in investment in New product funding since 1982.

This results in a continuous stream of new state-of-the-art Advanced Linear products, many of which you will hear more about today.

Before getting into the main body of the seminar, to put things in a broader technology context, we will briefly discuss several key trends in technology affecting the Advanced Linear products of the future.

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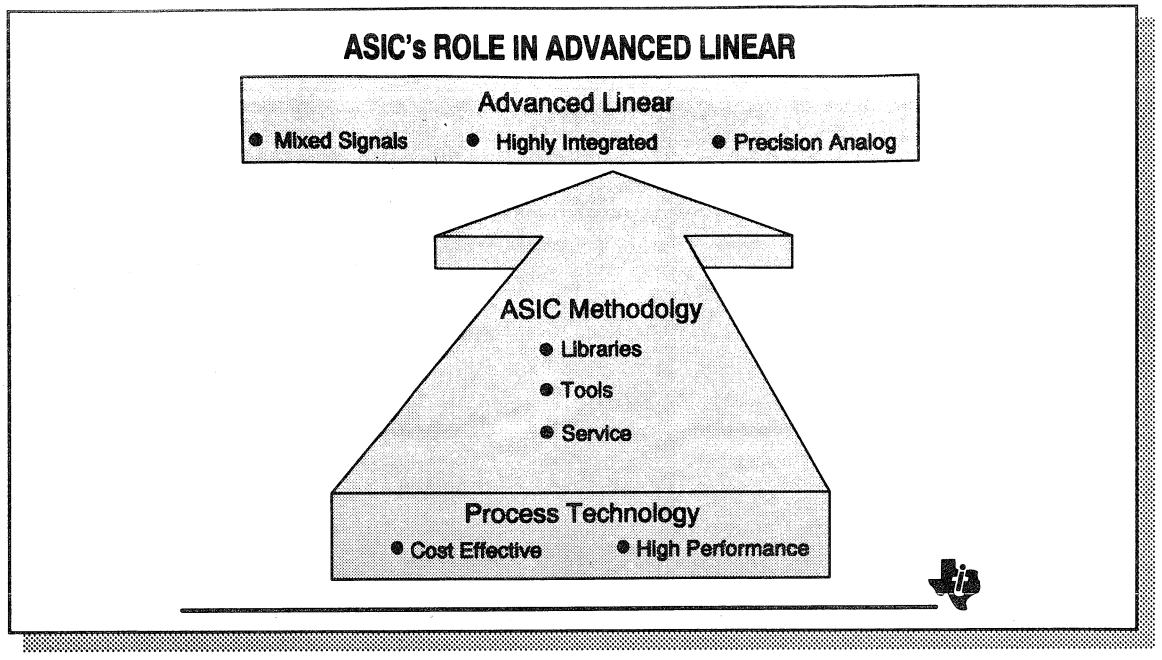

Figure 3 - ASICs Role in Advanced Linear

There are two key elements to success in Advanced linear. First - the foundation - is process technology. Onto this is built an ASIC methodology, comprising Cell Libraries, design automation and a service mentality. This methodology is increasingly important in the realisation of both catalog and custom products, with the necessary levels of integration and Analog precision.

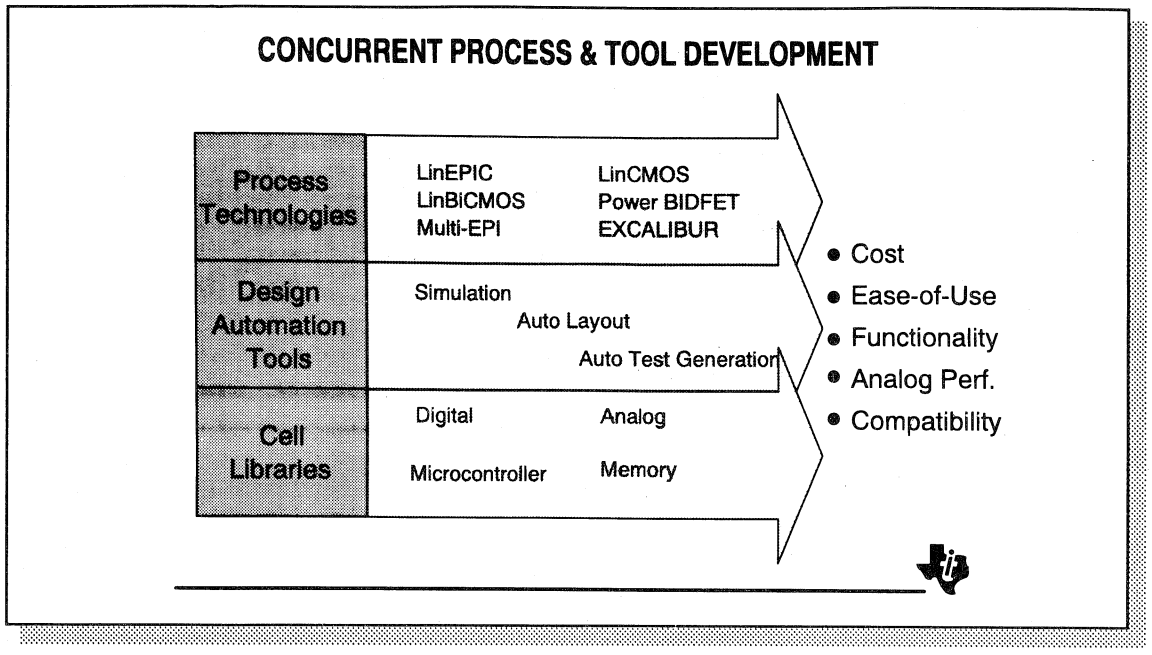

Figure 4 - Concurrent Process & Tool Development

TI has a broad range of advanced process technologies available for the implementation of Advanced Linear circuits. Examples include our 1 micron LinEPIC technology for high speed, high integration ICs with moderate precision, to LinBiCMOS(TM) which features 30V capability, compatibility with TI's 2 micron Standard Cell logic library and very low noise Bipolar analog capability. Increasingly important is the ability to integrate Power functions, and this is facilitated with TI's Multi-EPI and BidFET processes.

Leadership processes like these, however, are not enough. It is increasingly important that such processes be compatible with a broad range of Design Automation(DA) technologies as well as with each other. Processes combining the advantages of many of those mentioned are being developed at TI today for tomorrow's Mixed Signal VLSI ICs. This approach facilitates the re-use of previously developed cells in the implementation of VLSI ICs. The key point here is that, in the future, Process and DA tool development will increasingly occur concurrently, to enable next generation mixed signal VLSI implementations.

There are three key trends underway in the system design which are driving this requirement; Trends in device complexity, trends in device integration level and trends in Development cycle-time.

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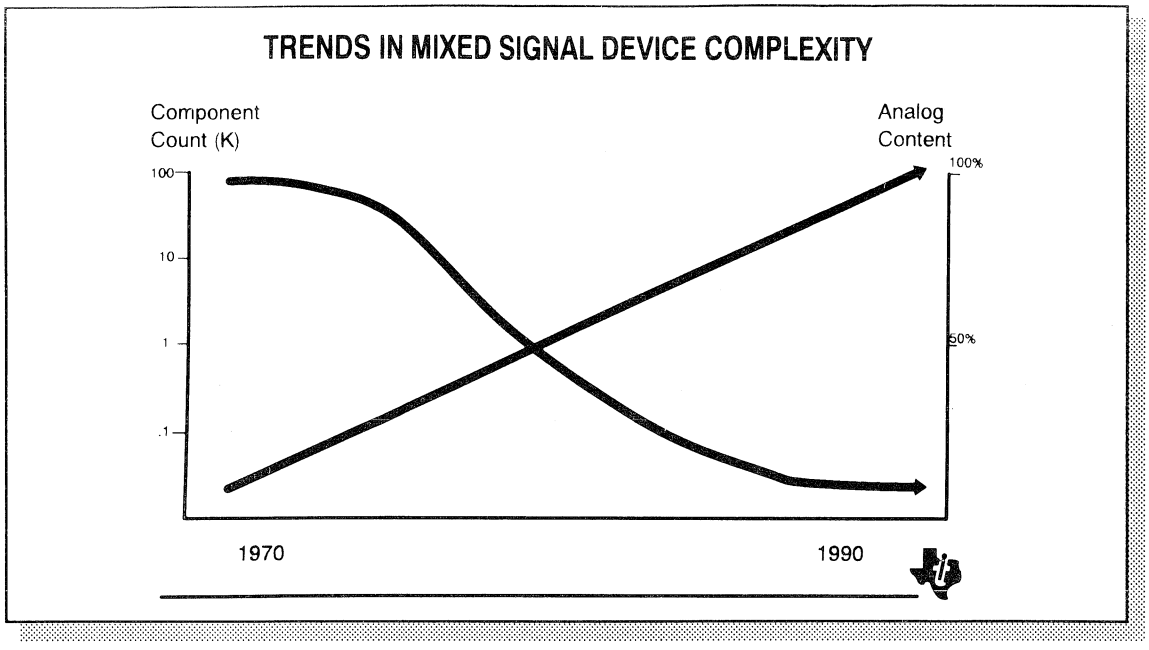

Figure 5 - Trends in Mixed Signal Device Complexity

Mixed signal device complexity has grown exponentialy for some time. Today TI is designing Advanced Linear devices containing over 100,000 circuit elements. Mirroring this trend has been an increase in the percentage of the design using digital circuitry. This is due to the incorporation of VLSI elements such as Memories, and Microcontrollers. However, it is in the analog portions of the design where the toughest design challenges remain.

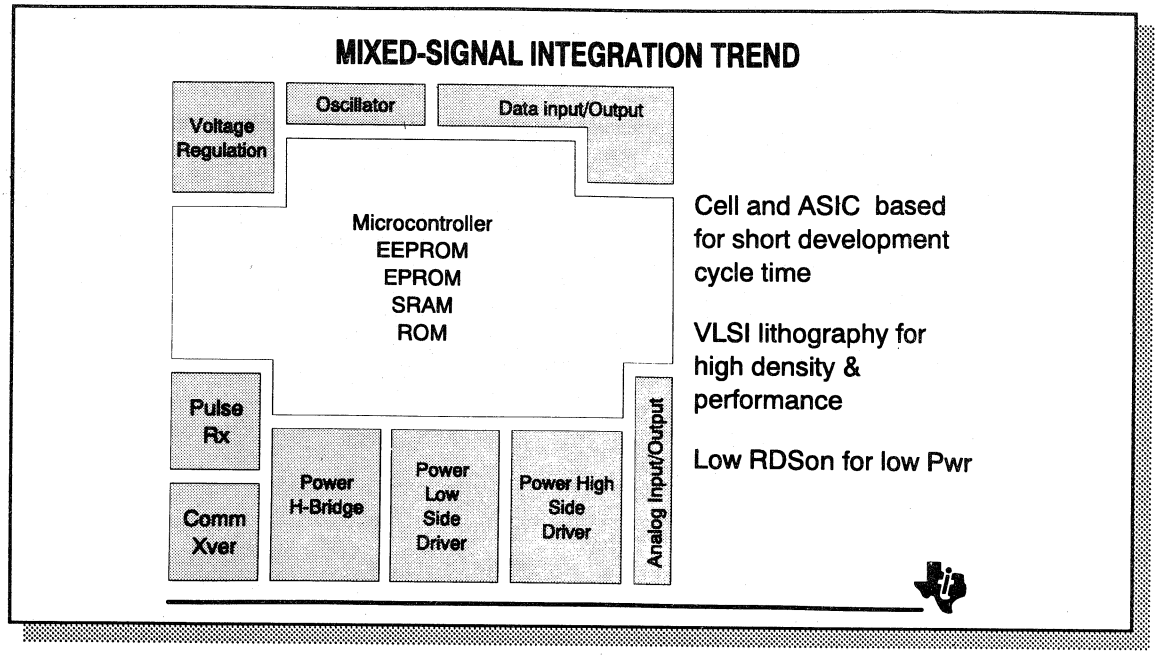

Figure 6 - Mixed Signal Integration Trend

Functionally, this device embodies many of the elements of a system. It has the usual Microcomputer and Memory elements. Much tougher, from a process and design point-of-view, is the inclusion of precision analog converters, low RDSon Power devices and high performance Data Transmission subsystems. For short development cycle-times a cell based methodology will be critical to implement these types of systems. New DA tools will be needed to combine these disparate elements, and process technologies that support both the digital, precision analog and power requirements are also necessary.

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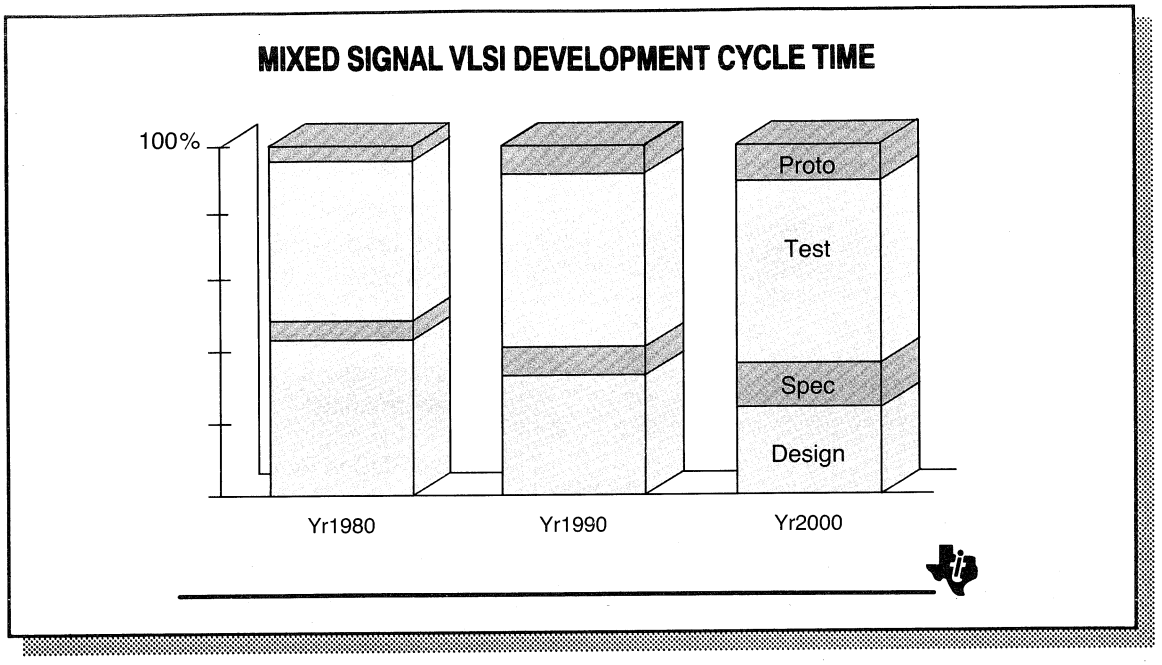

Figure 7 - Mixed Signal VLSI Development Cycle Time

The dominant contributors to overall development cycle-time of Advanced Linear catalog and custom components will remain the design task itself, and test development. TI's goal is to reduce each of these, and to structure the development process such that they can be performed increasingly in parallel.

Design Automation is the key to achieving the required improvements in development cycle time over the coming decade. There are three key trends in technology which will help us make them: Simulation, Layout and Test.

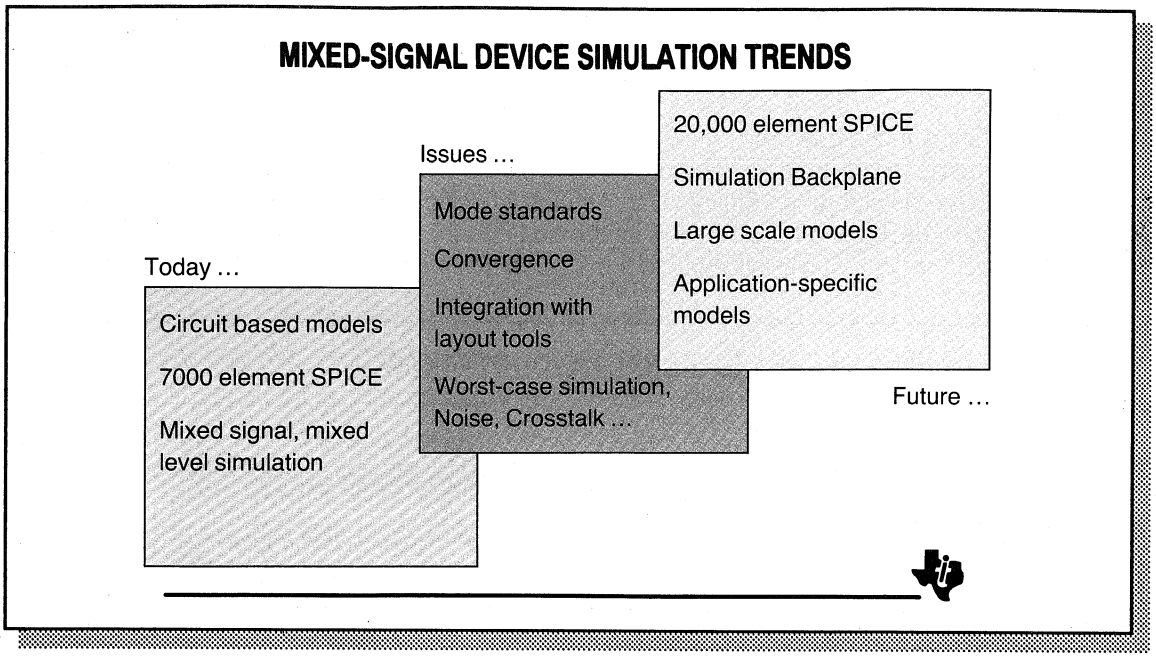

Figure 8 - Mixed-signal Device Simulation Trends

Simulation plays an important part in reducing cycle-time. Design "What-if" iterations can take place orders-of-magnitude faster in simulation than is practical with hardware bread-boarding approaches, and issues such as test are being increasingly comprehended at simulation time, further reducing development cycle-time.

As devices grow in size and complexity, so does the number of discrete simulation steps necessary to evaluate a design. Also, as performance increases, so does the requirement for simulation accuracy and resolution.

Today we consider 4-5 CPU hours a practical maximum for a simulation run. We use predominantly circuit-based models - (ie. models built up of discrete circuit elements.) These models are essentially continuous functions of simulation time. With these techniques, and a 4-5 MIP workstation we can simulate a 7000 element SPICE model.

There are several issues that must be addressed to make significant improvements. Model standards will emerge, allowing the use of the best available -and robust- model for the task at hand, instead of hastily built ad hoc models. Convergence, the satisfactory trend of multiple

Notes

SPICE iterations to close on a correct solution, will need to be addressed through better algorithms. Increasingly circuit based models will be displaced by behavioral models of entire system elements, allowing much faster simulation, of even worst case noise and cross-talk phenomena.
In the future, such techniques will allow 20,000 element SPICE simulations in our allowed 4-5 CPU hours. Large scale models, comprehending entire sub-systems, will become available... and these will be inevitably increasingly application specific. These models will require some form of simulation backplane to allow their integration into the rest of the simulation. At the same time workstation throughput will increase to the 20-50MIP range.

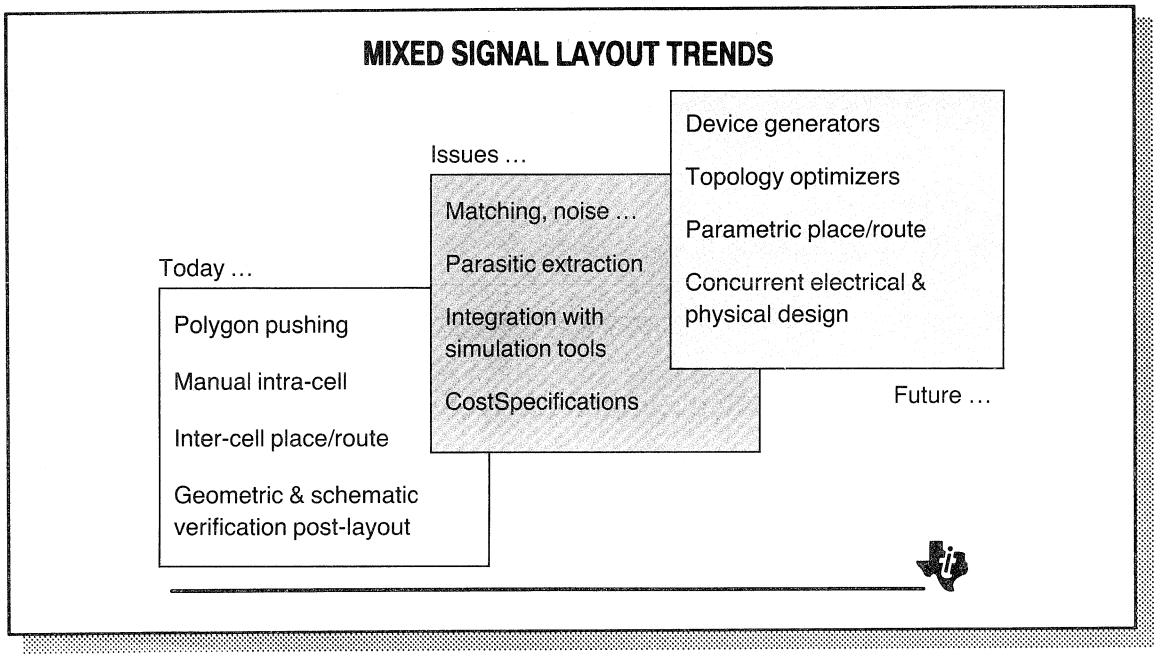

Figure 9 - Mixed Signal Layout Trends

The physical design of a mixed signal device has a disproportionately large influence on it's performance, compared with a purely digital implementation... Therefore physical layout directly impacts both the cost and performance of mixed signal systems. The complex and often subtle interaction between analog and digital functions such as noise, offset and matching are all strongly dependent on physical orientation. A transistor designed for linear operation may have completely different characteristics when laid out on a North-South axis compared with an East-West axis. Some of the key issues are; comprehending matching and noise, the ability to extract parasitic effects, and -of course- the ability to integrate Layout and layout tools.
Like Simulation, the challenges in layout are caused by simultaneous growth in integration, complexity and performance combined with the need to reduce development cycle-time.
Today the process is mainly manual. It is often refered to as "Polygon pushing" because of the manually created geometric shapes that require layout and inter-connecting. The layout in any particular cell (intra-cell layout) and between cells (inter-cell) is done by hand. Once complete, automatic software checks the resulting physical design against the Process "Design-rules" (DVER) and against the original schematic circuit (SVER).

In the future, much more of this process will be automated by increasingly sophisticated Device Generators, allowing computer synthesis of design-rule-correct cells according to pre-determined parameters. Such generators will extend to ever larger circuit elements, including recommended design practices. They will become integrated with other high-level topology optimisers and other analog circuit synthesisers.
The overall physical-electrical (Layout/simulation) design process will become much more tightly integrated, using shared databases, allowing automatic cell place-and-route software to comprehend analog idiosyncracies such as noise and matching.

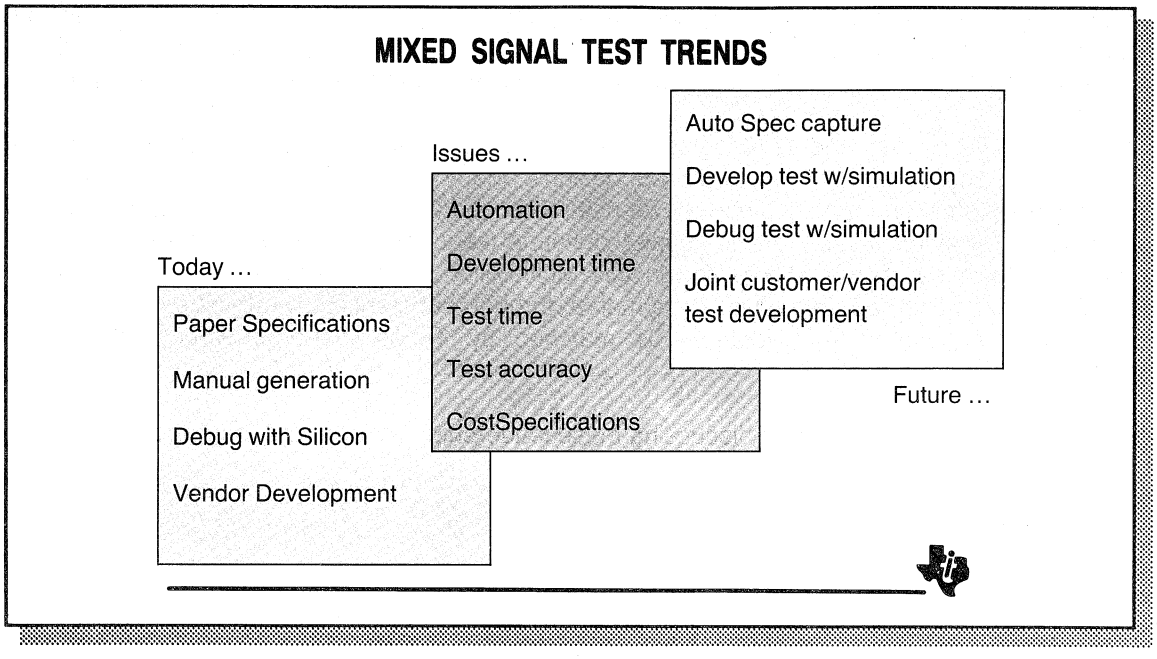

Figure 10 - Mixed signal Test Trends

We have seen that test generation is an increasing portion of the overall development cycle-time, and it has proven a particularly intractable challenge for Mixed-signal VLSI designs. Once again, the problem is compounded by the parallel trends in complexity, integration and performance. At the same time, test cost has increased markedly, driven by two factors: the need for very sophisticated - and hence expensive - testers; increased test-times to attend to the increased

Notes

complexity and precision requirements. The issues associated with improving test are the degree of automation in the test program synthesis stage, the duration of the test itself, and how we can improve device specifications to comprehend the test issue.(Design-for-test; DFT).
Today, we routinely use paper device specifications, which too frequently lack the necessary rigour or comprehensiveness to support more automated test-program generation. The test-programs are themselves generated manualy by the silicon vendor and the program is debugged with the 1st. prototype silicon.
In the future, automatic specification capture tools will be integrated into the DA environment, however, the lack of a generally available analog fault model makes this difficult. Test-program debug will start earlier in the overall development cycle, using test-vectors applied to simulation models. This will require the development of suitable analog test description languages, and the necessary translators for particular test machinery. Test is an area receiving increasing attention in TI's future.
Summarising, Texas Instruments recognises the key trends in our customers needs for Advanced Linear catalog and custom Mixed-signal VLSI designs. Many of the developments in TI's Process and Design Automation technologies that we have discused are already complete, and more are underway. Sustained investment in market driven Advanced Linear product development is allowing us to close on the #1 position in this Multi-Billion dollar market. Texas Instruments recognises the distinct requirements of this market through substantial investments in production capacity and support. This investment is matched by Texas Instruments commitment to Advanced Linear product R&D.

The balance of the seminar will be discussing these leadership products and their applications.

SECTION 2 .
SIGNAL CONDITIONING

SIGNAL CONDITIONING INDEX

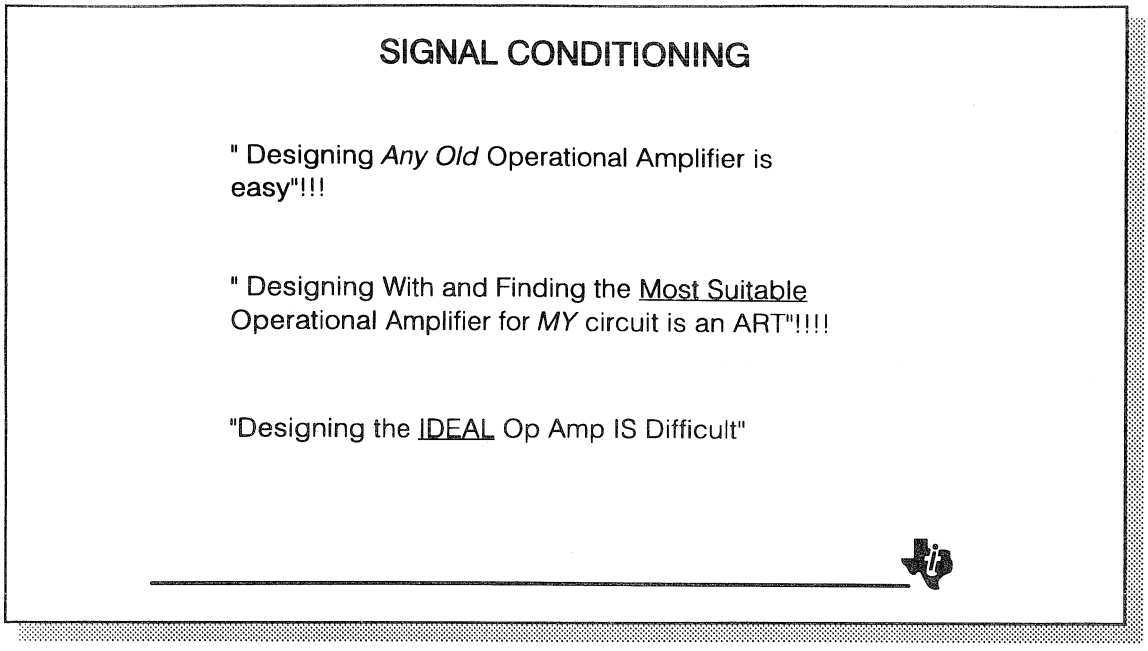

Figure 1- SIGNAL CONDITIONING

There are many thousands of different operational amplifiers in the world and probably over 50 companies manufacturing them. Like other semiconductor product families, every new device achieves higher levels of performance - offsets are lower, speed is increased, noise is reduced etc. In fact, often more emphasis is placed on *improving the performance of a device compared to the last*, without there being thought for why, where and how it will be used. TI believes it very important that new devices are designed for a reason other than they are better than the last - they must actually benefit the final application. Ensuring that each new product is suitable in the equipment for which it was designed is not an easy task.

If, when designing a new operational amplifier, the IC design engineer decided to optimise one particular parameter, say input offset voltage, then he would find it relatively easy to produce a product which was *Better than the last one*! It is likely however that the device would be of little use as a precision amplifier! By focusing on just offset voltage, other parameters important in precision circuits would be degraded. There is little point in having an op amp with 25μV offset voltage if the offset current is 1mA! Essentially therefore the total op amp needs to be considered.

Devices are increasingly being developed for specific applications and it is important that the semiconductor manufacturer understands the actual system needs and how this impacts the final op amps performance. A compromise will be necessary in order to optimise a device and all its parameters for use in a particular number of specific applications.

TI puts much effort into understanding the requirements of the market place and into developing products to satisfy these needs. Particular emphasis has been placed into understanding the requirements of both the system and the designer engineer. The aim of

this seminar is to highlight TI's new products, their key performance features and show by using applications and design theory why, where and how these devices can be used.

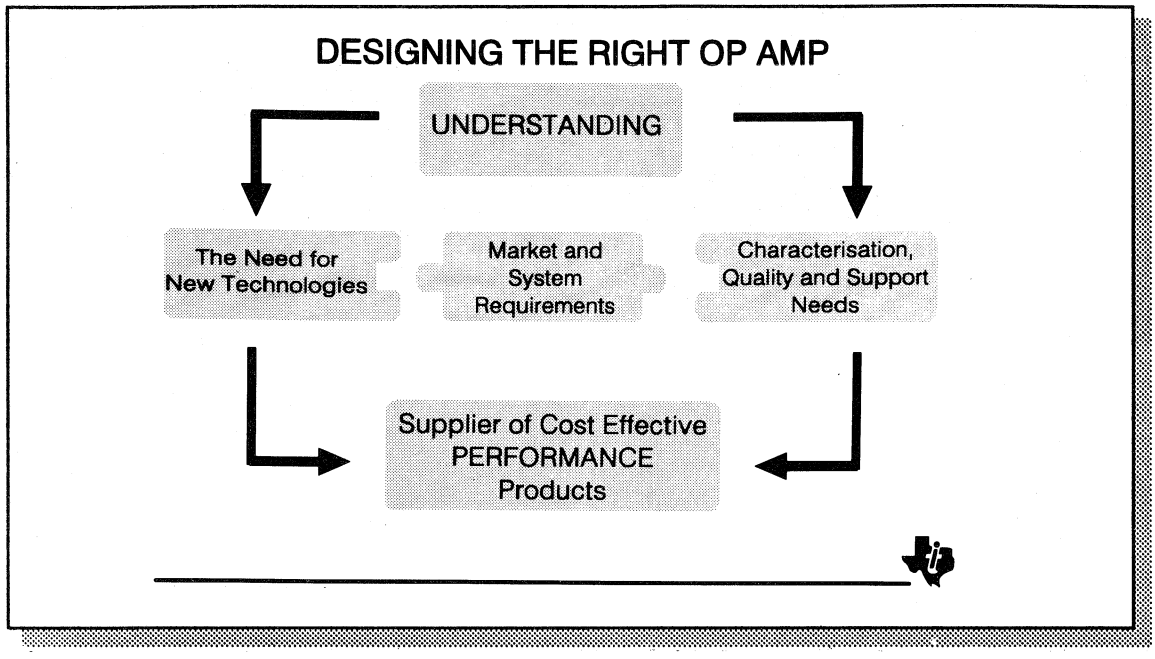

Figure 2- Designing the Right Op Amp

TI is and will continue to be a leading supplier of Cost Effective Performance operational amplifiers. To maintain this position, performance products must be developed which satisfy the demands of both the system design engineers and the end equipment. TI must therefore understand exactly what these requirements are.

To be able to provide the Right op amps for the market place, any company must have a clear understanding of 'The Total Need'. This understanding must reach beyond the 'Quest for the Ideal op amp ' - many other factors need to be considered.

TI has identified the following areas as being crucial in the development and supply of performance amplifiers;

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1) New Technologies

It is essential for design engineers to be able to use the most advanced and suitable technologies to enable the development of performance products. Skilled designers can only do so much - eventually the actual technology becomes the limiting factor. Throughout TIs history it has placed great emphasis into developing leading technologies to enable the production of performance products. Texas Instruments is the industry's leading supplier of products designed using Bifet and LinCMOS™ processes. Excalibur, TI's new complementary Bipolar/Bifet technology, has enabled the development of a number of precision, high speed, low power op amps - all of which are proving extremely popular in a wide range of different applications. The development of advanced, quality, performance technologies is one of TIs strengths and these skills are being put to good use in all areas of linear products. These technologies will be discussed in this seminar.

2) Market and System Understanding

TI focuses its products at particular applications and market segments. By understanding actual system requirements is it possible to provide devices which are highly suited to actual end equipments. TI has op amps ideally suited to applications in the following areas;- Automotive, Telecom, Instrumentation, Test and Measurement, Industrial Control, Audio and many others. By understanding the demands of these systems, an op amps parameters can be fully optimised.

3) Characterisation and Design Support Material

Having an operational amplifier which performs well is not enough - it must also be easy to use and its particular characteristics well understood. TI, like many other companies, is putting significant effort into giving excellent support and design information. Characterisation data has meant that the datasheet for a single op amp is now normally longer than 30 pages!

To ease system design and enable circuit simulation, TI has generated **Spice Macro-Models** for virtually all of its op amps and comparators.

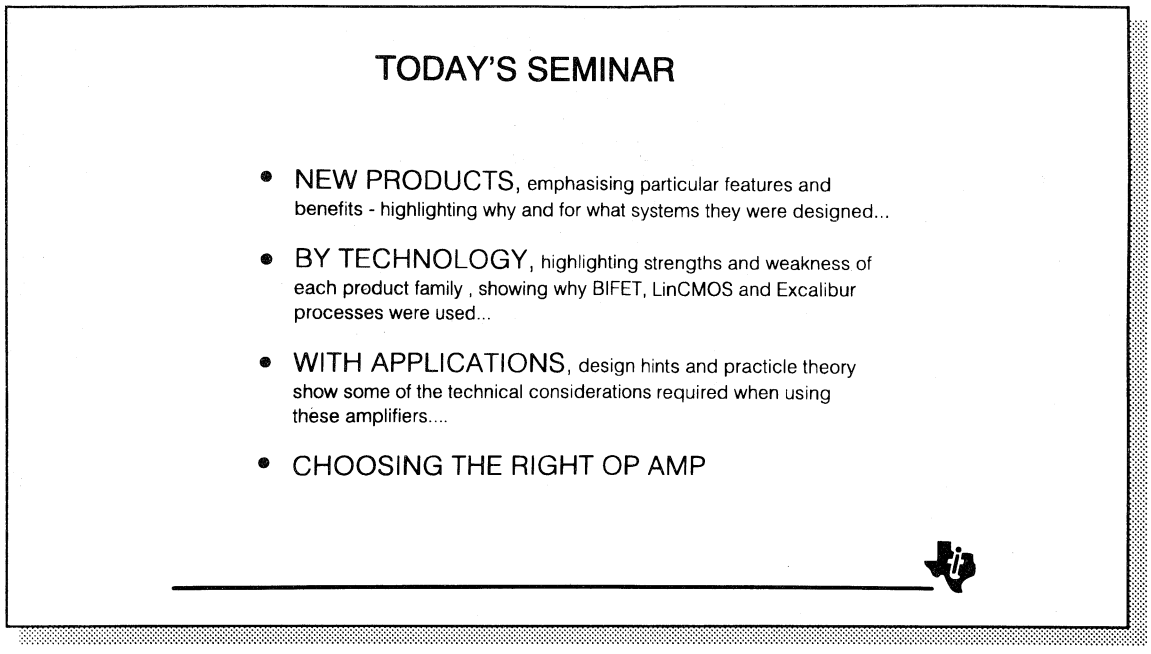

Figure 3- Todays Seminar

This seminar has two aims - to highlight New Products, and show, by using Applications and Design Considerations, where and how these op amps can be used.

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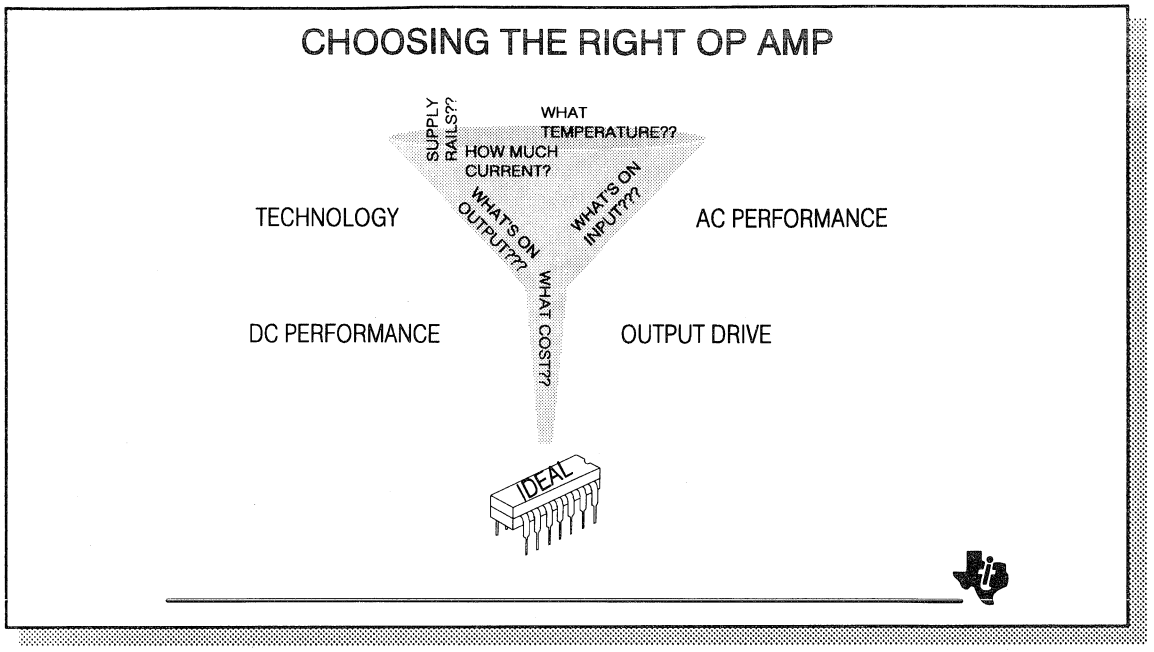

Figure 4- Choosing the Right Op Amp

A system design engineer has many constraints placed upon him(or her). Cost is an issue, but more often factors such as supply rails, noise, precision, output current etc determine what device can or can't be used in a particular application.

This seminar will try and show what limits these factors, and aims to help design engineers choose the *ideal* device for their particular application

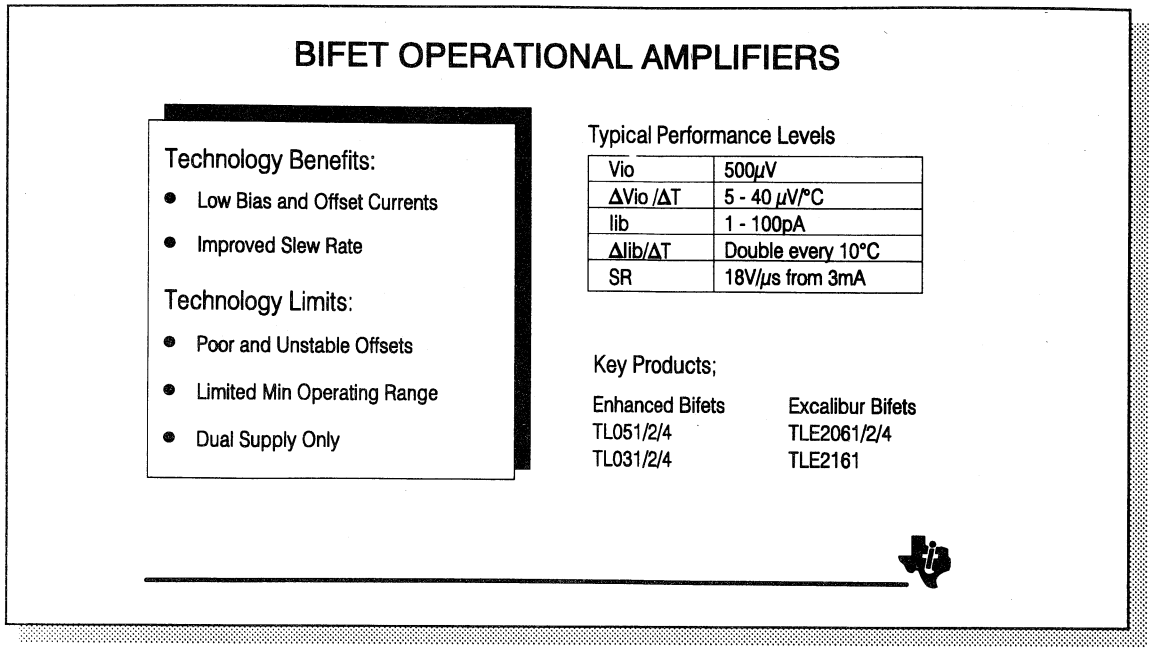

Figure 5- BIFET Operational Amplifiers

Bifet operational amplifiers were first introduced in the early 1970's and today they are among the most common op amp type. They are essentially bipolar op amps which use high voltage p-channel JFETs on the input. These JFETs have a number of advantages and disadvantages;

BIFET Advantages

High input impedance and low bias currents;
The inherent high input impedance of JFET transistors enables op amps with extremely low bias currents. This brings a number of significant advantages to many applications including integrators, sample and holds and filter type circuits. Care must be taken however as the bias currents will double for every 10°C increase in temperature. At high temperatures a Bifet's bias current may be higher than some bipolar circuits!

Notes

Improved AC performance;
When JFETs are used in an op amps input, the resulting gain of the op amps differential input stage is significantly reduced. The amplifiers internal compensation capacitor (which provides device stability) can therefore also be reduced and the result is a significant increase in slew rate. For the same supply current a Bifet op amp can easily have up to a five fold increase in slew rate over a bipolar equivalent.

Reduced Input Noise Current;
A benefit of both CMOS and Bifet operational amplifiers is their improved noise current. This is very important when interfacing to sources of a very high impedance. The input noise current is determined by the shot noise of the gate current - this is very low at 25°C.

BIFET Disadvantages

Poor and unstable offset voltages;
Bifet designs have typically far greater offset voltages than their bipolar equivalents. Their less uniform DC characteristics and poor thermal drift makes the essential accurate matching of the input transistors very difficult. They are also very prone to the induced stresses of plastic packages - real precision Bifets are normally only available in ceramic, metal can ot hybrid packages.

Typical standard selection Bifets in a plastic package may only achieve 2mV - 3mV offset voltage and their stability will be poor. Newer designs, such as the TL051 and TL031 series, discussed later, have improved processing and design techniques to achieve new levels of precision and stability.

Poorer CMRR, PSRR and Open Loop Gain specifications;
The reduced gain of the Bifets input stage which enables the improved AC performance also causes a reduction in various gain parameters of the device. This further reduces the suitability of the designs in precision applications.

Increased Noise Voltage;
A FET input stage will have a higher noise voltage and higher 1/f frequency when compared to bipolar devices.

TI's BIFETS

TL051/2/4 Family	TL071/2/4 Family	LF411/2
TL031/2/4 Family	TL061/2/4 Family	LF441/2
TLE2061/2/4 Family	TL081/2/4 Family	LF347/9
TLE2161		LF353

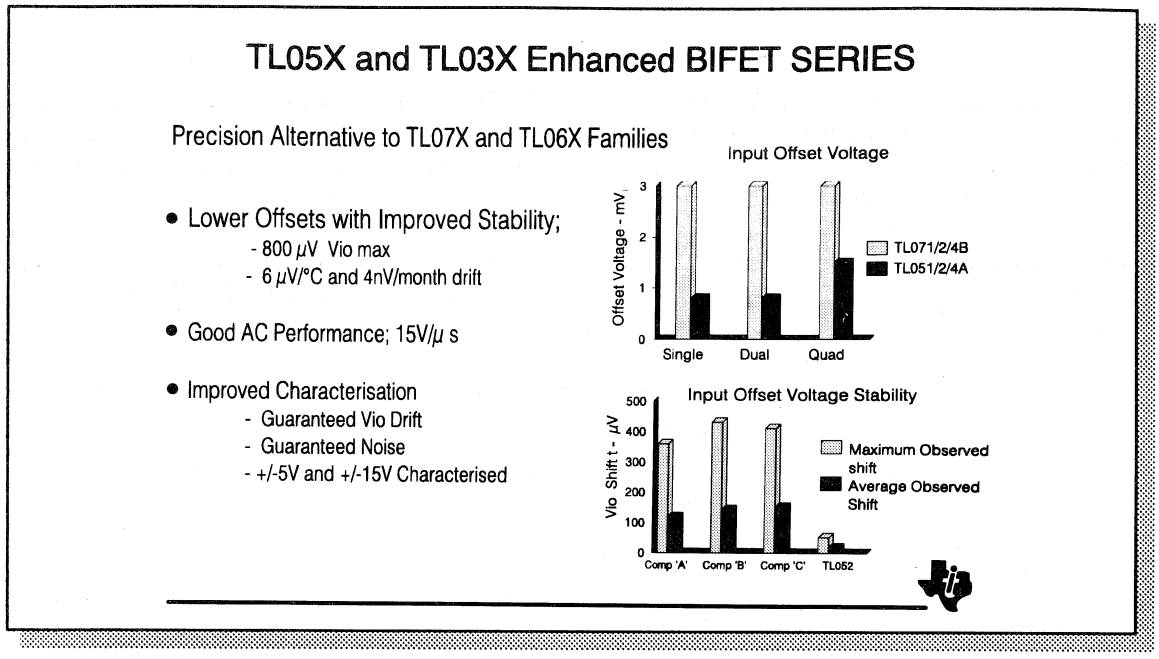

Figure 6- TL05X and TL03X Enhanced Bifet Series

Although extremely popular, one of the key factors which has restricted the use of Bifets in more applications are their relatively poor and unstable offsets. Achieving precision Bifets in plastic packages proved difficult and large yield loss meant relatively high prices. Realising this as a problem which should be addressed, TI put considerable effort into developing a new family of cost effective precise and stable Bifets. The result is the **TL051/2/4 and TL031/2/4** family of **Enhanced Bifets.**

By using new design, layout and processing techniques it was made possible to produce the level of performance as shown in the graphs above. Two selections of each device are available with the 'A' grade part achieving a maximum offset voltage of just **800μV**. The stability is also much improved and maximum values are also given.

Almost all the original products are still being used with their initial datasheets and these new designs benefit further from considerable characterisation data. The parts are fully specified at

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both +/-5V and +/-15V supply voltages with maximum values given for parameters such as noise.

Many applications are benefiting from the increased DC precision of these parts. Applications such as Audio, which were previously been seen as having purely AC demands, are using these parts extensively. More typical applications in control loop systems or filter circuits are also seeing the benefits.

Both designs are improved alternatives to the industry standard TL07X and TL06X families (TL05X is an improved version of the TL07X, TL03X is an enhancement of the TL06X), and are specified over a 'C', 'I' and 'M' temperature ranges.

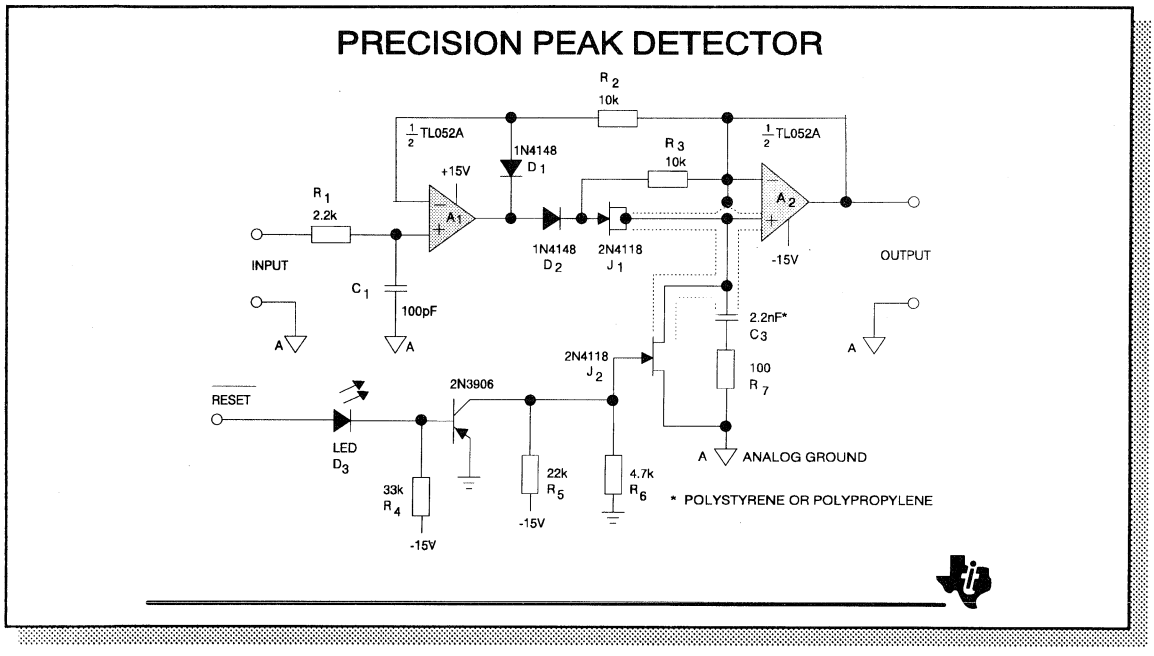


Figure 7 - Low Droop Precision Peak Detector

Basic Peak Detector

Peak detectors measure the maximum value of a fluctuating voltage. A basic peak detector consists of an ideal diode through which a capacitor is charged to a voltage equal to the peak input voltage. As long as the peak input voltage is higher than the stored voltage on the capacitor, the diode conducts and charges the capacitor. When the input voltage decreases, the diode turns off, and the maximum input peak voltage is stored on the capacitor. To measure a new and lower peak value, the peak-hold circuit must be reset by a switch discharging the capacitor. If defined slopes of the peak detector are required, a resistor in series with the capacitor limits the charge current, and a bleed resistor across the capacitor ensures a defined discharge rate.

A near ideal diode with no voltage drop is implemented using a real diode in the feedback loop of an op amp. To avoid unwanted discharge of the capacitor from loading, this is normally buffered with an op amp with low input bias current.

Improved Peak Detector

The shown low droop precision positive peak detector uses a TL052A dual JFET-input op amp to achieve very low DC errors and good holding characteristics. A bootstrapped diode circuit prolongs the holding time. The reset circuit is provided with a simple 5V logic interface. With A_1 configured as a non-inverting follower peak detector, this circuit stores the input voltage's positive peak across C_3. A_2 buffers the output. Note that leakage of the buffer op amp input, charging diode J_1, discharging switch J_2, and storage capacitor C_3, are all potential problem areas when accurate peak voltage levels have to be stored for long time periods.

Circuit Features

The actual circuit includes several features that minimize such leakage. J_1 is a low leakage 2N4118 n-channel JFET, that serves as a diode. Its small leakage is further reduced by minimizing the voltage across it; i.e. C_3 charges through D_2 and J_1, but because R_3 provides J_1 with a bootstrapped version of C_3's voltage, only D_2 sees a reverse voltage, maintaining the voltage across J_1 at the millivolt level resulting from D_2's leakage current through R_3. As the discharge switch's leakage current also represents a main leakage path for C_3 an n-channel JFET device with a low leakage off-state and low on-state impedance is selected for J_2. The storage capacitor needs to be a low leakage type with a low dielectric absorption specification to prevent recovery errors in the stored voltage. Polystyrene, polypropylene or teflon are the most suitable dielectrics for this application. The above features used to reduce the leakage of C_3 place the majority of the leakage to come from the buffer op amp's input bias current. TL052A has a max input bias current of 200pA at 25°C. For a 2.2nF capacitor, this leakage level leads to a maximum output voltage decay error given by:

$$\frac{dV}{dt} = \frac{I_{leakage}}{C_3} = 91\ \mu V / ms$$

Notes

Because of the overall feedback loop, the circuit achieves a high DC accuracy. A_2's offset and drift errors are servoed out in the peak sample period but do appear in the peak-hold mode. E.g. A_1 determines the peak output offset error in the acquisition period and A_2 in the hold mode. Consequently, DC precision op amps are required for both A_1 and A_2. As a dual op amp is more likely to have a closer offset matching, the output error due to offset shift between the peak sample and peak hold mode is reduced. TL052A has a 800μV maximum offset voltage at 25°C.

Design Details

The circuit has an inherent potential to detect unwanted transient peaks, which simply lock out subsequent desired peaks. This characteristic justifies a low-pass filter formed by R_1 and C_1 to remove fast erroneous glitches on the input. The chosen time constant, $R_1C_1 = 220ns$ should not have a major impact on the peak detector's speed. The rate of the voltage rise across C_3 is either,

1. $\frac{I_{max}}{C_3}$ (where I_{max} is A_1's short-circuit output current) or,
2. The slewing rate of A_1,

whichever is smaller. With TL052A's 50mA typical short-circuit current and C_3 = 2.2nF a maximum voltage rise of,

$$\frac{50mA}{2.2nF} = 22.7V/\mu s ;$$

can be calculated. This matches well with the op amp's specified 20.7V/μs slew rate. A high value of C_3 minimizes error due to parasitic leakage. Diode D_1 clamps the output voltage of A_1 to (V_{in} - V_{D1}) to improve speed and to limit the reverse bias voltage of D_2. If D_1 is conducting under negative input conditions, R_2 ensures that the voltage value held on the capacitor C_3 is still present on the output of the peak detector. To ensure correct and stable operation, the maximum input frequency should be much lower than,

$$\frac{1}{2\,\pi\,R_3\,C_{D2}} ;$$

where C_{D2} is the shunt capacitance of D_2. If required a capacitor can be placed across A_1 to optimize stability due to the load effect of C_3. Adjust this capacitor for minimum settling time. The circuit can be modified to capture negative peak values by reversing D_1, D_2 and substituting p-channel JFETs for J_1 and J_2. These alterations need however a modified reset circuit.

Proposed Improvements and Alterations

Replacing A_1 with a wider bandwidth TLE2141 improves speed and settling time. For low supply operation, an improved accuracy can be achieved by replacing A_1 and A_2 with the dual TLC2202 op amp offering much lower input bias current and lower offset voltage. However, speed has to be compromised.

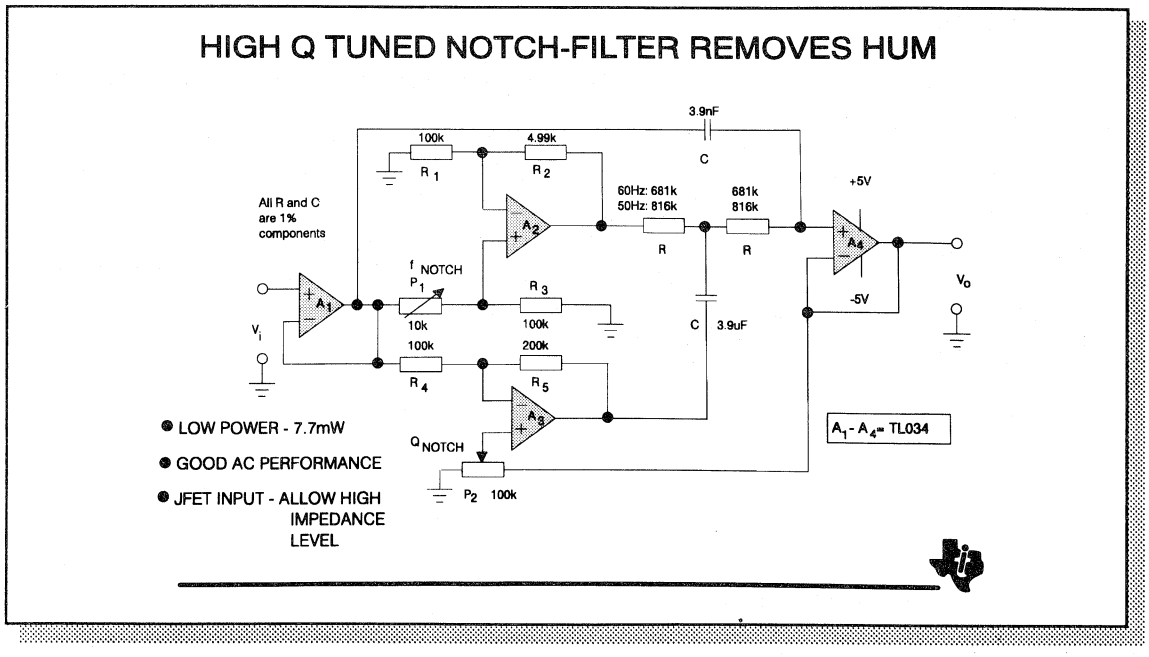


Figure 8 - High-Q Active Notch Filter Removes Hum

What is a Hum Notch Filter?

A frequent problem when measuring signals from sensors is the presence of 50Hz or 60Hz mains hum in the signal. In severe cases the interference can completely obliterate the signal of interest. When different signal conditioning amplifiers with high common mode rejection ratios fail to solve the problem or where they are not used, filter techniques are often employed.

Notes

A Notch or Band-Stop filter in the signal path - tuned to the hum frequency - effectively reduces or eliminates 50Hz or 60Hz interference. Such a filter must have a linear phase response outside the notch region to avoid distortion of the desired signal. This is particularly important where AC-signals, such as electrophysiological parameters are measured. The shown high-Q tuned active notch filter implementation uses a quad Enhanced Bifet op amp, the TL034, and has a minimum phase distortion.

Basic Hum Notch Filter

Traditional, simple band-stop filters using only a single op amp configured for a parallel-T Notch Filter have the following disadvantages:

1. Even accurate components, say 1%, still give a worst case variation in the notch frequency of a few percent. This variation from the ideal frequency, combined with a deep notch with high-Q, easily results in a filter which is not tuned for the right frequency at the deepest part of the notch. Ageing and temperature drift of filter components cause similar problems. If the notch frequency differs - say 2-3% from the theoretical value - due to component tolerances lower hum rejection can be expected. A maximum attenuation of 20-30 times compared with the desired signal can be achieved nearly independent of the chosen Q value for the notch filter.

2. Trimming of the filter's notch frequency to match the hum frequency is not a trivial task with a simple parallel-T active notch filter as the notch frequency and filter Q usually interact.

High-Q Tuned Hum Notch Filter

The shown Bridged-T active notch filter configuration overcomes problem 1. and 2. It features independent tuning of the notch frequency, f_{notch} and the notch depth Q_{notch}. Initial trimming of f_{notch} with P_1 to match the mains frequency allows the tolerance of the filter determining components to be ignored. Residual component drift will now only cause minimal shift in the filter's notch frequency. Assuming 50ppm/°C drift of R and C over a ±25°C temperature range gives a minimum 50dB (300 times) hum attenuation compared with the previous discussed 26-30dB (20-30 times) for the simple parallel-T implementation - a ten fold improvement in terms of hum rejection.

In addition, the filter configuration allows for independent Q_{notch} tuning with P_2 if required. However, a fixed Q_{notch} factor is often desired for simplicity and can be set to a maximum stable value using a fixed resistor for P_2. With the TL034 in the shown configuration a Q_{notch} factor in excess of 1000 can be realized corresponding to more than 63dB hum rejection when trimmed exactly to 50Hz or 60Hz respectively.

Why use the TL034 Bifet Op Amp?

The Enhanced Bifet TL034 used is an inexpensive op amp ideally suited for these types of applications:

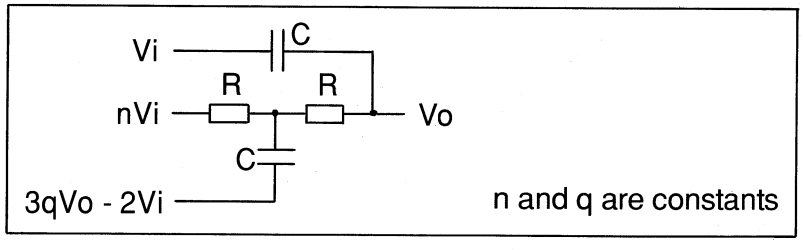
1. Low Power Consumption, 8mW typical combined with good AC-performance (2V/μs minimum slew rate and 1MHz typical unity gain bandwidth) allows use in active filters for portable equipment.

2. The JFET input stage provides low input bias current and low noise current - thereby enabling high impedance components to be used. This is especially important in low frequency active filters, such as in 50Hz and 60Hz band-stop filters as the total physical volume can be significantly reduced by employing smaller capacitor values with a corresponding high impedance and insignificant physical size.

3. Low Offset Voltage (800μV maximum @ 25°C) and stable offset voltage (5μV/°C and 0.04nV/month typically) adds little DC error to the signal of interest.

Filter Design Details

Basic RC Bridged-T Active Notch Filter:



Notes

Using superposition technique the transfer function can be derived as:

$$V_o = V_i \frac{R||(\frac{1}{Cs}) + R}{\frac{1}{Cs} + R||(\frac{1}{Cs}) + R}$$

$$+ nV_i \frac{\frac{1}{Cs}||(R + \frac{1}{Cs})}{R + \frac{1}{Cs}||(R + \frac{1}{Cs})} \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}}$$

$$+ (3qV_o - 2V_i) \frac{R||(R + \frac{1}{Cs})}{\frac{1}{Cs} + R||(R + \frac{1}{Cs})} \frac{\frac{1}{Cs}}{R + \frac{1}{Cs}};$$

$$V_o = V_i \frac{R^2C^2s^2 + n}{R^2C^2s^2 + 3(1 - q)RCs + 1};$$

$$\boxed{\frac{V_o}{V_i} = \frac{R^2C^2s^2 + n}{R^2C^2s^2 + 3(1 - q)RCs + 1};} \qquad \omega_o = \frac{1}{RC} \Rightarrow$$

$$\boxed{\frac{V_o}{V_i} = \frac{s^2 + n\,\omega_o^2}{s^2 + 3(1 - q)\,\omega_o s + \omega_o^2};}$$

In the actual notch filter shown in this application n and q are implemented as follows:

$$n = (1 + \frac{R_2}{R_1}) \frac{R_3}{P_1 + R_3}; \qquad f_{notch} = f_o \sqrt{n}; \qquad \omega_o = \frac{1}{RC} = 2\pi f_o;$$

P_1 can be used to set $0.95 < n < 1.05$ placing a variation in f_{notch} of ±2.5% relative to f_o with the shown component values.

$$q = \text{Fractional potentiometer value of } P_2 \qquad Q_{notch} = \frac{1}{3(1 - q)};$$

P_2 can be used to vary the steepness of the notch. To avoid instability when $q = 1$, a 27Ω resistor can be placed in series with P_2.

$$r = \frac{R_5}{R_4};$$

The ratio, r, is chosen to be 2 in this application. If r is exactly 2, a maximum notch depth can be obtained. A notch depth of 70dB was measured using 1% components for the actual circuit. Ultimately, the maximum notch depth is determined by the matching of the two resistors, R, the two capacitors, C, and the op amps open loop gain. If $0 < r < 2$ a pair of complex conjugated zeros appear. If desired, R_5 can be made adjustable, allowing for adjustment of the notch depth. For $r > 2$ the circuit produces sinusoidal oscillations at the frequency, f_o.

A_1 is acting as impedance converter but is really uncommitted - it can be used to provide other sensor signal conditioning functions as required.

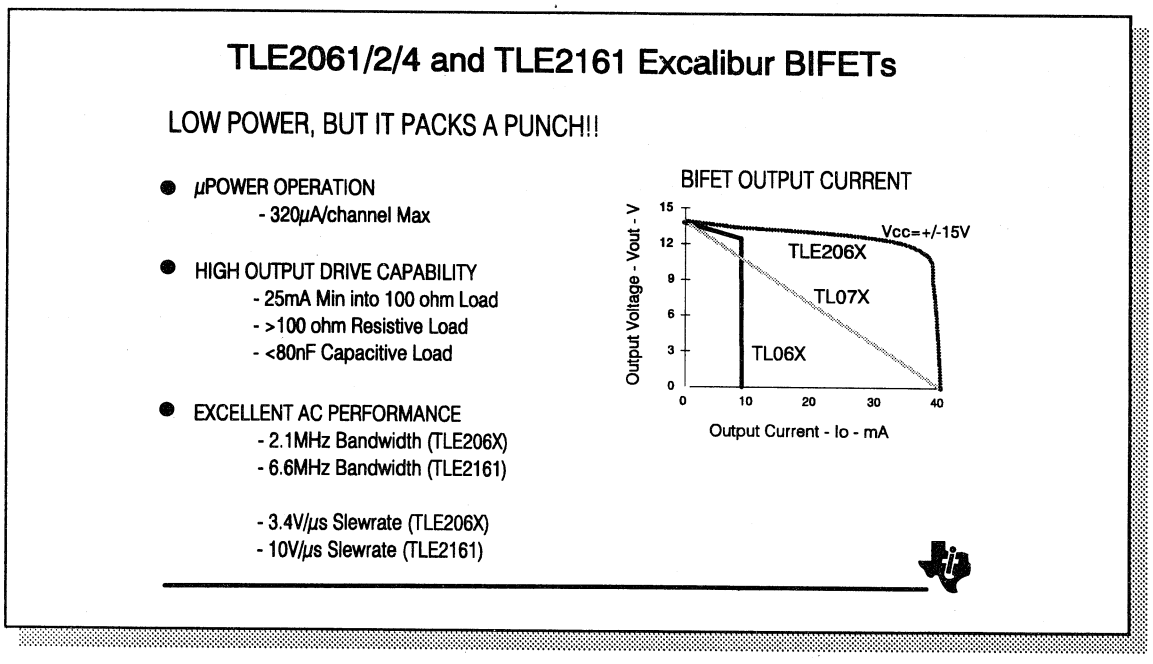


Figure 9- TLE2061/2/4 and TLE2161 Excalibur Bifets

The latest Bifets to be released by Texas Instruments are the TLE2061 family of low power, high output drive op amps. Designed using TI's new Excalibur technology (see figure 33), these devices offer a number of features not previously available from a Bifet.

Notes

The designer's task when developing these products was to produce a family of Bifets with microwatt power consumption but with the ability to drive heavy resistive and capacitive loads. The result is a part which typically consumes less than **300µA** of supply current but can also deliver in excess of **25mA of output current!** The device is guaranteed to drive 100ohm resistive loads and will remain stable when driving capacitances up to 80nF! A further feature of its excellent output performance is its relatively low distortion. Even with microampere supply currents, the **total harmonic distortion is 0.025%,** (Avd=2, f=10kHz, R_L=10kΩ).

The excellent output drive has enabled these devices to be used extensively in low power telecom circuits - the parts are particularly well suited in the 2 Wire - to - 4 Wire hybrid circuit found in line card and modem circuits which has a typical impedance of 600Ω.

DC wise the TLE2060's also perform outstandingly, the maximum offset voltage for the TLE2061B is **500µV**, with a specified Vio drift of 0.005µV/month and 6µV/°C. This is better still than the enhanced Bifets discussed previously.

Although achieving a very respectable **2.1MHz bandwidth** and a **3.4V/µs** slew rate, a decompensated version, the TLE2161 is also available to satisfy the more demanding AC requirements - this is discussed in figure 11.

Targeted initially at low power telecom equipment these versatile devices are finding applications in a number of other systems. Power supplies are making use of their high common mode input range, audio systems from its AC performance and standard low power instrumentation and filter circuits are benefiting from the combination of low offset voltages and low bias currents.

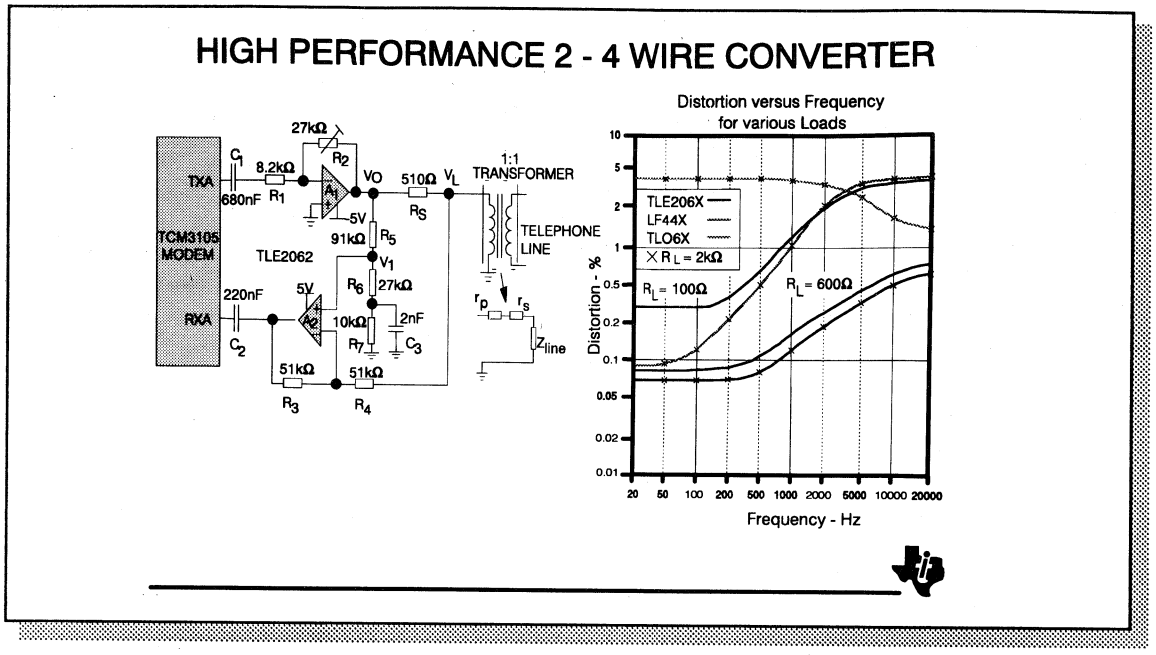


Figure 10 - High Performance 2 - 4 Wire Converter

Driving transmission lines creates extra demands on any operational amplifier. These demands are clearly shown in an application where the op amp needs to drive a 600Ω transformer coupled telephone line with the minimum of distortion.

The telephone line will be carrying information in both directions, minimising cable costs, resulting in the primary of the isolating transformer acting as both an input and an output. So when the modem is driving the line (via TXA) some of the signal will be fed back to the input of the modem, RXA, by amplifier A2. This signal is reduced by the R_5, R_6, R_7 and C_3 network: The output of A1 is fed to the non-inverting input of A2 and is subtracted from the primary voltage. Careful choice of R_5, R_6, R_7 and C_3 minimises any signal from TXA being fed to RXA.

As the system is duplex the output impedance of the TXA op amp A1 must match the line impedance, but in order to achieve low distortion the output impedance of A1 must be low.

Notes

The **TLE2062** was designed for applications requiring such a high drive capability and at the same time a low quiescent power consumption. The TLE2062 is capable of operating from ±22V down to ±3.5V, and when driving a 100Ω load from a ±5V supply has a guaranteed minimum output swing of ±2.5V . It provides this output with a very low level of distortion. As can be seen no other similar type of devices can provide either this output drive or the low level of distortion. All other devices offering similar performances require a power consuming ±12V or more supply voltage. Any distortion produced by the op amp will be sent down the telephone line via the transformer and will also be fedback to the receiver at RXA. The transformer's bandwidth limiting will help to reduce some of the distortion sent down the line, but it cannot reduce the distortion fedback to RXA. The distortion fedback to RXA can be difficult to counteract thus decreasing the quality of the telephone system.

To match the line's impedance, the TLE2062 has to have a series resistor R_S on its output. R_S will form a potential divider with the winding resistances of the transformer and the line impedance. Over the frequency range of interest, the matching transformer will add phase shift to the output V_L. So the choice of R_5, R_6, R_7 and C_3 should take this potential division and phase shifting into account. Looking from the line the impedance seen will be the winding resistances in series with R_S, and so R_S should equal the line impedance minus the winding resistances:-

$$R_S = Z_{line} - (r_p + r_s) \quad \text{.....where } r_s + r_p \text{ are the primary and secondary winding resistances of the transformer.}$$

The actual impedance of the telephone line can vary enormously from the typical 600Ω, ranging from 1200Ω down to 100Ω, so the value of R_S will change depending on the position of the 2 - 4 wire converter in the system and the length of the telephone line. In this application, assuming ideal impedance of the line, the low output impedance of the TLE2062 means that the series resistor, R_S, will need to be around 510Ω, ($r_S + r_p = 100\Omega$).

Looking at the nodes V_O, V_L, V_1 and V_S yield the following equations:

$$V_1 - V_S = [V_L - V_S]\, R_1/(R_O+R_1) \quad \text{..... Ignoring } Z_L \text{ effect on } R_O.$$

$$V_1 = V_O \times Z_1/(Z_O + Z_1)$$

$$V_L = V_O \times Z_L/(Z_S + Z_L) \quad \text{..... Where } Z_L = Z_{line} + r_S + r_p$$

R_O and R_1 are made equal to one another to maintain the received signal dynamic range. A value of 51kΩ relieves any loading by A2 and provides a lower power compromise with any thermal noise. Therefore for V_S to equal zero :-

$$\frac{Z_O}{Z_1} = 1 + 2\frac{Z_S}{Z_L}$$

As stated, the value and largely the phase of Z_L will vary with frequency due to the telephone line and the transformers' inductive natures, and so these effects should be considered. With a 600Ω telephone line Z_L = 700Ω, and so

$$\frac{Z_O}{Z_1} = 1 + 2\frac{510}{700}$$

Therefore

$$Z_O = 2.46 \times Z_1.$$

Resistors R_5, R_6 and R_7 are used to provide the matching for Z_O/Z_1, while C_3 is used to counteract the phase shift and reduce the gain at higher frequencies. Using the values of 91kΩ, 27kΩ, 10kΩ and 2nF for resistors R_5, R_6, R_7 and capacitor C_3 yields attenuations in the region of 10 to 30 dB of the frequency range of interest. Reducing the power fed back to RXA by 10 to 1000.

Notes

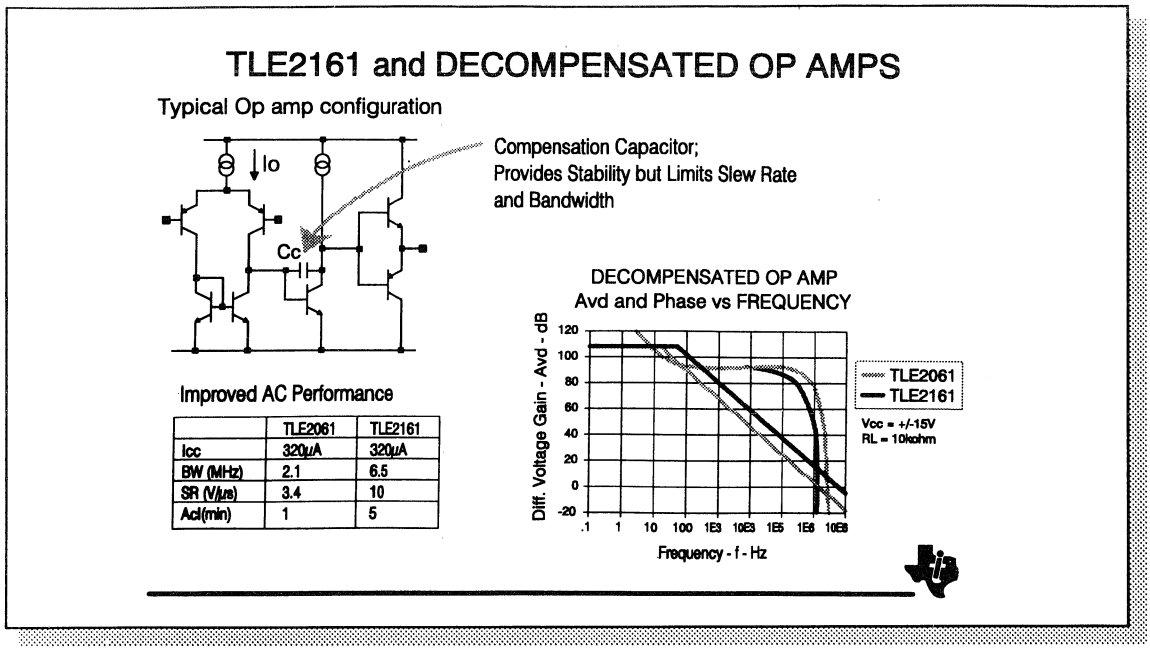


Figure 11- TLE2161 and Decompensated Op Amps

Manufacturers are continuing to release decompensated operational amplifiers, and the TLE2161, a decompensated version of the TLE2061, is the latest Bifet version from TI.

Decompensated Op Amps

The slide above shows a simplified schematic of an operational amplifier. The internal capacitor, Cc, is used to ensure that the device is stable. Its size is dependent upon the gain of the input stage and the position and number of internal poles within the amplifier. This capacitor ensures device stability and determines the slewrate and bandwidth of the op amp. Normally the capacitor is designed such that the amplifier is stable with closed loop gains down to 1. In a decompensated amplifier the size of this decompensation capacitor is reduced, the device will now no longer be unity gain stable. Instead the capacitor is chosen such that the amplifier is now stable at a different minimum closed loop gain (for most op amps this is 5).

The advantage therefore is a device which meets the same DC requirements as the compensated part but which has much improved slew rate and bandwidth performance.

The table below shows how, by decompensating the TLE2061, the TLE2161 has improved. DC performance is unchanged.

	Bandwidth	Slew Rate	Icc
TLE2061	**2.1MHz**	**3.4V/µs**	**280µA**
TLE2161	**6.5MHz**	**10V/µs**	**280µA**

* Acl(min) = 5, values are typical.

Another performance decompensated amplifier available from TI is the TLE2037, low noise precision op amp. This has a bandwidth of 80MHz, compared to 15MHz for the compensated TLE2027.

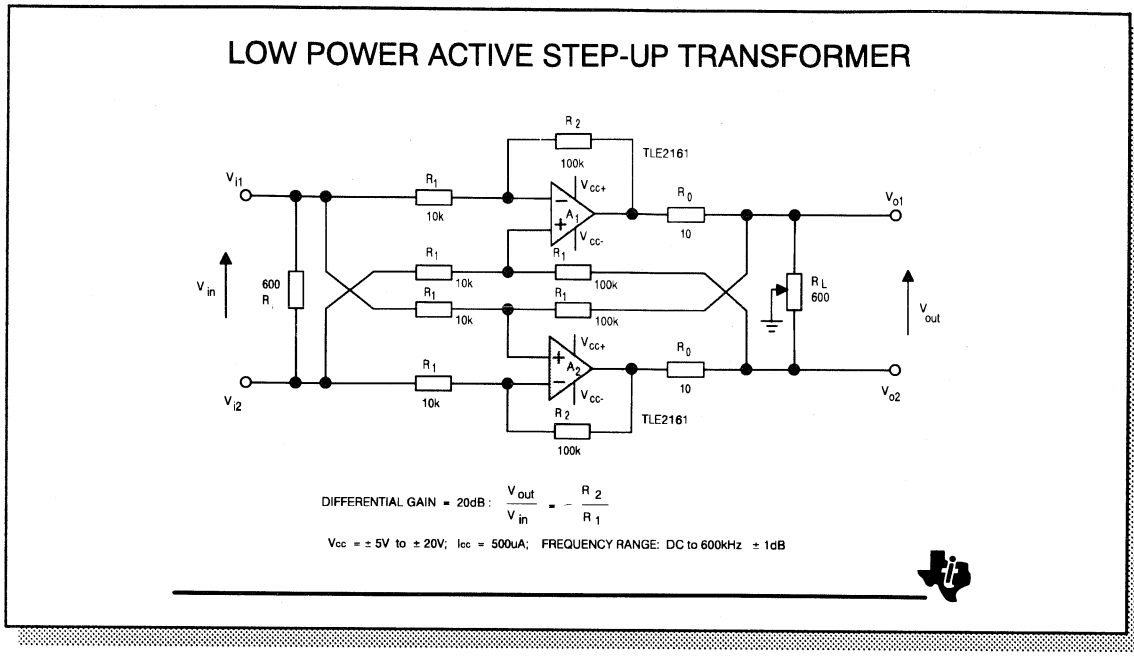


Figure 12 - Low Power Active Step-up Transformer

Transformers and Differential Transmission Lines

Small signal transformers are widely used in telecommunication equipment and professional audio applications to drive or terminate a differential or balanced transmission line with a characteristic line impedance of 600Ω. Such transmission lines provide a simple and noise immune media for transferring small AC signals in the speech or audio frequency range from microphones to amplifiers, from mixing desks to peripheral equipment or between nodes in telecommunication systems - not to mention the standard telephone line as the best known application. Common mode noise and hum signals picked up by a differential line are effectively suppressed by the common mode rejection and balance of the receiver.

Notes

Transformers have of course the advantage of high isolation combined with robustness and passive operation. Their voltage transfer ratio is typically 1:1 but in some applications a signal level step-up or an impedance conversion is required. Using a transformer rather than a standard differential line driver amplifier allows for the drive of unbalanced loads without reduction in the output swing.

Differential line driver amplifiers need high output current capability to maintain the swing under heavy load conditions but have usually superior bandwidth performance and low output impedance.

Active Step-up Transformer

A differential-input differential-output amplifier can be constructed by parallel coupling of two differential input amplifiers. However, the illustrated low power active step-up transformer is more than a standard differential-input differential-output amplifier - the circuits unique configuration is widely used in professional audio applications. The cross coupled feedback approach ensures that the output of the differential line driver looks exactly like a transformer. Either output can be shorted to ground without changing the circuit gain of 10 or 20dB. The input of the differential line driver amplifier can be set for inverting, non-inverting or single ended operation. The shown differential input configuration combined with the unique differential output approach provides an active differential-input differential-output amplifier acting in many respects exactly as a step-up transformer - hence the figure heading: Active Step-up Transformer.

The very low 500µA (typical) quiescent supply current makes this circuit especially suited for battery driven applications and portable equipment or for use in telecommunication and audio applications, where several identical circuits are used in the same equipment.

Why use the Excalibur TLE2161 Op Amp?

Similar circuits can be implemented with several different amplifiers - such as the TLE2027 and TLE2037 - both are also capable of driving low impedance loads over the speech or audio frequency range. However, the low power TLE2161 Excalibur op amp is unique in terms of power consumption. It operates in this application requiring only a quiescent supply current of 250µA (typical) each, while simultaneously being capable of driving a 100kHz $20V_{pp}$ signal into a 600Ω load!

The excellent AC performance for such a low power op amp is achieved by a JFET input stage, combined with Excalibur processing and decompensation for a minimum gain of five for stability. This combination yields a 10V/µs slew-rate and 6.5MHz gain-bandwidth product allowing operation in both the speech and audio range. In addition to the shown application, these properties are useful in low power active filter design.

TLE2161's low offset, down to 500µV max @ 25°C, does not disturb the DC balance of the line. Also, the JFET input's low input offset current adds insignificant errors to the total offset voltage even with the given high feedback impedance level.

Design Details

Ignoring the influence of R_O and R_L on the output voltage, V_{out} (assuming ideal op amps), the voltage transfer function of the circuit can be derived from:

$$V_{o1} - V_{o2} = \left[- V_{i1} \frac{R_2}{R_1} + V_{i2} \frac{R_2}{R_1 + R_2} \left(1 + \frac{R_2}{R_1} \right) + V_{o2} \frac{R_1}{R_1 + R_2} \left(1 + \frac{R_2}{R_1} \right) \right]$$

$$- \left[- V_{i2} \frac{R_2}{R_1} + V_{i1} \frac{R_2}{R_1 + R_2} \left(1 + \frac{R_1}{R_2} \right) + V_{o1} \frac{R_1}{R_1 + R_2} \left(1 + \frac{R_2}{R_1} \right) \right] ; \quad (1)$$

$$(V_{o1} - V_{o2}) = - \frac{R_2}{R_1} (V_{i1} - V_{i2}) ; \qquad <=> \qquad V_{out} = - \frac{R_2}{R_1} V_{in} ; \qquad \text{or}$$

$$\boxed{\frac{V_{out}}{V_{in}} = - \frac{R_2}{R_1}} \qquad (2)$$

If one of the differential outputs nodes - say V_{o1} is loaded heavily to ground by an unbalanced load or even shorted to ground, the opposite output amplifier, A_2 senses the decrease in V_{o1}'s output voltage and compensates by boosting its own output, V_{o2}. The sense feedback ensures that the gain remains as given by (2). The voltage at both non-inverting op amp inputs is approximately zero volt. When V_{o1} decreases, the voltage on the non-inverting input of A_2 increases, thereby raising the voltage V_{o2} to maintain the output voltage, V_{out}. Also, the voltage drop across R_O is adjusted out. Consequently, the line driver with differential input can drive unbalanced loads, exactly like a true transformer.

In order to ensure that one output can drive the total output swing, when the other is shorted, the output swing under normal balanced load conditions must be held below half the maximum swing. With an input signal, $V_{in} = 2V_{pp}$, the output swing, $V_{out} = 20V_{pp}$. This level can easily be sustained by one op amp if the other 's output is shorted to ground.

The choice of resistor impedance for R_1 and R_2 is a compromise between on one side, low power consumption for small signal levels and high input impedance, against on the other

Notes

side, significant speed requirements. If the feedback resistor, R_2, is larger than 100kΩ it may add further phase shift due to parasitic input capacitance, that could lead to instability. Additionally, the common mode rejection will be reduced as accurate matching of high impedance resistors is difficult. Good input common mode rejection requires well matched values of all R_1s and all R_2s.

The circuit operates from ±5V to ±20V supplies and the maximum output swing is of course limited by the applied supply voltage. At very high frequencies however, the slew rate limitation of the op amp influences the maximum output swing. To produce a non- slew rate limited $10V_p$ sinusoidal signal at 100kHz, $10 \times 2\pi \times 100 \times 10^3$ V/s = 6.3V/μs minimum slew rate is required. This is well below the op amp's specified minimum of 7V/μs.

Measured Performance

Measured typical performance is given in the table.

Parameter	Test Conditions	Measured Performance	Unit
Frequency Response	V_{out} = 5V_{pp}, V_{CC} = ±15V, R_L = 600Ω	0 - 600 ±1	kHz dB
Maximum Output Voltage Swing	Balanced Load, f = 20kHz,		
	R_L = 600Ω, V_{CC} = ±20V	54.6	V_{pp}
	R_L = 600Ω, V_{CC} = ±15V	42.6	V_{pp}
	R_L = 600Ω, V_{CC} = ±5V	12.8	V_{pp}
	R_L = 300Ω, V_{CC} = ±5V	11.6	V_{pp}
	R_L = 100Ω, V_{CC} = ±5V	8.0	V_{pp}
Max Common Mode Input Voltage Range	V_{CC} = ±20V	±17.9	V_{pp}
	V_{CC} = ±15V	±12.8	V_{pp}
	V_{CC} = ±5V	±3.0	V_{pp}

At low frequencies, the common mode rejection ratio of the circuit depends on resistor matching. However, at high frequencies, it is affected by the op amps own common mode rejection ratio. Using resistors with 1% tolerance, more than 50dB common mode rejection was obtained for frequencies less than 10kHz.

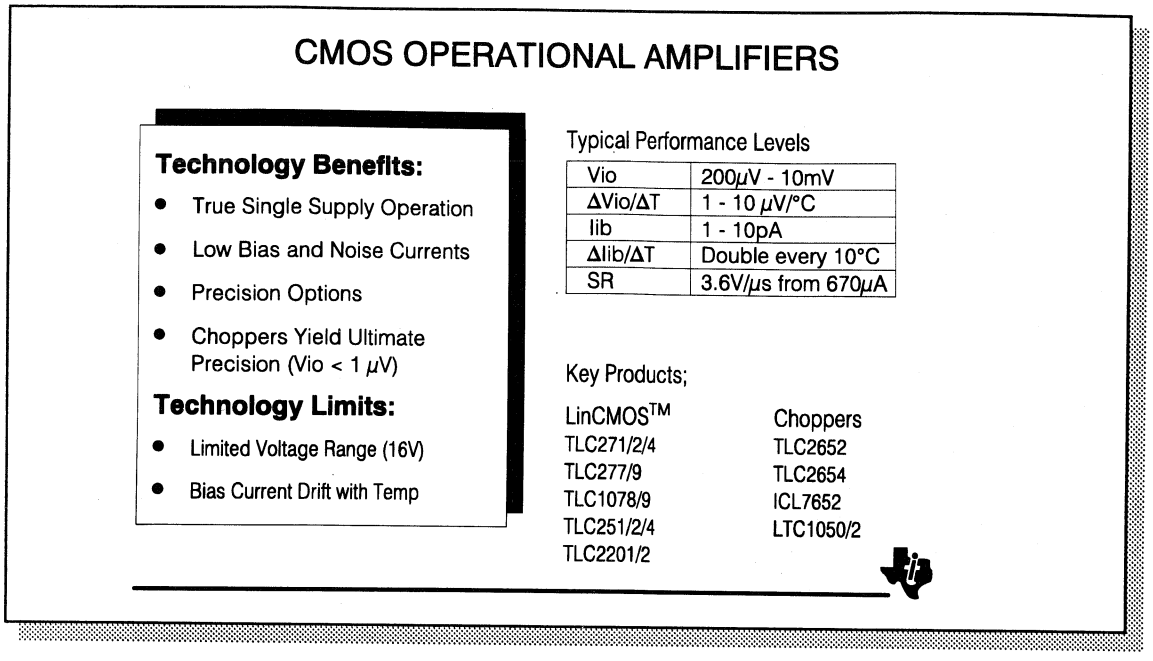


Figure 13 - CMOS Operational Amplifiers

Although originally considered to be too unstable for many linear functions, CMOS amplifiers are now well accepted as a real alternative to many bipolar, Bifet and even dielectrically isolated op amps.

Texas Instruments was the first company to release linear devices designed using the CMOS process, LinCMOS™, which was specifically developed for linear circuits. The first products were released in 1983, and LinCMOS™ and its next generations are still being used today to realise a whole range of linear functions - from op amps to A-D convertors.

LinCMOS™ will be discussed later in the seminar, but the various strengths and weaknesses of CMOS technologies are highlighted below.

Notes

CMOS Advantages

Single supply operation;
By far one of the most significant advantages of using a device designed using CMOS technology is their excellent single supply operation. By using PMOS on the input stage and an NMOS on the output stage it is possible to develop a device with an input common mode range that includes the negative rail and an output stage that swings all the way down to the negative supply - true single supply operation! This feature obviously makes the devices extremely popular in battery powered applications.

Low Voltage and low Supply current applications;
TI has low bias op amps capable of operating with supply currents of less than 10μA and at supply voltages down to 1.4V. Single supply battery powered applications benefit further by using these parts.

High input impedance and low bias currents;
Like Bifet op amps, using MOS transistors on the input stage enables op amps with high input impedance and low offset and bias currents. Bias currents can be in the fA range but difficulty in testing, and various leakage currents mean that these levels of performance are rarely specified. A typical LinCMOS^{TM} op amp has a bias current at 25°C of 100fA. Over temperature however the bias currents will double for every 10°C increase in temperature.

ESD (Electrostatic Discharge) Protection;
Something which is perceived to be a problem but with devices designed using LinCMOS^{TM} is not. All devices produced using LinCMOS^{TM} are designed to withstand 2kV ESD - something many bipolar designs cannot claim. Protection circuits found in LinCMOS^{TM} devices are discussed in figure 14.

CMOS Disadvantages

Limited Voltage range;
Although ideal for low supply voltage applications, most CMOS parts will not operate with supply voltages greater than 16 or 18 Volts. This is a limitation in some wide supply, instrumentation applications.

Limited Offset Voltages;
The best CMOS devices can achieve offset voltages as low as 200μV which is better than Bifet parts but does not compete with the best bipolar designs. Typical CMOS op amps will have an offset voltage specification of 2mV - 10mV. The stability of CMOS devices is however improved over Bifet designs.

Chopper stabilised op amps however, which are discussed in detail later, are designed using CMOS technology and achieve the ultimate in DC precision. Maximum offsets as low as 1μV are realisable.

High Noise voltage;
Like Bifets, a MOS input causes devices to suffer from a high input noise voltage and high 1/f corner frequency, their input noise current is normally extremely low. The TLC2201 however, discussed in foil 20, actually features a combination of low voltage and current noise specifications.

TI's CMOS amplifiers

TLC2201/2	ICL7652	TLC277/9	TLC271	TLC27L2/4
TLC2652/4	LTC1052	TLC27L7/9	TLC272/4	
TLC1078/9	LTC1050	TLC27M7/9	TLC27M24	

LinCMOS™ was TI's first linear CMOS technology and the resulting products are now industry standards. It has since been upgraded with **Advanced LinCMOS™** which because of smaller geometries and more compact capacitors has enabled the true interface of digital and analog structures - the most obvious result has been performance a/d convertors. **LinBiCMOS™**, is the latest revision - it features the CMOS structures as found in Advanced LinCMOS™ but also has true bipolar transistors included. This technology is being extensively used as part of TI's LinASIC™ program.

Notes

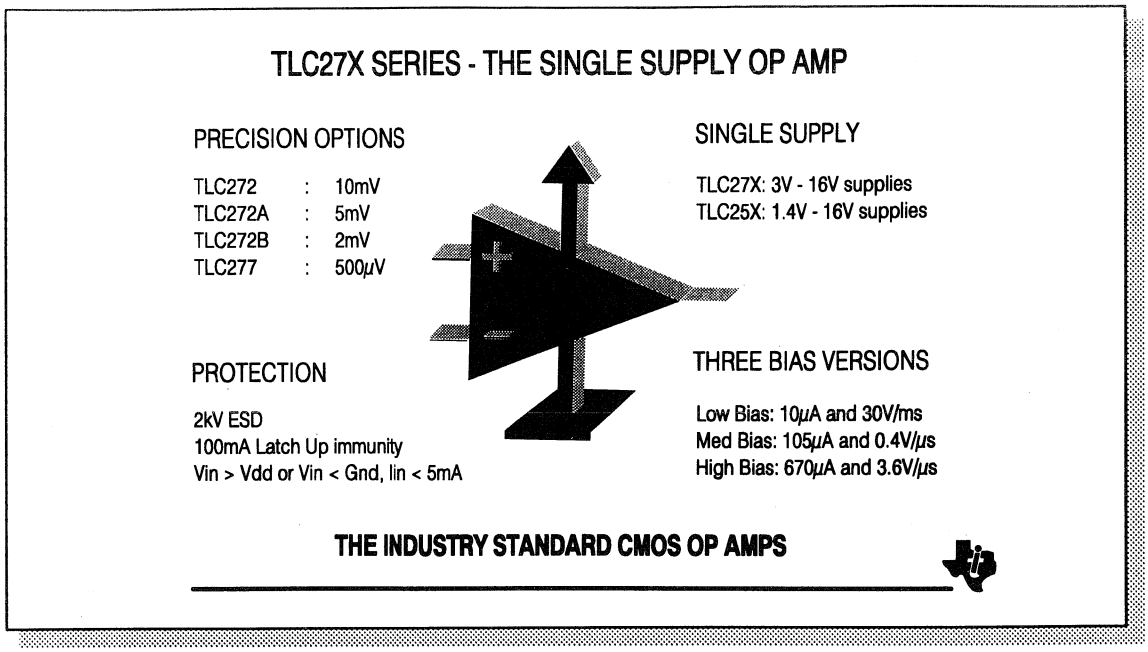


Figure 14 - TLC27X Series - The Single Supply Op Amp

The first LinCMOS™ op amps were released in 1983 and there are now a number of families to chose from. Newer designs have been optimised for precision, low noise or low power and are discussed in detail later in the seminar. This figure summarises the various features of the original designs;

If we consider the part number of a standard LinCMOS™ op amp the whole family can be easily understood. A typical part number is....**TLC27L2AID.**

'TLC2' means the device is a LinCMOS™ op amp. Parts starting TLC3... are comparators. Standard amplifiers (beginning TLC27) operate with supply rails ranging from 3 to 16 Volts. The **TLC25X** version have been designed to operate with **1.4V supplies**.

'L' refers to the Bias version. The standard family of products are available in 3 Bias versions - each determines the supply current and corresponding AC performance of the amplifier. 'L' means low bias with low supply current and low slew rates. 'M' would mean medium bias and no letter equates to high Bias (see above figure).

'2'. There are single, dual and quad versions available and this number relates to the number of channels. Care must be taken however as the **TLC277** and **TLC279** (duals and quads) are also available. These devices are precision, zener zapped versions with low offsets down to 500μV, and are also available in 3 bias options.

'A' means the device has been offset selected, with a maximum Vio of **5mV**. Standard parts are specified with **10mV** of offset and the 'B' selection has **2mV** of offset. As stated above, real precision is available from the TLC277 and TLC279.

'ID' . All CMOS op amps are available in a number of different packages (DIL, SO, Ceramic and chip carrier) and are specified over a number of temperature ranges ('C', 'I', and 'M').

Protection

ESD - Electrostatic Discharge is one of the most common causes of damage to CMOS devices. To reduce failures due to this phenomenon, each pin on Texas Instruments LinCMOS™ devices is protected by internal circuitry.

Standard ESD protection circuits safely shunt the ESD current by providing a mechanism whereby one or more transistors break down at voltages higher than the normal operating voltage but lower than the breakdown voltage of the input gate. This type of protection scheme is limited by leakage currents which flow through the shunting resistors during normal operation after an ESD voltage has occurred. Although these currents are small, in the order of tens of nanoamps, CMOS amplifiers are usually specified to draw input currents as low as tens of picoamps.

To overcome this limitation, TI design engineers developed a patented ESD protection circuit which can withstand several 2-kV ESD pulses while reducing or eliminating leakage currents that may be drawn through the input pins.

All input and output pins on LinCMOS™ and Advanced LinCMOS™ products have associated ESD protection circuitry that undergoes qualification testing to withstand 2000V discharged from a 100pF capacitor through a 1500 ohm resistor (human body model) and 200V from a 100pF capacitor with no current limiting resistor (Charge device model). These tests simulate both operator and machine handling of devices during normal test and assembly operations.

Latch Up - Latch-up occurs when an input or output voltage exceeds the supply rails, causing a parasitic SCR between the supply rails to turn on. When this occurs, the device supply current can increase from 20μA to many mA, which causes either functional or parasitic device failure. The only way to turn off this SCR is to remove the power to the device.

Voltages exceeding the supply rails can occur on I/O pins during many different stages of the manufacturing process. During board level testing (manual or bed-of-nails), stray voltages may be applied when contact is first made to the active circuit. ESD discharge from a person touching the end product may find its way to the I/O pin of the CMOS device and cause latch - up.

Notes

LinCMOS™ and Advanced LinCMOS™ products are designed to withstand - 100mA I/O currents without latch-up. During wafer probe, every I/O pin is tested to this limit at 25°C with a very short duration pulse test that limits the amount of power and prevents damage to the device under test.

An additional feature of TI's protection circuits is their ability to be able to withstand a continuous +/- 5mA current on any I/O pin. If the input current is limited to less than 5mA, then the voltage can be significantly higher than the supply voltages.

For more information about ESD, Latch-up and the various quality and test flows of LinCMOS™ and Advanced LinCMOS™ devices, please refer to the **LinCMOS™ Technology Highlights brochure.**

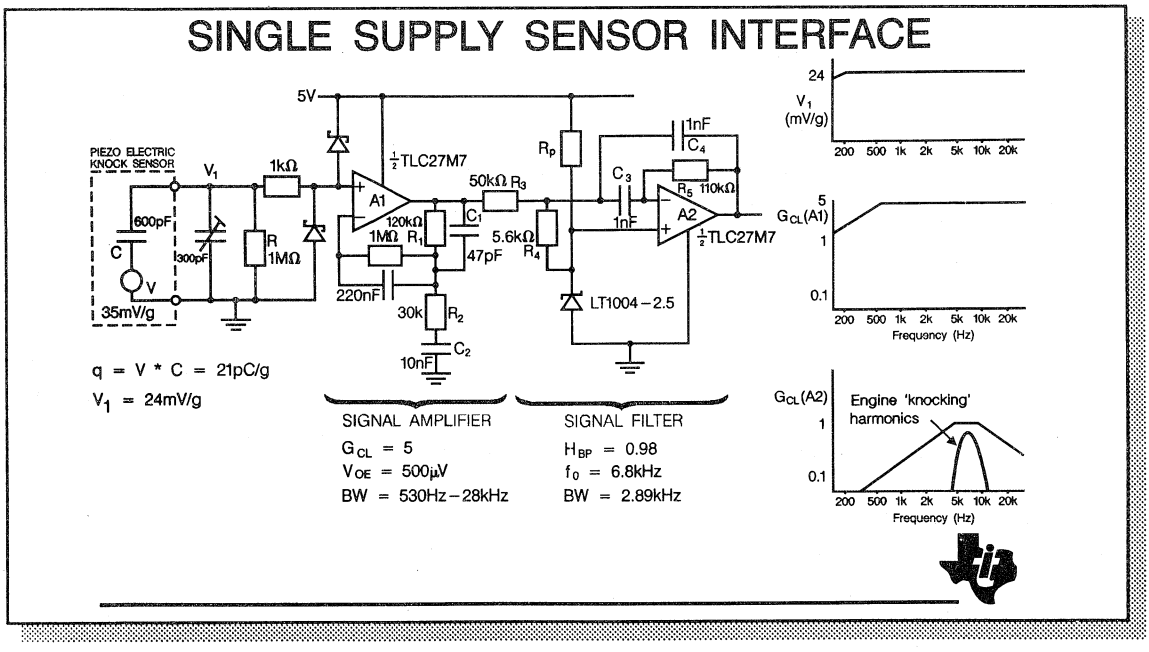


Figure 15 - Single Supply Sensor Interface

The increase in use of electronics in the automotive industry has brought about the need for single supply op amps, capable of operating from a +5V supply. The LinCMOS family of devices was designed for these applications, using a PMOS input stage gives the common-mode range down ground, while an all NMOS class A output stage gives it an output swing which also includes ground.

This application shows the TLC27M7, utilising these features, interfacing to a piezoelectric pressure sensor used to sense knocking in an internal combustion engine. The first op amp is in a non-inverting configuration, making use of its high input impedance and its common-mode range down to the negative rail.

The piezoelectric sensor is an ac sensor and can be modelled by a voltage source in series with a capacitor. The sensor can be considered as working in two modes one as a sensors which produces charge or as a sensor which produces ac voltages. In this application the TLC27M7 is amplifying the voltage produced by the sensor.

Interfacing to the sensor is a 1MΩ resistor and a calibrating capacitor, this capacitor can be used to alter the high pass cut-off frequency of the sensor as well as affecting its gain. The shunt resistor is included to provide both a current path for any bias currents of the op amp and to provide a current path for any current flowing out of the sensor. In order not to load the sensor this shunt resistor needs to have a large resistance, and for this reason the TLC27M7 is ideal. No bipolar op amp has a high enough input impedance and more importantly low enough bias currents to be able to interface with these resistances.

The first op-amp, acting as the sensor interface, doubles as a wideband filter amplifying the input signal plus filtering out signals which are not of interest. The second op amp in the TLC27M7 is connected in a Delyiannis-Friend configuration producing a bandpass filter, which is used to filter out all other signals.

The advantages of this circuit is that all the filter's key parameters can be designed and decided sequentially, simplifying the design process. The input resistors act as attenuators bringing the gain of this filter to unity. The centre frequency of the circuit is determined by the feedback resistor, R_5 , and the thevenin equivalent of the input attenuating resistors, R_{TH}.

$$\omega_o = \frac{1}{C * \sqrt{R_5 R_{TH}}}$$

and

$$R_{TH} = \frac{R_3 * R_4}{R_3 + R_4}$$

The quality factor, Q, of the filter depends solely on the ratio of the feedback resistor to the thevenin equivalent of the input resistors.

$$Q = \frac{1}{2}\sqrt{\frac{R_5}{R_{TH}}}$$

Notes

When engine knock starts to occur the sensor will generate a range of signals, whose frequency is not present when the engine is running properly, which the second op amp is used to exclusively amplify. The characteristic knock frequency of the engine will change depending on the size of the cylinders and the cylinder block's material. To meet all these changes in frequency a wideband sensor and a versatile op amp are requite; most of these sensors have bandwidths into the tens of kilohertz, meaning that one form of sensor should suit almost all applications. The TLC27M7 with a unity gain bandwidth of 600kHz and an input offset voltage of 500μV provides the accuracy and speed required by the system, without using capacitive coupling.

This example typifies a usual LinCMOS™ op amp application requiring low bias currents and low quiescent currents whilst providing accurate signal conditioning.

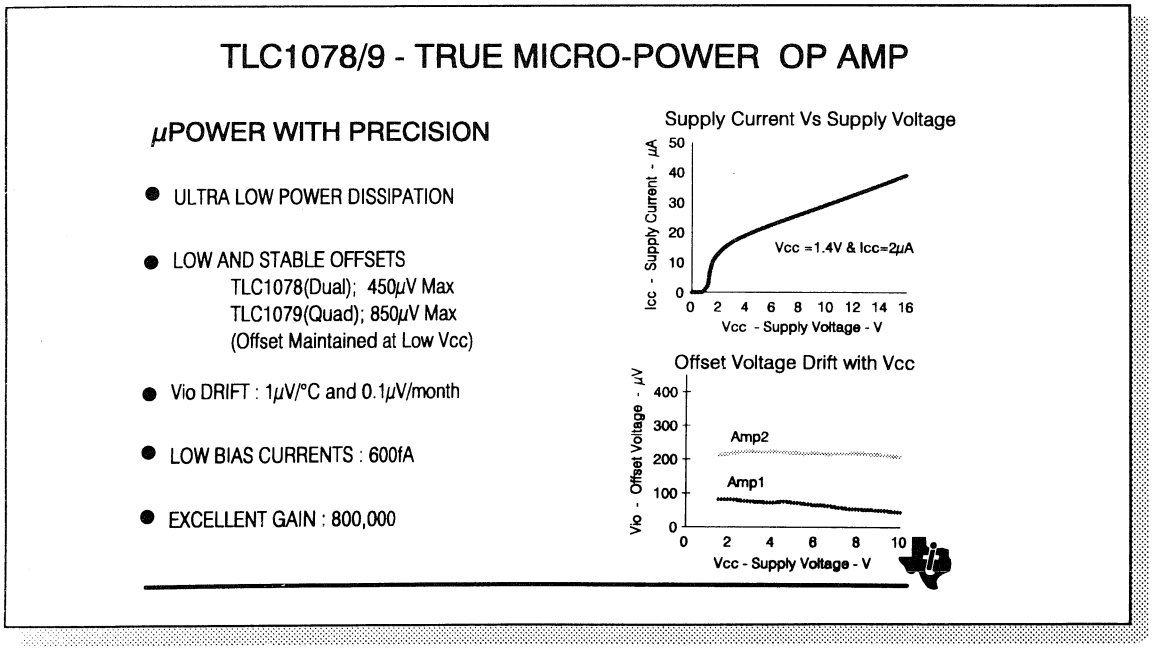


Figure 16 - TLC1078/9 - True Micro-Power Op Amps

The TLC1078 and TLC1079 were developed as an extension to the existing LinCMOS™ family of op amps. They were designed and optimised to combine true micropower operation with excellent precision.

These devices will operate over the1.4V to 16V supply voltage range - power consumption is always low but it reduces with supply voltage and at 1.4V the device typically consumes 2μA of supply current per channel.

For precision operation the TLC1078 has a maximum offset voltage of 450μV with extremely low drift of 1μV/°C and 0.1μV/month. Unlike bipolar devices which may appear to achieve better levels of performance, these devices continue to sustain these low offset voltages even

when the supply voltage drops below the characterised value. Some bipolar designs experience an offset voltage increase of 5 fold as the supply voltage reaches it lower limits!

The other key parameters for DC precision designs are low bias currents and high open loop gain. Because the device is CMOS, bias currents are obviously low and introduce minimal DC errors. An added advantage is that they also cause negligible power dissipation in external resistors - a key factor in low power designs.

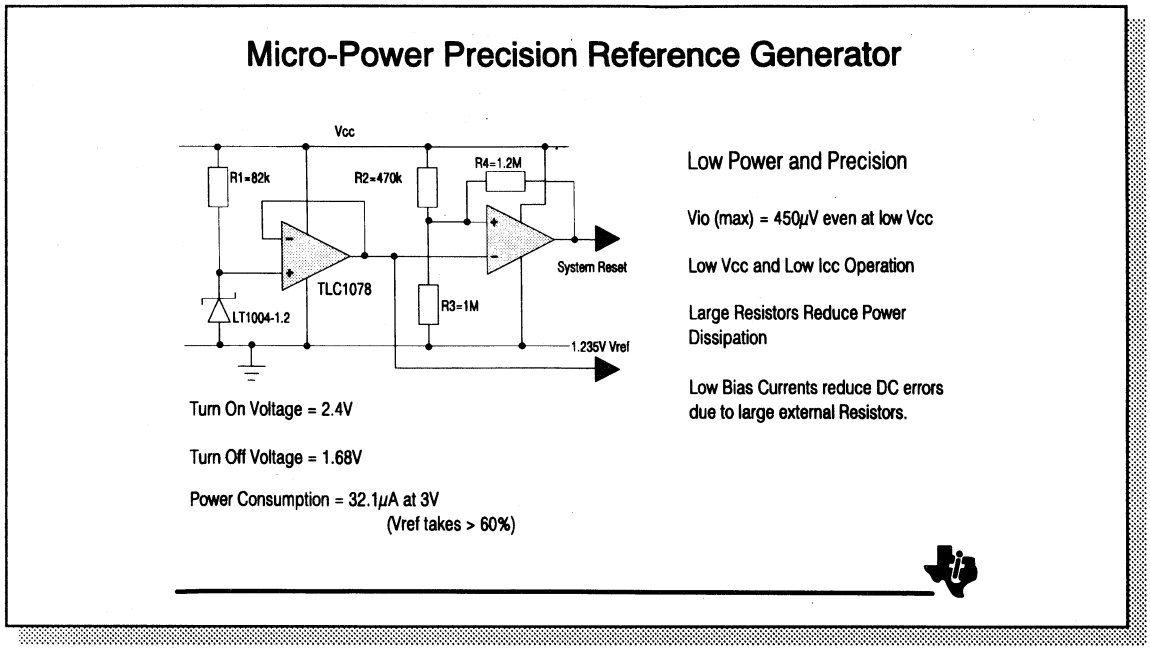


Figure 17 - Micro-Power Precision Reference Generator

Although a relatively simple circuit this application highlights very well many of the factors to be considered when designing low power, precision applications.

This circuit is targeted at low power, portable battery driven circuits and therefore the major requirement for this application is that power consumption should be kept at a minimum and that the circuit should operate at very low supply voltages. A dual op amp, the TLC1078, has

Notes

been chosen to build a circuit which both supplies a precision reference and also generates a 'System Reset' signal (with hysterisis) when the power supply drops. The 1.235V reference can be used to supply other parts of the circuit (anything from a/d convertors to comparators) and the Reset signal can be used to instigate battery-back-up or activate an external signal to show that the battery is running low.

The factors considered in this design were;

Low and Stable offsets;
Although not normally recognised as real precision amplifiers the op amp's chosen in this application are CMOS designs. Designed using the LinCMOS^{TM} technology, both amplifiers in the TLC1078 op amp have a maximum offset voltage of just 450μV. A bipolar op amp, with a lower specified offset voltage could have been chosen, but the relative final precision of such a device may actually have been worse.

Many low power bipolar op amps suffer from a significant increase in offset voltage as the supply voltage is reduced. A device specified with 100μV offset at 5V, is likely to have a much worse V_{IO} at lower supply voltages.

Low Bias Currents;
The second important factor to consider is the low input bias currents associated with CMOS designs. The DC error caused by bias currents flowing through external resistors is significantly higher for bipolar op amps than CMOS designs.

Bias currents are of particular importance when used in low power circuits. All resistors used in this application are large to reduce power dissipation, and therefore the DC error caused by bias currents flowing through these resistors is increased! There is therefore a trade-off between low power dissipation and absolute precision.

Low Vcc and Icc Operation;
The TLC1078 used in this application will operate from supply voltages as low as 1.4V and from supply currents less than 10μA. In this application the majority of current is consumed by the 'Low Power' reference. At 3V, the power consumption is 32.1μA, of which the reference consumes over 60%.

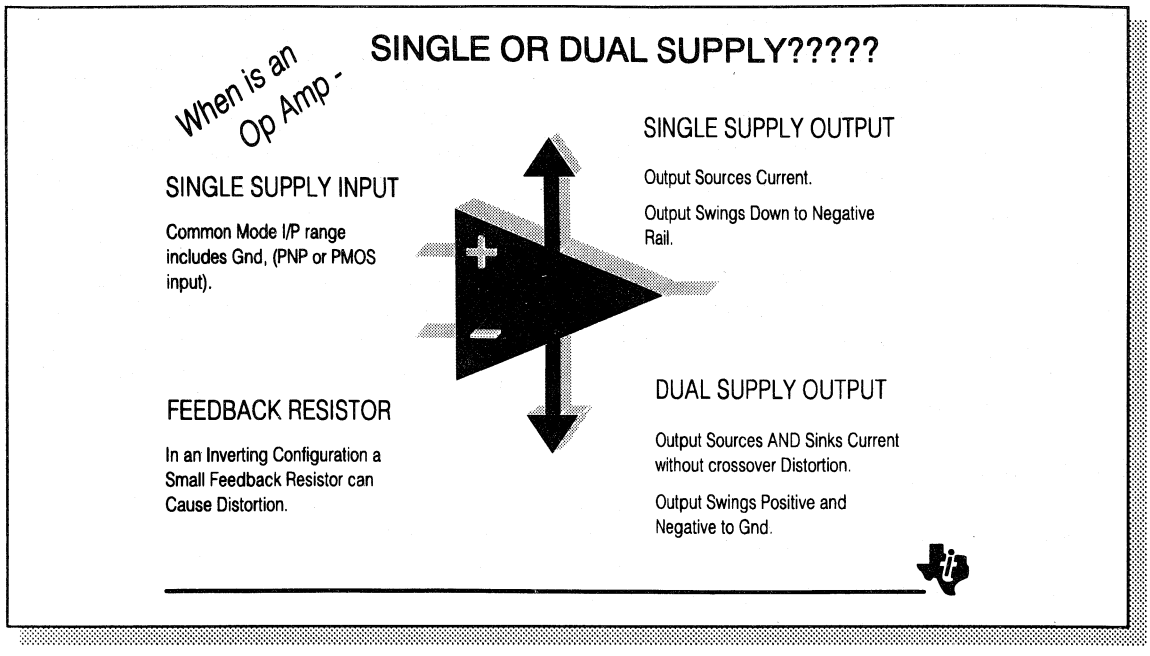


Figure 18 - When is an Op Amp Single or Dual Supply?

There are a number of fundamental differences between operational amplifiers that have been developed for either single or dual supply applications. Many design problems are caused by an engineer using an op amp with the wrong configuration of power supplies. By understanding a few basic ground rules, often technology related, it is possible to ensure an op amp is always used correctly.

Transistor Type on Input
A single supply op amp should have a Common Mode input voltage range that includes the negative supply rail (usually ground) and have an output that also swings very close to this rail.

A Common Mode input range that includes the negative rail can be achieved by using the following transistor types on the op amp's input; PNPs, 'P-Channel' Mosfets or 'N-Channel'

Notes

JFETs. Bipolar op amps can easily be designed with PNPs on the input and therefore single supply performance can be easily achieved from bipolar technologies. CMOS devices make good single supply op amps because they use PMOS transistors on the input stage, but Bifets have a problem! 'N-Channel' JFETs exhibit very poor stability and high leakage with high drain-gate voltages, and today are rarely used in the input stage of an op amp. Bifets then, use 'P-Channel' JFETs on the input and are therefore not developed for single supply applications.

Bifets and bipolar op amps with NPN input stages do however have their benefits. They now have a Common Mode input range that can include, (and in the case of the TLE2061 family actually exceeds) the positive rail. This is useful in various 'High-Side Monitoring applications' such as power supply circuits. NPNs also have the advantage of enabling op amps with lower noise and increased gain and precision.

Output Stage Design

The second requirement for a single supply op amp is that the output must swing very close to the negative rail. In the case of CMOS designs this is easily achieved by using NMOS transistors on the output - developing an output that swings to within a few microvolts of the ground is relatively simple. In this type of circuit the output has been designed to predominantly source current.

Bifet and bipolar op amps can effectively use the same type of bipolar output stage but developing an output that swings down to the negative rail using these technologies is not so simple. In op amps such as the LM324, the output has been designed specifically to source current, and for use in single supply applications. The typical requirement, however, for the majority of amplifiers designed using bipolar or Bifet technologies is that they are able to both **Sink and Source current -** ie they are capable of driving a load that is connected to the mid point of their supplies without crossover distortion. This feature, when combined with the capability of the output to swing all the way to the negative rail makes the design of an output stage very complicated. Clever design techniques are therefore needed to realise true single supply bipolar op amps. Devices such as the TLE2141 and LT1013 are examples of products that perform well in both situations - they have an output that swings to the negative rail but they can also sink and source current.

Other newer bipolar op amps are also often termed single supply amplifiers - their common mode input range includes ground and their output swings very close to, if not all the way to the negative rail. An example is the TLE2021 family, these designs are ideally suited to many single supply applications and are very different to products which have been optimised for dual supply applications only.

Newer CMOS designs are also being developed for use with both single and dual supply rails. Op amps such as the TLC2201, TLC2652 and TLC2654 are excellent with a single supply, and their output will swing all the way down to the negative rail. With dual supplies their output will happily sink and source current, and will swing to within a few hundred millivolts of each rail without causing distortion.

Figure 19 shows what errors can occur if an op amp, designed for single supply circuits, is used in a dual supply configuration.

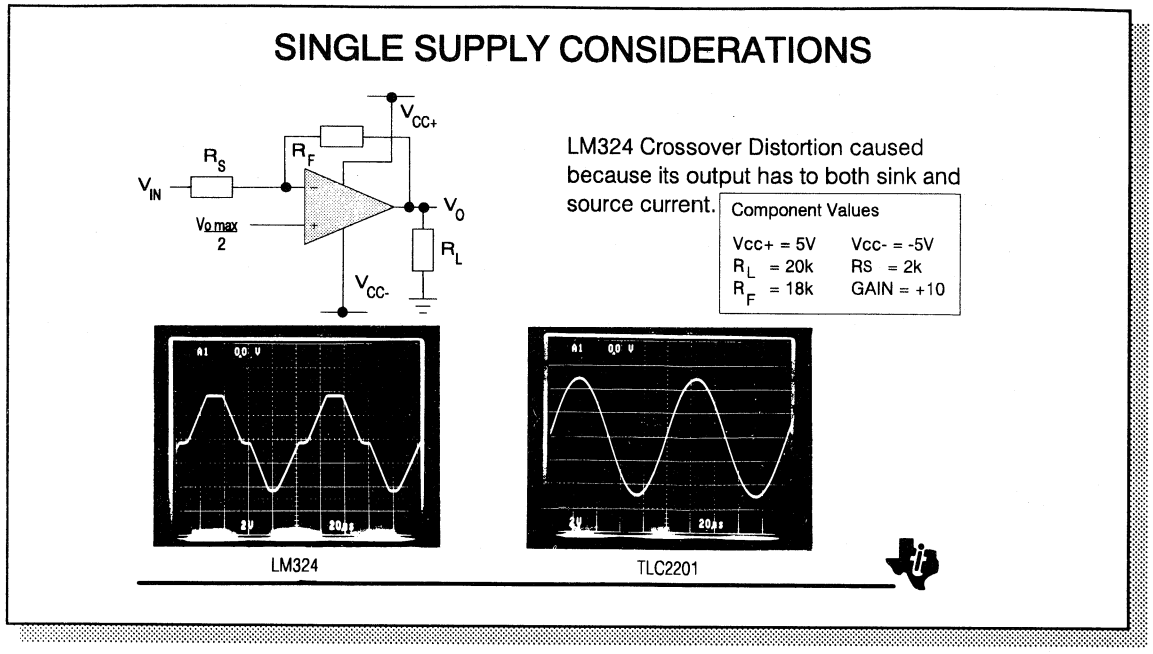


Figure 19 - Single Supply Considerations

Figure 18 effectively put single supply op amps into two categories;

1) Those whose output can source current only
2) Those that can both sink and source current and have been designed to drive a load which is connected to the mid point of the supplies.

If a single supply op amp, such as the LM324, is used in an application where it needs to both sink and source current then the output signal may be heavily distorted. The device has not been designed to make the cross-over from sinking to sourcing current smoothly, and therefore distortion is very apparent - see photo on left. This problem is also made worse because the load being driven in this application is not easily handeled by this device. If the load resistor is increased then the amount of distortion will reduce. Remember that the feedback resistor is seen as a load and that to reduce distortion it should be kept large.

Notes

The photo on the right shows the TLC2201(a single supply CMOS op amp), used in the same circuit as the LM324. This device outperforms the LM324 in several ways;

1) The device is designed to sink and source current and also has the ability to work like other CMOS parts in single supply applications
2) The TLC2201 can drive heavier loads than the LM324 - the equivalent load here is 10kΩ and the LM324 is beginning to suffer.
3) The TLC2201 has a much wider output swing. With +/-5 V supplies the output will swing to +/- 4.7 V - true single supply operation.

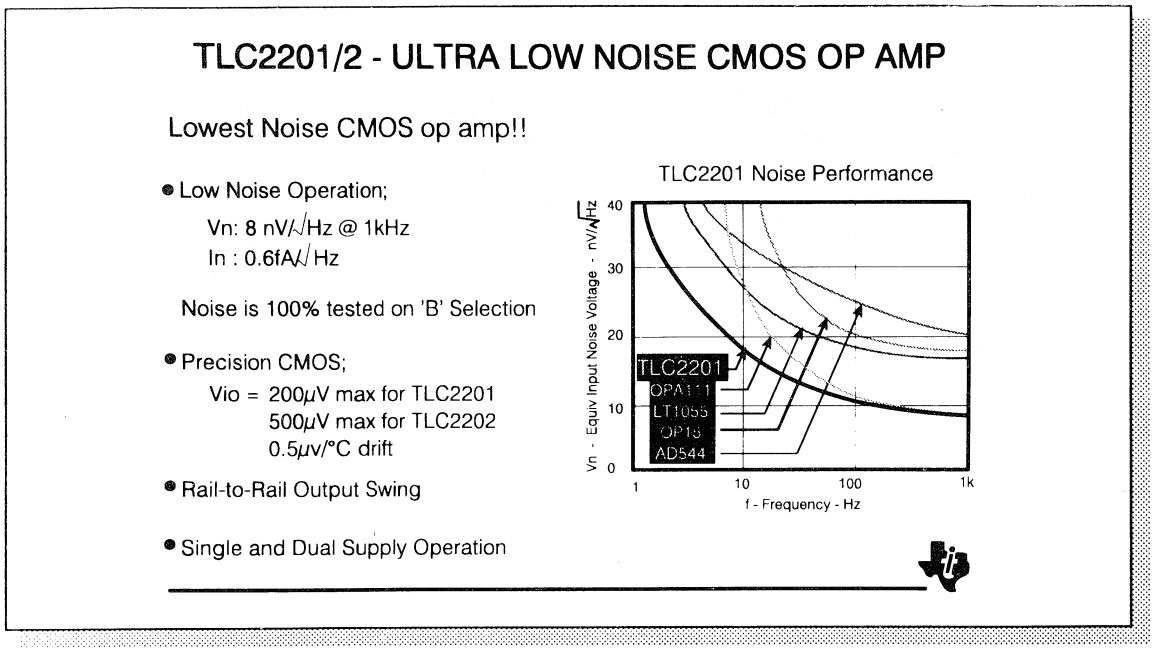


Figure 20 - TLC2201/2 - Ultra Low Noise CMOS Op Amps

The TLC2201 and TLC2202 are among the **WORLDS lowest noise** CMOS or JFET input operational amplifiers. Designed using Advanced LinCMOS™ technology, these precision op amps have proved extremely popular in a number of different applications.

Noise Performance - CMOS devices typically suffer from relatively high noise voltage and high 1/f frequency. Normally performing worse than Bifet op amps, they are typically not used in critical low noise applications. What all FET input devices benefit from however is a low noise current specification. Figure 21 explains why this is critical when interfacing to high impedance sources.

The TLC2201 and TLC2202 are unique because they combine low noise voltage (V_n) with extremely low noise current (I_n). A V_n specification of **8nV/√Hz (@ 1kHz)** easily compares with some bipolar op amps, while I_n equal to **0.6fA/√Hz**, matches the very best FET input amplifiers. The result is an op amp which can now be used in a wide range of low noise

applications. It achieves outstanding performance when interfacing to even medium impedance sources and can replace discreet JFETs or matching transformers to achieved improved performance and lower costs.

The noise performance is specified with single(5V) or dual supplies (higher supply voltages are more typical) and its performance is guarantied for the 'A' and 'B' selections ('A' by sample test, 'B' by 100% test).

Precision - The TLC2201 is one of the worlds most precise CMOS op amps (non chopper stabilised). A maximum offset voltage of 200µV combined with its obvious low offset and bias currents enables the device to be used in many precision applications.

Rail to Rail Output Swing - Like other LinCMOS^{TM} op amps, the TLC2201 and TLC2202 are ideally suited to single supply applications - under normal conditions the output is guarantied to swing within 50mV of the negative rail. A further benefit of these devices however is the ability of the output to actually swing to each rail - With +/- 5V supplies the output will swing to +/-4.7V. In single supply applications dynamic range is often crucial and the ability of these devices to provide an increased output signal significantly improves the performance of single supply circuits.

Applications - Both devices offer a number of benefits to a wide range of applications. Low noise enables the device to be used as an interface to high impedance sensors including piezoelectric transducers, pH meters and pin diodes. The devices are therefore ideal for test and measurement equipment. Rail to Rail output swing increases the performance and capability of single supply circuits, and when combined with its precision the device is ideal as an accurate signal conditioning interface in data acquisition circuits.

Notes

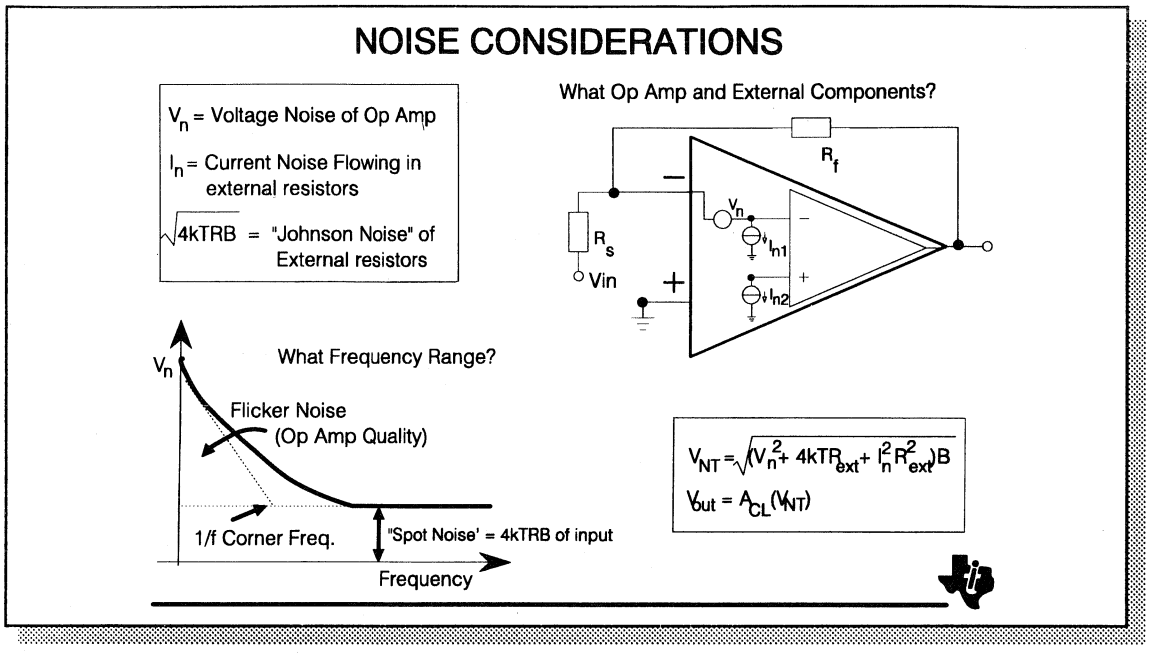


Figure 21- Noise Considerations

There are a number of factors to consider when developing a low noise circuit using operational amplifiers, these are discussed below:

Sources of noise

Johnson (or Thermal) Noise;
A resistor lying on a table will have a particular noise associated with it. Known as "Johnson Noise", this figure is not related to the quality of the resistor and its noise voltage is equal to;

$$V_n = \sqrt{4kTRB}$$

Where k = Boltzmann's Constant = $1.38 * 10^{-23}$ J/K
T = Absolute temperature in kelvin = (298 @ 25°C)
R = Resistance value
B= Noise Bandwidth in Hz.

It is often useful to remember that a 100kΩ resistor has a Johnson Noise equal to 40nV rms over a 1 Hz bandwidth.

Johnson Noise is unpredictable but has a gaussian distribution, giving it a flat spectrum over frequency. It must also be remembered that this Johnson Noise is independent and extra to the errors caused by current flowing through the resistor.

In a low noise circuit the Johnson Noise of the external source resistor is often the limiting factor and it is one which can not readily be reduced. An alternative source may be the only solution!

Shot Noise;
Shot Noise(or schottky noise) is associated with the current flowing through a pn junction and is actually due to fluctuations in current. Shot noise becomes more dominant the lower the value of the actual current;

$$I_n = \sqrt{2qI_oB}$$

Where q = Electron Charge = $1.6 * 10^{-19}$ C
Io = DC operating Current
B = Noise Bandwidth in Hz

Like Johnson Noise, Shot Noise is unpredictable and is gaussian in distribution and is referred to as having a 'white' spectrum..

1/f or Flicker Noise;
Both operational amplifiers and resistors have noise characteristics different to what is expected from the Johnson Noise calculations. At low frequencies, noise is significantly increased, and follows a 1/f characteristic - ie the noise spectrum has an equal amount of power per decade of frequency. This noise, known as Flicker Noise, is very much dependent upon the quality of both the op amp and resistor. A Wire-wound resistor will have a lower noise than a carbon equivalent.

With operational amplifiers the amount of Flicker noise is very dependant upon the quality of the op amp and the level of care put into the design as well as the actual process being used. The point at which the flicker noise crosses the constant 'Spot Noise' of the op amp is known as the 'corner frequency'.

Popcorn Noise;
Popcorn Noise sounds like noise popping when played through a speaker. It is characterised by "hopping" between different noise levels, and can last from milliseconds to seconds. The source is not clearly understood but is reduced by cleaner processing. Good low noise processes should have no popcorn noise.

Notes

Summing Noise Sources

Noise Sources are random and therefore should be geometrically or RMS summed. The most well recognised formula for working out the total noise of an operational amplifier circuit which includes the different noise sources is;

$$V_{nt} = \sqrt{(V_n^2 + 4kTR_{ext}^2 + I_n^2R_{ext}^2)B} \quad \text{.....(1)}$$

Where V_n = Voltage Noise of Op Amp
I_n = Current Noise of Op Amp
$4kTR_{ext}$ = Johnson Noise of external Resistors.

Noise Related to an Op Amp

There are typically two parameters specified in the datasheet of an operational amplifier, noise voltage and noise current;

Noise Voltage;
The noise voltage of a bipolar op amp is due to the Johnson noise of the base spreading resistor r_{bb} and the Shot noise of the collector current in the input transistors. There is also an error due to the flicker noise, associated with the input transistors base current flowing through the base resistors. At low frequencies the noise is dominated by the Flicker noise whilst at high frequencies, the Johnson noise is the major factor.

The noise voltage of a FET input amplifier is dominated by the Johnson noise of the channel resistance and is normally significantly higher than a bipolar design.

The noise voltage characteristics for both parts have a 1/f characteristic although the 'corner frequency' of FET input designs is typically much higher than for bipolar. It should also be noted that CMOS designs have a worse 1/f noise compared with Bifet op amps, but newer products developed using 'cleaner' CMOS technologies such as LinCMOS™ have greatly improved the noise performance and lowered the 1/f corner frequencies.

The 1/f region of the noise curve of an amplifier is particularly critical when designing precision circuits which operate at relatively low frequencies - very common in instrumentation equipment. An op amp with a low 1/f corner frequency is essential.

Current Noise;
For operational amplifiers with a bipolar input stage, the noise current is caused by Shot noise variations of the base current and flicker noise of r_{bb}. FET input amplifiers have a noise current specification caused by the shot noise associated with the gate leakage of the input FETs, this is significantly lower than for bipolar designs.

An op amp's noise current flows through the external resistors of an op amp generating an error source equal to $\sqrt{I_n^2 R_{ext}^2 B}$ - therefore the larger the external source resistors the larger the error due to noise current. Because the base current of a bipolar transistor is much

higher than the leakage current of a FET transistor, the noise current of a CMOS or Bifet part is much lower than a bipolar design. FET input amplifiers are therefore normally used if a circuit has a large source resistance. As the bias current of a FET input part doubles for every 10°C increase in temperature, the noise current, In, increases by $\sqrt{2}$ for every 10°C increase.

Equation (1) above, shows how these parameters are combined. The result from this equation is in fact an RMS term which is often preferred in its in its peak to peak form. If the RMS noise voltage is multiplied by 6.6, you have a 99.7% certainty that the peak to peak value will not exceed the result.

Further examination of equation (1) shows that there is a point at which the noise of a system is dominated by the external resistors. A term, of particular use when talking about bipolar op amps is the 'Equivalent Noise resistance', equal to V_n/I_n shows when the errors due to the noise current are than that due to the noise voltage

Noise Bandwidth

It can be seen from equation (1), that the Noise Bandwidth of the operational amplifier circuit is critical - the wider the frequency of operation the larger the amount of noise within that system. A low noise circuit must therefore have its noise bandwidth limited as much as is possible.

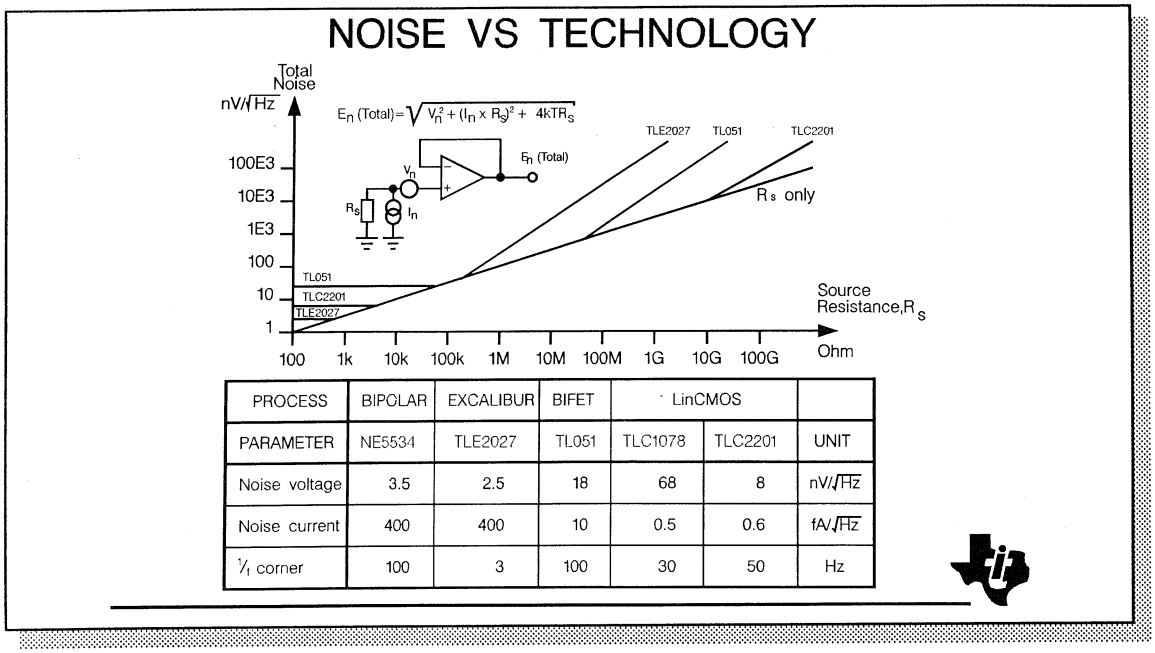
The Noise Bandwidth of an operational amplifier circuit is normally limited by using a filter network. It must be remembered however that the Noise Bandwidth is often very different to the RC Bandwidth of the filter which is limiting the noise. If a filter has a slow rolloff then the noise contribution by the signals with a higher frequency than the RC bandwidth can be significant. The Noise Bandwidth of a 1st order low pass filter (butterworth) is 1.57 x f_{3dB} of the filter. This is an increase of over 50%. A filter is of least 2 orders is normally recommended.

FILTER ORDER	NOISE BANDWIDTH
1	1.57 x f_{3dB}
2	1.11 x f_{3dB}
3	1.05 x f_{3dB}
4	1.03 x f_{3dB}
"Brick Wall"	1.00 x f_{3dB}

Notes

Noise on Output

Most noise calculations will work out the equivalent total noise on the input of the op amp. Like other errors this noise error is multiplied by the closed loop gain to give the equivalent noise on the output of the op amp.



PROCESS	BIPOLAR	EXCALIBUR	BIFET	LinCMOS		
PARAMETER	NE5534	TLE2027	TL051	TLC1078	TLC2201	UNIT
Noise voltage	3.5	2.5	18	68	8	nV/√Hz
Noise current	400	400	10	0.5	0.6	fA/√Hz
$1/f$ corner	100	3	100	30	50	Hz

Figure 22 - Noise vs Technology

The previous figure discussed the relevance of noise voltage and noise current and how depending upon the source impedance each or both may be of importance. The graph and table in the figure above compares the overall noise performance of low noise op amps from each major technology. The formula to remember is;

$$V_{nt} = \sqrt{(V_n^2 + 4kTR_{ext}^2 + I_n^2R_{ext}^2)B}$$

V_n = Noise Voltage of Op Amp
I_n = Noise Current of Op Amp
$4kTR_{ext}$ = Noise of Resistors.

This figure shows that bipolar amplifiers are the best for a that, providing the source resistance is small, low noise voltage. Amplifiers like the TLE2027 have extremely low noise voltage specifications which means that, providing the source resistance is small, they achieve the best overall noise performance.

As the size of the external resistors increases, the Johnson noise of these components begin to dominate the total noise equation. Not surprisingly, the lower the value of the op amps noise voltage, the smaller the resistor needs to be before it begins to prevail - resistor size can prove a severe limitation when designing low noise circuits with low noise op amps.

As the source impedance increases, there comes a point when the noise current, In, flowing through these resistors dominates the total noise equation. Because bipolar resistors have a significantly higher noise current than FET input amplifiers, this error term can quickly cause the largest error. Low noise CMOS designs like the TLC2201 have such a low noise current specification, combined with a relatively low noise voltage, that it is often the best choice even with medium sized external source impedances.

The other specification highlighted by this figure is the 1/f corner frequency of the op amp. Low noise bipolar designs will normally have much lower specifications than FET input designs (3Hz for the TLE2027), although again, the TLC2201 has a very good specification relative to other FET input designs. It is worth noting that the NE5534 has a high 1/f corner frequency and yet it is still recognised as a low noise part - 1/f should not necessarily be used to compare the performance of different amplifiers.

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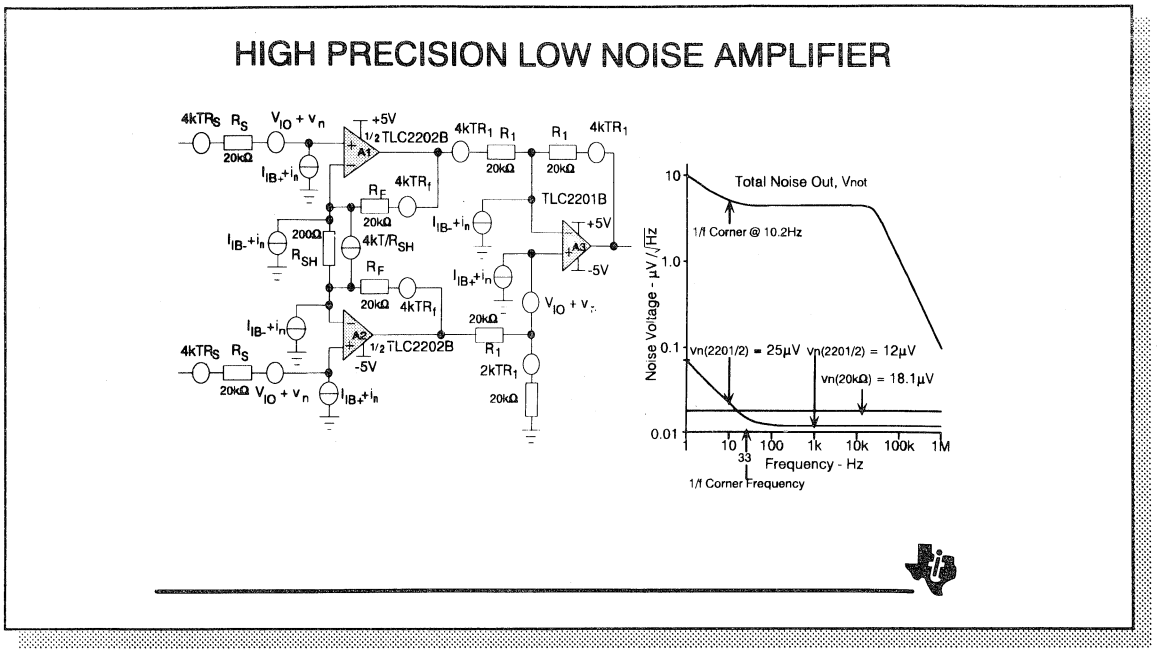

Figure 23 - High Precision Low Noise Amplifier

When designing low noise systems the voltage noise of the amplifier is not the only important parameter. The wide variety of transducers, and their resistances, can often make the noise voltage of the op amp negligible when compared to the Johnson noise of these resistances. With very high impedance transducers the noise current of the amplifier dominates the total circuit noise.

In most applications involving the TLC2201B and TLC2202B operational amplifiers the thermal noise of the source and/or feedback resistors will be the most important. This is due the TLC2201/2 having a maximum noise voltage of only $12nV/\sqrt{Hz}$ and a noise current of $2.53fA/\sqrt{Hz}$ (@25°C), giving it an effective noise resistance (ratio of noise voltage to noise current) of above 4MΩ. This means that only when dealing with impedances above 4MΩ is the effect of the noise current of the TLC2201 going to be larger than its noise voltage. The offset error that this impedance would create would be 80μV.

The 3 op amp instrumentation amplifier is a versatile configuration and can be used to yield the best performance from an op amp; in particular the TLC2201 with its high input impedance, good common-mode rejection ratio as well as its excellent input and output swings.

As in most low noise systems the input stage will have the largest effect on the signal to noise ratio. Using the TLC2202 in the input stage makes use of its very low noise currents and noise voltages as well as its very low offset voltage. The common-mode range down to the negative rail adds further versatility to the application whilst maintaining the accuracy required.

When working out the noise of a system it is best to relate each stage's noise to its input. This will normally make analysis easier, as both the input signal and the input referred noise will be multiplied by the op amp's non-inverting gain, $1+ R_f/R_{sh}$, (signals via the inverting input will be multiplied by $-R_f/R_{sh}$). The instrumentation amplifier configuration adds some further complexity to the analysis; with the input stage sharing a resistor, R_{sh}, between its two op amps' inverting input terminals. The use of R_{sh} is two-fold; A, R_{sh} provides the instrumentation amplifier with its good common-mode rejection characteristics, and B, R_{sh} sets the gain at $1+2R_f/R_{sh}$. With the input stage sharing R_{sh} between the two op amps it is easier to consider the thermal noise of R_{sh} to be in the form of a current ($4kT/R_{sh}$), which adds to the noise current of each op amp's inverting input.

The sources of noise for both input stage op amps will be the same. The non-inverting input will exhibit the noise voltage, v_n, of the op amp itself, in addition will be the thermal noise of the source resistor, $4kTR_S$, and the noise generated by the noise current, i_n, through R_S. These voltages are uncorrelated and will therefore RMS sum together. Due to the virtual short across the op amps' inputs (the very high open loop gain forces the two inputs together) the noise voltage at the non-inverting input will appear at the inverting input. This means that the total noise on the non-inverting input will be multiplied by the inverting gain of the opposing op amp in the input stage. So the noise generated on the non-inverting input, v_{ni+}, of each op amp will be:-

$$v_{ni+} = \sqrt{v_n^2 + 4kTR_S + i_n^2R_S^2}$$

The noise current on the inverting input will flow through the feedback resistor, R_f, creating a noise voltage at each op amp's output, which sums together with the thermal noise voltage of R_f. The noise current on the inverting input will be the noise current of the device plus the thermal noise current of R_{sh}. As this noise voltage is at the output of the op amp (just as the bias current error is added to the output of the op amp), referring it to the non-inverting input entails dividing it by the non-inverting gain. The resultant is the noise generated by a resistance equivalent to R_{sh} in parallel with R_f. This extra source generates further non-inverting input referred noise. However it will not appear at the inverting input, as the noise is actually being generated at the output.

Notes

Therefore the total noise voltage referred to the input, $v_{nri(1)}$, of amplifier A1 will be the noise generated at the non-inverting input summed with the noise due to the parallel combination of feedback resistor, R_f, and shunt resistor, R_{sh}. Therefore:-

$$v_{nri(1)} = \sqrt{v_{ni+(1)}^2 + i_{n(1)}^2 * \left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)^2 + 4kT\left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)}$$

and the input referred voltage, $v_{nri(2)}$, of amplifier A2 will be:-

$$v_{nri(2)} = \sqrt{v_{ni+(2)}^2 + i_{n(2)}^2 * \left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)^2 + 4kT\left(\frac{R_f * R_{sh}}{R_{sh}+R_f}\right)}$$

The third amplifier will have a similar equation except that R_S will be replaced with $\frac{1}{2}R_1$ and $R_{sh}R_f/(R_{sh}+R_f)$ will be replaced with $\frac{1}{2}R_1$, yielding:

$$v_{nri(3)} = \sqrt{v_{n(3)}^2 + 2*4kT(\frac{1}{2}R_1) + 2 * i_n^2*(\frac{1}{2}R_1)^2}$$

The output of A1 (*and for A2*) will be $v_{nri(1)}$ ($v_{nri(2)}$) multiplied by the non-inverting gains RMS summed with $v_{ni+(2)}$ ($v_{ni+(1)}$) multiplied by its inverting gain. Assuming all op amps have the same worst case noise voltages and currents, the output noise voltage, $V_{no(1)}$ of A1 will be:-

$$V_{no(1)} = \sqrt{\left(1 + \frac{R_f}{R_{sh}}\right)^2 * v_{nri+}^2 + \left(\frac{R_f}{R_{sh}}\right)^2 * v_{ni+}^2}$$

Op amp A2 will have a similar output noise voltage. The third op amp A3 will multiply the noise voltages from A1 and A2 by its inverting gain. It will RMS sum these together with its own noise voltage (which is multiplied by its own non-inverting gain), yielding a total output noise voltage, V_{not}, of:-

$$V_{not} = \sqrt{2 * \left(1 + \frac{R_f}{R_{sh}}\right)^2 * v_{nri+}^2 + 2 * \left(\frac{R_f}{R_{sh}}\right)^2 * v_{ni+}^2 + 2 * v_{nri(3)}^2}$$

To maximise noise rejection, the gain of the first stage will normally be large while the gain of the last stage will be small (frequently, as here, unity to minimise any common-mode errors), and so reducing the effect of the final stage's noise. Using bipolar input op amps in the final stage will have a greater effect on the noise level due to their much larger noise currents. These larger noise currents place a compromise on the limit on the range of values for A3's source resistors, smaller source resistors generate less noise voltages, but load the input stage op amps' outputs introducing distortion.

With R_f=20kΩ, R_{Sh}=200Ω, R_1=20kΩ, R_S=20kΩ the non-inverting gain of the input stage will be 101 and the inverting gain will be 100. These values coupled with the TLC2201B/2B's maximum noise voltage of 12nV/$\sqrt{Hz}$ (guaranteed at 1kHz) and noise current of 2.53fA/$\sqrt{Hz}$ (calculated for 1kHz) the following values are achieved.

For A1 and A2

$$V_{ni+} = 21.7nV/\sqrt{Hz}\ V_{nri} = 21.8nV/\sqrt{Hz}$$

$$V_{no} = 3.10\mu V/\sqrt{Hz}$$

and for A3 $V_{nri} = 21.7nV/\sqrt{Hz}$

The resulting output noise voltage, V_{not}, spectral density for the TLC2201/2 instrumentation amplifier will be:-

$$V_{not} = 4.39\mu V/\sqrt{Hz}.$$

Referring this value to the input (dividing by the signal gain = 201) implies an input referred noise voltage of 21.8nV/$\sqrt{Hz}$. This value is dominated by the thermal noise of the source resistor, with a low noise bipolar op amp the noise would be dominated by the noise current of the device. So when interfacing to high impedances the TLC2201/2 provides a very low noise and a highly accurate solution.

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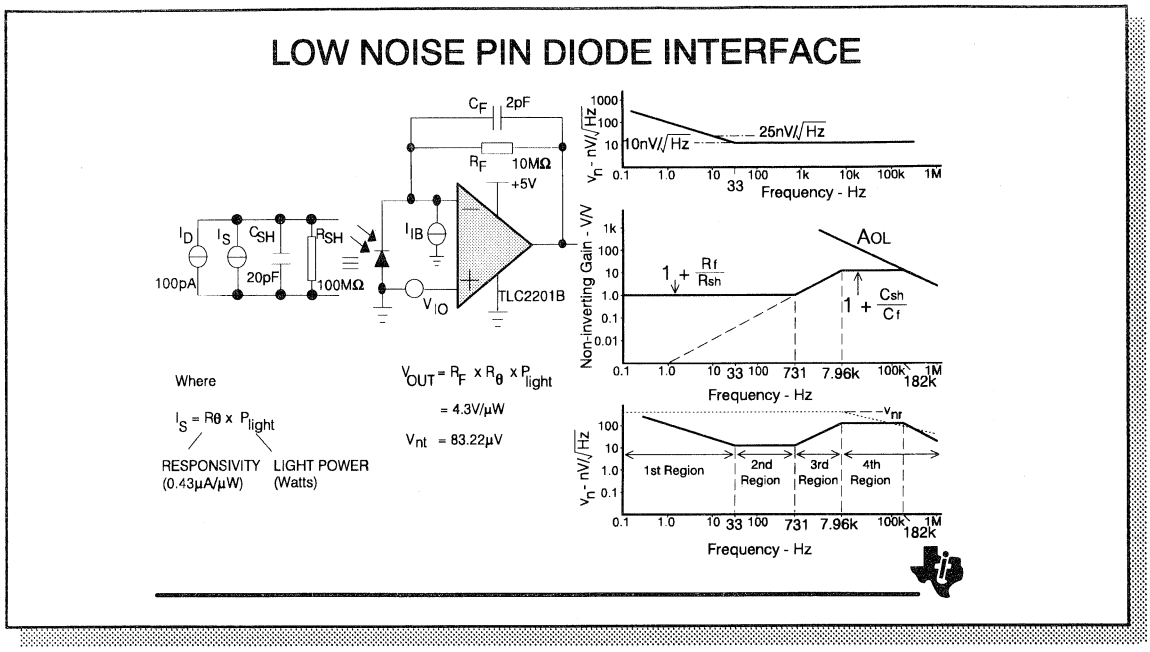

Figure 24 - Low Noise PIN Diode Interface

When interfacing to a wide variety of sensors the key factors in deciding which op amp will be used in the application are high input impedance, low input offset voltages and low noise voltages. A device perfect for applications requiring these specifications is the **TLC2201**.

No application shows the need for such parameters more clearly than when interfacing to a PIN photo-diode. Once again as in most applications requiring high input impedances it is the bias currents which are of importance, as feedback will multiply the op amp's input impedance by the circuit's loop-gain.

When using a PIN diode a small `dark' current will flow through it. This dark current is the bias current of the PIN diode. In parallel with the dark current is the current which is due to the light shining onto the device. It is the dark current along with the current noise which decides the error floor of the system. So if the dynamic range is not to be severely degraded the input bias currents of the op amp should be smaller than the dark current of the PIN diode. A typical PIN diode such as hp's 5082-4204 has maximum dark current of 100pA (at zero voltage bias and at 25°C). The TLC2201 with a maximum bias current of 20pA (calculated from the maximum bias current specifications over temperature) at 25°C provides a good safety margin.

The PIN diode is a light power to current converter and as such needs to interface to a trans-impedance amplifier. The result is that in order to get the required gain the feedback resistor of the op amp will normally have to be large. This feedback resistor will form a pole with the shunt capacitance of the diode and the op amp's input capacitance, which can lead to instability. Although this effect may well be reduced by the parasitic board capacitance which is in effect in parallel with the feedback resistor. This `feedback' capacitor can be increased to reduce the circuit's wideband noise, but this will reduce the application's bandwidth. Hence

the required gain decides the value of R_f and the required signal bandwidth decides C_f. As well as converting the signal current to a voltage, the large feedback resistor adds to the offset voltage of the op amp by multiplying the bias currents of the op amp and the dark current of the PIN diode by its value.

The equivalent model of a PIN diode contains a shunt resistance, R_{sh}, which coupled to the feedback resistor gives the op amp a non-inverting gain of $1+R_f/R_{sh}$ (which frequently exceeds unity). It is therefore very important to use an op amp with low offset voltages and drift. The PIN diode's shunt capacitor also provides a limit to the range of frequencies over which the diode can be operated. Like all semiconductor barrier capacitances it is very voltage dependent, and can be reduced by placing a negative voltage across the diode.

The overall low frequency output voltage will therefore consist of the following factors:-

$$Vo = R_f * R_\varnothing * P_{light} + R_f * I_D + V_{IO} * \left(1 + \frac{R_f}{R_{sh}}\right) + R_f * I_{IB}$$

where $R_\varnothing$ is the responsitivity of the diode to light power (in amperes per watt), and P_{light} is the amount of light falling onto the diode's sensitive area (in watts).

The temperature effects of the PIN diode dominates any drift effects of the op amp's V_{IO}. R_{sh} will tend to halve every 10°C, just as the bias currents will tend to increase. The 0.5μV/°C (typical) drift of the TLC2201 will be swamped by the change in gain due to R_{sh}.

As with all high impedance applications, the input stage is very susceptible to interference and leakage from the board. Any current injection into the input can be converted into millivolts of offset error. For this reason, it is standard practice for guard rings to be placed around the inputs of the op amp, reducing the influence of interference around the board. To decrease leakage of the board a teflon based board will normally give the best performance.

In addition to offset errors, which are DC, noise errors will be introduced due to the PIN diode's noise and the op amp's noise.

The noise current will be the shot noise due to the dark current of the PIN diode and the bias current of the op amp. The noise current of the TLC2201 is $2.53fA/\sqrt{Hz}$ while the dark current of the PIN diode would generate $5.66fA/\sqrt{Hz}$. The feedback resistor will generate noise due to

Notes

the noise currents of the PIN diode and the op amp and also its own thermal noise. A 10MΩ resistor generates 62nV/$\sqrt{Hz}$ (due to shot noise of the PIN diode and op amp) and 406nV/$\sqrt{Hz}$ (due to thermal noise). At these values the noise voltage of the TLC2201 (guaranteed to 25nV/$\sqrt{Hz}$ at 10Hz) would seem to be negligible, but the shot noise and thermal noise appear directly on the output of the op amp while the op amp's noise voltage will be multiplied by the op amp's gain. The op amp's gain will increase above the low frequency gain to $1 + C_{sh}/C_f$. This gain will only be band-limited by the op amp's unity gain bandwidth. The non-inverting gain can rapidly increase over temperature (due to the large variance in R_{sh}, at a faster rate than the current noise, so a low noise voltage device is the best solution.

The non-inverting gain of the TLC2201 is:-

$$G_{cl} = 1 + \left(\frac{R_f}{1 + s * R_f * C_f}\right) * \left(\frac{1 + s * R_{sh} * C_{sh}}{R_{sh}}\right)$$

At low frequencies the R_f/R_{sh} ratio will dominate, and at higher frequencies the C_{sh}/C_f ratio will decide the noise and a.c. gain. The poles of the circuit will be at:-

$$f_1 = \frac{1}{2\pi}\left(\frac{1}{C_{sh} + C_f}\right) * \left(\frac{R_{sh} + R_f}{R_{sh} * R_f}\right) \qquad f_2 = \frac{1}{2\pi * R_f * C_f}$$

With R_{sh} = 100MΩ, R_f =10MΩ, C_{sh} = 20pF and C_f = 2pF the poles are at f_1 = 731 Hz and f_2 = 7.96kHz. f_2 will also be when the trans-impedance gain of the TLC2201 starts to roll off.

At low frequencies the noise voltage of the TLC2201 will be amplified by 1.1 but at the higher frequencies it will be amplified by 10. This splits the noise curve into three distinct parts; the low frequency gain, transition gain and the high frequency gain. At higher frequencies the gain bandwidth product will reduce the gain. A further complication to the noise analysis is the flicker effect of the op amp's noise voltage, and so making 4 regions to the curve.

The first region is from virtually dc to the 1/f corner frequency of the TLC2201B which is of the order of 33Hz. Over this region the noise voltage of the TLC2201 follows this approximate equation:-

$$v_n^2 = \left(\frac{v_{n(10)}^2 - v_{n(1k)}^2}{f} * 10\right) = \frac{4810 * 10^{-18}}{f}$$

Where $v_{n(10)}$ is the noise voltage specification at 10Hz, $v_{n(1k)}$ is the specification at 1kHz.

Calculating the noise over the region of 0.01Hz to 33Hz (ignoring the noise below 0.01Hz) and adapting that equation yields

$$V_{n1}^2 = 4810 * 10^{-18} * \left(1 + \frac{R_f}{R_{sh}}\right)^2 * \ln\left(\frac{f_c}{f_a}\right)$$

$$V_{n1} = 69.35 * \left(1 + \frac{10^7}{10^8}\right) * \sqrt{\ln \frac{100}{0.01}} \ldots\ldots\ldots\ldots\ldots\ldots \text{nV}$$

$$= 231.5\text{nV}.$$

The second region will cover the frequency range 33Hz to 731Hz. Over this frequency range the noise voltage is `white' and so has equal power per unit frequency and so the noise included over this range is calculated as follows:-

$$V_{n2} = v_{nwhite} * \left(1 + \frac{R_f}{R_{sh}}\right) * \sqrt{f_1 - f_c}$$

$$= 12 * \left(1 + \frac{10^7}{10^8}\right) * \sqrt{731 - 33} \ldots\ldots\ldots\ldots\ldots\ldots\ldots \text{nV}$$

$$= 348.7\text{nV}$$

The third region is where the resistances are being shunted out by their parallel capacitances, here the gain is increasing by 20 decibels per decade. By extrapolating this curve down to the 1Hz point the noise produced can be considered as increasing with frequency, simplifying the calculation. The equation of this line is:-

$$v_{n(1Hz)} = \left(1 + \frac{Rf}{Rsh}\right) * \left(\frac{v_{n(1kHz)}}{f_1}\right)$$

The noise content within the f_1 to f_2 band will be the area under this curve, the actual integration will be of the noise voltage squared. Therefore the noise content over this region results in the following equation:-

$$V_{n3} = \left(1 + \frac{R_f}{R_{sh}}\right) * \left(\frac{v_{n(1kHz)}}{f_1}\right) * \sqrt{\frac{f_2^3}{3} - \frac{f_1^3}{3}}$$

$$= 1.1 * \frac{12}{731} * \sqrt{\frac{(7.96*10^3)^3}{3} - \frac{731^3}{3}}$$

$$= 7.40\mu\text{V}$$

Notes

Over the fourth region the noise is flat, but the gain then starts to follow the open loop characteristic of the op amp. This introduces a bandwidth limit of:-

$$BW = \frac{B_1}{1+\frac{C_{sh}}{C_f}} - f_2$$

BW will be multiplied by $\pi/2$ to achieve the noise bandwidth, hence the noise voltage contained in the fourth region has this characteristic:-

$$Vn4 = v_{n(1kHz)} * \left(1 + \frac{C_{sh}}{C_f}\right) * \sqrt{\frac{\pi}{2} * BW}$$

$$= 12 * \left(1 + \frac{20}{2}\right) * \sqrt{\frac{\pi}{2} * 174 * 10^3}$$

$$= 69.0\mu V$$

In addition to the noise voltage from the amplifier, there will be the noise voltage due to the thermal noise of the feedback impedance and to the noise voltage generated by noise current through the feedback impedance.

Only the real part of the feedback impedance produces noise and just as the signal gain rolled off at f_2 so will the thermal noise. The thermal noise will therefore follow this characteristic:-

$$V_{nr} = \sqrt{4kTR_f} * \sqrt{f_2 * \frac{\pi}{2}}$$

$$= 45.4\mu V$$

The noise current will generate a noise voltage equal to:-

$$V_{nc} = i_n * Re\left(\frac{R_f}{1 + s * R_f * C_f}\right)$$

$$= \sqrt{5.66^2 + 2.53^2} * 10^{-15} * R_f * \sqrt{f_2 * \frac{\pi}{2}}$$

$$= 6.93\mu V$$

The total noise voltage will be the RMS sum of all noise voltages:-

$$V_{nt} = \sqrt{V_{n1}^2 + V_{n2}^2 + V_{n3}^2 + V_{n4}^2 + V_{nr}^2 + V_{nc}^2}$$

$$= \sqrt{0.231^2 + 0.349^2 + 7.40^2 + 69.0^2 + 45.4^2 + 6.93^2}$$

$$= 83.22\mu V$$

Comparing each of the noise voltages over each region, the overall output noise voltage is dominated by the thermal noise of R_f and the out of frequency of interest bandwidth noise voltage of the op amp.

The signal to noise ratio relative to R_f is $\sqrt{R_f}$, so as R_f increases the output increases, the thermal noise increases but at a much reduced rate.

The noise of the op amp in region 4 can be reduced by increasing C_f, but this reduces the bandwidth of the application, and C_f will normally have been chosen to meet the application's requirements. A better way of reducing this high frequency noise is to reduce the op amp's high frequency gain by reducing the value of C_{sh}. This can be done by applying a negative voltage across the diode. The effect of this is to raise the frequency of f_1 whilst lowering the high frequency gain of the op amp.

In the application shown the common mode range of the TLC2201 is being exploited in a single rail circuit making the application of a negative voltage across the diode impossible.

Another point to note is that the speed of this application is limited by C_f and not the op amp, if a faster application was required the trans-impedance gain would need to be reduced, but this would also reduce the signal to noise ratio of the application.

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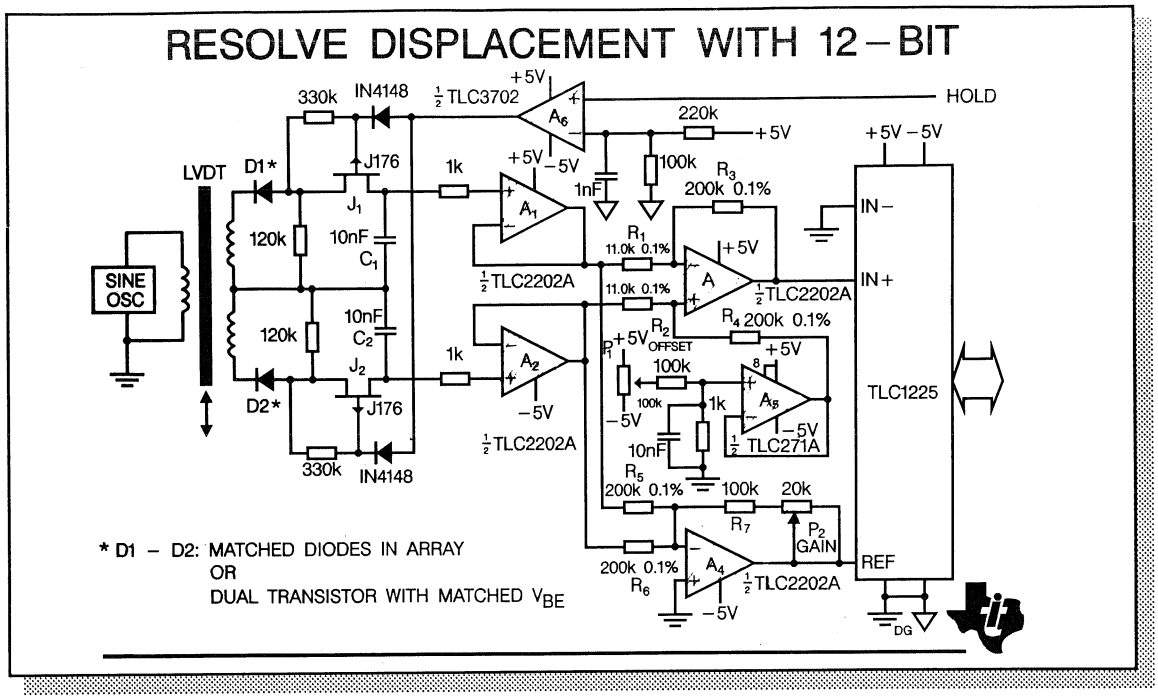


Figure 25 - Resolve Displacement with 12 Bit

Measure Position with an LVDT

The field of robotics represents an almost limitless arena for high resolution position sensing in mechanical systems. For that purpose, a transducer - the Linear Variable Differential Transformer (LVDT) is often employed. When combined with precision conditioning TLC2202 op amp circuitry and a 12-bit plus sign TLC1225 a/d converter, high resolution measurements of displacement are possible from ±5V supplies.

An LVDT is a transformer with a mechanical moveable core. The primary is driven by a sine wave, usually amplitude stabilised. Sine drive eliminates error inducing harmonics in the transformer. The two secondaries are connected in opposed phase. When the core is positioned in the magnetic centre of the transformer, the secondary outputs cancel and there is no output. Moving the core away from the centre position unbalances the flux ratio between the secondaries, developing an output.

Signal conditioning circuits for LVDT outputs involve rectification and smoothing to convert the AC signal into a DC signal proportional to position. Rectification circuits vary from simple half wave rectifiers to complex synchronous demodulators. After filtering or smoothing, the DC signal can then be simply digitized by an a/d converter.

Application Circuit Features

The LVDT in this application has its centre between the two secondaries grounded. The amplitudes of the secondary coils' output signals are directly proportional to the core position

and are also each other's complement. As the core moves, one output rises while the other falls. Despite using simple detector diodes, D_1 and D_2, to rectify the AC signals from the transducer, the circuit obtains many high performance features.

The application incorporates a sample and hold circuit that keep the detectors output stationary during a conversion. The rectified signal is sampled on the hold capacitors, C_1 and C_2, and held constant while the a/d conversion takes place. Low leakage JFET switches, J_1 and J_2, in addition to CMOS inputs on the TLC2202 op amps, A_1 and A_2, prevent discharging and give a low droop rate. The differential, rectified and held LVDT output is then amplified by a differential amplifier, formed by the TLC2202 CMOS op amps, A_1, A_2 and A_3.

Summing the outputs of the two secondaries by A_4, and using this signal as the converter's reference has two very definite advantages. It helps eliminate any need for precision stabilization of the oscillator's amplitude. It also obviates compensating for temperature dependent gain changes in the transformer. Using this approach ensures that such common mode signals have no effect on the digitized output of the a/d converter.

Why Use the TLC2202 Advanced LinCMOS Op Amp?

The TLC2202 is an ideal op amp for precision applications operating from low supply voltages and requiring rail-to-rail output swing. Particularly for A_1 and A_2 in this application:

- A very low input bias current is essential to prevent discharging of the hold capacitors C_1 and C_2. TLC2202's CMOS inputs ensure a maximum input bias current of 100pA over temperature.

- A common mode input range and output swing close to the negative supply are required. TLC2202 fully support these needs and has even a common mode input range to the negative rail.

- The input offset voltage must be low and stable enough to allow reliable trimming of the system offset to 12 bits accuracy. The 500μV maximum offset of the TLC2202 is just acceptable.

Notes

- As a high common mode voltage is present on the inputs of A_1 and A_2, a good common mode rejection is necessary to prevent excess offset and offset drift. The minimum 85 dB over temperature adds little additional offset error and insignificant offset drift over common mode voltage variations.

Particularly for A_3 and A_4 in this application:

- Low input offset and rail-to-rail output swing. TLC2202's outputs swing very close to both supply rails provided that it is not loaded heavily.

Design Details

Transducer

The chosen component design assumes a LVDT with a maximum differential linear output voltage of ±250mV peak. The outputs of the two secondaries are assumed to be centred around 4V peak, which make up the common mode voltage. This leaves some room for variations in the sine wave amplitude due to oscillator drift and transformer transfer ratio changes with temperature, which the circuit compensates for as previously described.

Rectifier plus Sample and Hold Circuit

It is essential that the two rectifier diodes D_1 and D_2 have identical voltage drops and that their drops track with temperature. Two matched diodes in an array should be used. Alternatively, a double transistor with precision matched V_{BE} characteristics could be used as rectifying diodes by connecting the base and collector of each transistor. Be aware that reverse bias protection diodes in some double transistors prevent this use. A rectification resulting in a negative output voltage was chosen as the common mode range of the succeeding TLC2202 op amps have a wider negative than positive common mode range.

P-channel JFET switches J_1 and J_2 were chosen to allow switching with the available ±5V supplies (the source signals can be close to -5V, so n-channel JFETs would require a minimum turn-off voltage of $V_{GS(OFF)}$ - 5V, corresponding to -8 to -10V for most devices). The 330kΩ gate-source resistors keep the gate-source voltages equal to zero volts in the switches on-state condition. In off-state, the gates are brought close to +5V by the switch control comparator, A6, which interfaces directly to logic signals. It is possible to control p-channel JFETs directly from logic levels but the used TLC3702 LinCMOS comparator provides better isolation from digital glitch noise.

The values of C_1 and C_2 were chosen to provide a low droop rate during the hold period, where leakage from the inputs of A_1 and A_2 plus the JFETs discharge the capacitors. The droop rate, dV/dt, can be calculated from:

$$\frac{dV}{dt} = \frac{I_{leakage}}{C}.$$

Differential Amplifier

A standard instrumentation three op amp configuration is used for the differential amplifier. The purpose of the first two amplifiers, A_1 and A_2, is to buffer the voltages hold on C_1 and C_2. The third amplifier, A_3, acts as a differential amplifier providing the common mode suppression. The gain setting resistors, R_1, R_2, R_3 and R_4, used, must be well matched to achieve good common mode rejection - preferably better than 0.1%, to give more than 60dB rejection. The gain has been accommodated to give full scale for a ±250mV peak transducer signal. To remove transducer offset plus op amp offsets an adjustment is included. A single TLC271A LinCMOS op amp, A5, buffers the potential divider circuit around P_1. Stability of this adjustment rely on supply rail drift tracking within 1%.

Reference Amplifier

The sum of the two secondary outputs is used to generate a ratiometric reference voltage. Op amp A_4 sums the two signals through R_5 and R_6. Precision tracking of these resistors is required to ensure a reference input voltage, REF, whose level depends only on the sum of the two secondary voltages. The potentiometer, P2, sets the full scale range, which of course most be equal to or higher than the IN+ voltage to the a/d converter. Any changes in the sine oscillators amplitude, transformer transfer ratio over temperature or other common mode errors are cancelled with this arrangement. The voltage levels set at the IN+ and REF pins should allow for some room for such common mode drift.

A/D Converter

TLC1225 is a self-calibrating 12-bit plus sign bipolar or 12-bit unipolar a/d converter with 10µs conversion time. In unipolar configuration, only a single +5V supply is required. Bipolar mode, as used in this application, needs however dual supply rails but provides a ±5V input range. The differential input voltage is converted ratiometric to the reference input and converted to a parallel word, which interfaces directly to a 16-bit data bus.

Software controlled self-calibration allows calibration of the a/d converter at power up, before every conversion cycle or whenever appropriate. This feature ensures long term stability, preventing frequent re-calibration of the application and avoid expensive initial trimming at the factory.

Notes

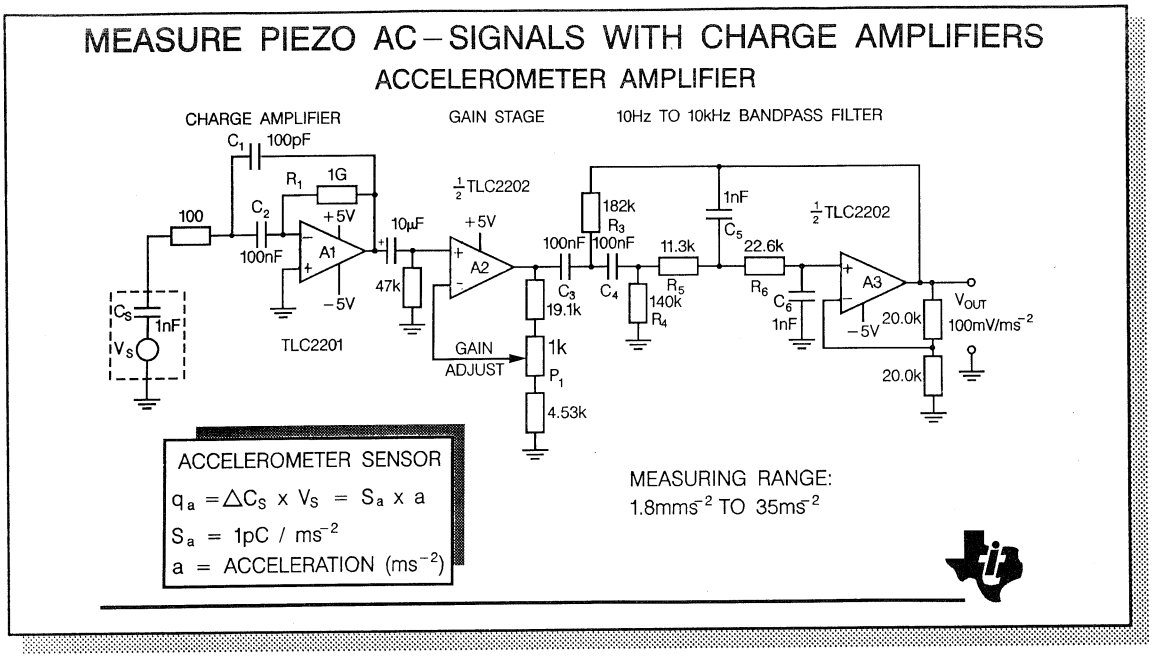


Figure 26 - Measure Piezo AC - Signals with Charge Amplifiers

Piezo Transducer Interfaces

When interfacing op amps to piezo transduces, two basic modes are employed; Voltage mode or Charge mode. Both principles require an op amp with very high input impedance and low bias current, which limits the choice to JFET or CMOS input op amps. The dynamic range of such interfaces to piezo transducers that exhibits AC signals, is usually limited by the noise produced by the op amp. The TLC2201 and TLC2202 are Advanced LinCMOS op amps that challenge the input noise of the very best JFET input op amps and are simultaneously capable of operation from low supply voltages.

Voltage mode operation requires that the op amp is placed very close to the sensor as parasitic load capacitance on the sensor output will change its sensitivity. A cable between the sensor and the op amp will not only attenuate the sensor's output - but variations in the cable capacitance due to mechanical influence easily modulates the desired signal. When voltage mode configuration is used, the amplifier is usually incapsulated together with the sensor such as in electric microphones.

Charge mode operation is widely used, primarily because the influence from any shunt capacitance across the sensor is eliminated. Consequently, the length of a connected cable will not influence the sensitivity but affect only the maximum bandwidth of the measuring system.

Accelerometer Application

The illustrated application converts an acceleration input, a, measured by a piezo electric acceleration sensor and conditioned by an accelerometer amplifier, to an output voltage, V_{out}, proportional with the sensed acceleration. The circuit provides a wide dynamic range thanks to the very low input noise and rail-to-rail output swing of the Advanced LinCMOS op amps, TLC2201 and TLC2202 used. Additionally, the entire circuit operates from ±5V supplies, ensuring overall low power consumption.

The accelerometer amplifier consist of three sections, a charge amplifier that converts the sensor output charge to a voltage, a gain stage and a 10Hz to 10KHz bandpass filter, which limit the amplifier's noise bandwidth.

If an accelerometer sensor with a sensitivity of $1pC/ms^{-2}$ is employed, a maximum full scale rms acceleration of $35ms^{-2}$, or approximately 36g can be measured. The lowest acceleration that can be detected is determined by the charge amplifier's noise. Assuming typical system noise with a minimum of 5dB S/N ratio, vibration or acceleration levels down to $1.7mms^{-2}$ corresponding to 0.17mg are theoretical measurable.

Sensor

The equivalent electrical model of a piezo electric acceleration sensor can be thought of as a voltage source, V_S, in series with a small sensor capacitor, C_S. Variations in capacitance due to physical deformation will cause charge, q_a, to be dumped into the charge amplifiers summing junction. Characteristic parameters for such a sensor are the sensitivity, S_a, and the sensor capacitance, C_S.Their relationship to the produced charge, q_a, is given by:

$$q_a = \Delta C_S * V_S = S_a * a \; ; \quad \text{where a = acceleration ;}$$

The sensor (B&K type 4384) used in this application has the following typical parameter values: $S_a = 1pC/ms^{-2}$ and $C_S = 1nF$.

Notes

Charge Amplifier

The purpose of the charge amplifier is to transform the high output impedance of the acceleration sensor and amplify its relatively weak signal. A basic charge amplifier consist of a high gain operational amplifier with a feedback capacitor. When charge is dumped into the amplifier's summing junction from the sensor, the amplifier manipulate its output voltage to maintain the charge in the feedback capacitor equal to the charge dumped into the input, so that the voltage in the summing junction tends to be at null. For the actual application, A_1 is acting as charge amplifier and C_1 is the feedback capacitor. Ignoring the effect from R_1, C_2 and the 100Ω input resistor, the transfer function from acceleration input to A_1's output voltage, E_{o1} becomes:

$$E_{o1} = -\frac{q_a}{C_1} = -\frac{S_a}{C_1} * a \quad <=> \quad \frac{E_{o1}}{a} = -\frac{S_a}{C_1}; \quad (1)$$

By insertion of actual component and parameter values, (1) becomes:

$$\frac{E_{o1}}{a} = -\frac{1pC/ms^{-2}}{100pF} = -10mV/ms^{-2}; \quad (2)$$

If higher vibration or acceleration levels than 36g have to be measured, C_1 can be increased to reduce the gain of the charge amplifier.

A large feedback resistor, R_1, provides a leakage path for A_1's input bias current and prevents the op amp's output from being driven into saturation. As R_1 together with C_1 forms a highpass filter with a 3dB frequency, $f_o = 1/(2\pi R_1C_1) = 1.59Hz$; the value of R_1 needs to be vary large if low frequencies are of interest. The exceptional large value of 1GΩ is chosen because the effect of its thermal noise decreases as R_1 increases. This is discussed in the noise evaluation section. An upper limit of R_1 is given by the offset produced when A_1's input bias current passes through it. With TLC2201's 100pA maximum input bias current over temperature, a worst case offset of (1GΩ * 100pA) = 100mV is generated. However, as the maximum signal output from A_1 is only 500mV peak, no limitations on the op amp's output swing follows. To prevent swing limitations on the succeeding gain stage, the charge amplifier's output is AC coupled.

To avoid A_1's input bias current from contributing to the charging of C_1, a DC blocking capacitor C_2 is placed between the very high impedance AC summing junction and the op amp's inverting input terminal. The effect of C_2 on the transfer function can be ignored with the value chosen. A 100Ω resistor in series with the charge amplifier's input provides some protection, when the sensor is disconnected. A lowpass filter is formed together with C_1 but at frequencies beyond interest. Thermal noise from 100Ω will not affect the overall accelerometer amplifier's noise performance.

Charge amplifiers very high input impedance require carefully layout, PCB cleaning and guarding. The summing junction would benefit from teflon stands. Both capacitors should be of a low leakage type such as polypropylene, polystyrene or teflon.

Gain Stage

A simple non-inverting gain stage is implemented by one half of a low noise TLC2202 op amp to boost the charge amplifier's output voltage five fold. Additionally, the gain stage around A_2 allow for ±10% gain adjustment with P_1 to accommodate variations in the sensitivity of the sensor. The gain should be adjusted to yield an overall accelerometer amplifier output voltage, V_{out}, of $100mV/ms^{-2}$. Thermal noise from the potential voltage divider, does not contribute to the total system noise.

TLC2202's output stage features near rail-to-rail output swing with the load impedance provided.

Filter

Following the gain stage is a 10Hz to 10kHz bandpass filter, implemented around the second half of TLC2202. The purpose of this filter is to remove low frequency excess noise and limit the upper noise bandwidth. In fact, the bandpass filter consists of a combined 2nd order 10Hz highpass and 2nd order 10kHz lowpass filters with Butterworth characteristics. Design of this filter section assumes no mutual interaction between the two filter sections. This is only possible because the cut off frequencies are so far apart and that an impedance level has be chosen to minimise interaction.

Design details of the filter are trivial and only covered briefly. Assumptions: $\omega_{oHP} = 1/(2\pi * 10Hz)$, $\omega_{oLP} = 1/(2\pi * 10KHz)$, a midband gain of two and a 2nd order maximum flat or Butterworth Q factor, $Q = 1/\sqrt{2}$. The transfer function, H(s), can then be shown to be given by:

$$H(s) = \frac{s^2}{s^2 + \left(\frac{1}{R_4C_3} + \frac{1}{R_4C_4} - \frac{1}{R_3C_3}\right)s + \frac{1}{R_3R_4C_3C_4}} * \frac{\frac{1}{R_5R_6C_5C_6}}{s^2 + \left(\frac{1}{R_5C_5} + \frac{1}{R_6C_5} - \frac{1}{R_6C_6}\right)s + \frac{1}{R_5R_6C_5C_6}}; \quad (3)$$

Notes

$$H(s) = \frac{s^2}{s^2 + \frac{\omega_{oHP}}{Q} s + \omega_{oHP}^2} * \frac{\omega_{oLP}^2}{s^2 + \frac{\omega_{oLP}}{Q} s + \omega_{oLP}^2} \quad ; \quad (4)$$

Comparing (3) and (4) yield the following design equations and component values:

Highpass: Choose $C_3 = C_4 = C = 100nF$;

$$R_3 = \frac{\frac{1}{Q} + \sqrt{\frac{1}{Q^2} + 8}}{4\omega_{oHP} C} = 182.1k\Omega \cong 182k\Omega \text{ (E96 value)} ;$$

$$R_4 = \frac{4}{\omega_{oHP} C} \frac{1}{\sqrt{\frac{1}{Q^2} + 8 + \frac{1}{Q}}} = 139.1k\Omega \cong 140k\Omega \text{ (E96 value)} ;$$

Lowpass: Choose $C_5 = C_6 = C = 1nF$;

$$R_6 = \frac{1}{Q\, \omega_{oLP} C} = 22.51k\Omega \cong 22.6k\Omega \text{ (E96 value)}$$

$$R_5 = \frac{1}{R_6 C^2 \omega_{oLP}^2} = 11.25k\Omega \cong 11.3k\Omega \text{ (E96 value)} ;$$

Why use Advanced LinCMOS TLC2201 and TLC2202 Op Amps?

The charge amplifier requires a CMOS or JFET input op amp with very low input voltage and noise current. In addition, the input bias current should be as low as possible to avoid excess offset that limits the dynamic range.

For the gain stage and filter section, a relatively low voltage and current input noise is still required. But more important is the low distortion rail-to-rail output swing providing output voltage levels, that easily interface to a connected sample & hold plus a/d converter circuitry.

If these essential needs are added to the demand for low cost, low power and low supply operation (±5V), the TLC2201 and TLC2202 are about the only op amps available meeting these requirements.

Noise Considerations

If a multi-stage amplifier is constructed such, that the input noise of the first stage multiplied with its gain is larger that the input noise of the succeeding stage etc, the first stage will

dominate the noise of the total multi-stage amplifier. Following this principle, the charge amplifier's gain has been chosen to produce an output noise, E_n, significantly higher than the input noise of the gain stage. Consequently, the noise evaluation is focussed on the noise produced by the charge amplifier in the bandwidth limited by the filter section. Wideband noise generated by A_3, (which is only limited by its falling open loop gain), is low and can be ignored.

Three sources dominates the output noise from the charge amplifier:

- **e_n**, input noise voltage density from A_1, TLC2201; (e_n = 8nV/$\sqrt{Hz}$ typical)
- **I_n**, input noise current density from A_1, TLC2201 ; (i_n = 0.6fA/$\sqrt{Hz}$)
- **R_1**, thermal noise density generated by R_1 (1GΩ), and equal to $\sqrt{4kTR_1}$;

Where k = 1.38 * 10^{-23}J/K (Boltzmann's constant; and T = 298K (absolute temperature @ 25°C).

Assuming that the charge amplifier's input is shorted by the sensor's characteristic capacitance, C_S, and that C_2 and the 100Ω input resistor does not influence the noise, the charge amplifiers output noise density, $E_n(s)$, is given by:

$$E_n^2(s) = \left(1 + \frac{R_1 \parallel \frac{1}{C_1 s}}{\frac{1}{C_S s}} \right)^2 * \left(e_n^2 + i_n^2 \left(R_1 \parallel \frac{1}{C_1 s} \parallel \frac{1}{C_S s} \right)^2 + 4kTR_1 \left(\frac{\frac{1}{C_1 s} \parallel \frac{1}{C_S s}}{R_1 + \frac{1}{C_1 s} \parallel \frac{1}{C_S s}} \right)^2 \right) ;$$

$$E_n^2(s) = e_n^2 \left(\frac{R_1(C_1 + C_S)\, s + 1}{R_1 C_1 s + 1} \right)^2 + i_n^2 R_1^2 \left(\frac{1}{R_1 C_1 s + 1} \right)^2 + 4kT\, R_1 \left(\frac{1}{R_1 C_1 s + 1} \right)^2$$

Notes

The total rms noise measured on the charge amplifiers output can now be calculated from:

$$E_n(rms) = \sqrt{\int_{-oo}^{+oo} |E_n(j2\pi f)|^2 d(f)} \; ; \qquad s = j\omega = j2\pi f$$

To simplify this task, we will analyse the three components of $E_n^2(s)$, and determine which dominate in the frequency band of interest.

$$E_n^2(s) = E_{e_n}^2(s) + E_{i_n}^2(s) + E_{R_1}^2(s) \; ; \qquad s = j\omega = j2\pi f \quad =>$$

$$|E_n(j2\pi f)|^2 = |E_{e_n}(j2\pi f)|^2 + |E_{i_n}(j2\pi f)|^2 + |E_{R_1}(j2\pi f)|^2 \; ;$$

e_n generated noise: $E_{e_n}(s) = e_n \left(\frac{R_1(C_1 + C_S)\, s + 1}{R_1 C_1\, s + 1} \right) \; ;$

$$|E_{e_n}(j2\pi f)| = e_n \sqrt{\frac{1 + \left(\frac{f}{f_{zero}}\right)^2}{1 + \left(\frac{f}{f_{pole}}\right)^2}} \; ;$$

Zero frequency: $f_{zero} = \frac{1}{2\pi R_1 (C_1 + C_S)} = 0.14Hz$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59Hz$

Noise; $f << f_{zero}$: $e_n = 8nV/\sqrt{Hz}$ (typical)

Noise; $f >> f_{pole}$: $e_n \left(1 + \frac{C_S}{C_1}\right) = 88nV/\sqrt{Hz}$ (typical)

i_n generated noise: $E_{e_i}(s) = i_n R_1 \left(\frac{1}{R_1 C_1\, s + 1} \right) \; ;$

$$|E_{e_i}(j2\pi f)| = i_n R_1 \sqrt{\frac{1}{1 + \left(\frac{f}{f_{pole}}\right)^2}} \; ;$$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59\text{Hz}$

Noise; $f << f_{pole}$: $i_n R_1 = 600\text{nV}/\sqrt{\text{Hz}}$ (typical)

R_1 generated noise: $E_{R_1}(s) = \sqrt{4kT R_1}\left(\frac{1}{R_1 C_1 s + 1}\right)$;

$$|E_{R_1}(j2\pi f)| = \sqrt{4kT R_1}\sqrt{\frac{1}{1 + \left(\frac{f}{f_{pole}}\right)^2}};$$

Pole frequency: $f_{pole} = \frac{1}{2\pi R_1 C_1} = 1.59\text{Hz};$

Noise; $f << f_{pole}$: $\sqrt{4kTR_1} = 4.1\mu\text{V}/\sqrt{\text{Hz}};$

Clearly, the current and thermal generated noise dominates at very low frequencies. The amplitude of the current generated noise, $|E_{in}(j2\pi f)|$, is reduced by -20dB/decade above f_{pole}. Consequently, it has shrunken to the same level as the amplitude of the voltage generated noise, $|E_{en}(j2\pi f)|$, at:

$$\frac{i_n R_1}{e_n \frac{C_1 + C_S}{C_1}} \frac{1}{2\pi R_1 C_1} = \frac{i_n}{2\pi e_n (C_1 + C_S)} = \frac{600\text{nV}}{88\text{nV}} * 1.59\text{Hz} = 10.8\text{Hz};$$

Current generated noise has therefore no effect on the total noise in the 10Hz to 10KHz frequency band at 25°C. Note that the 10.8Hz frequency remains constant with changes in R_1.

Notes

Similarly, the amplitude of the thermal generated noise, $|E_{R1}(j2\pi f)|$, equals the amplitude of the voltage generated noise, $|E_{en}(j2\pi f)|$, at:

$$\frac{\sqrt{4kTR_1}}{e_n \frac{C_1 + C_S}{C_1}} \frac{1}{2\pi R_1 C_1} = \sqrt{\frac{4kT}{R_1}} \frac{1}{2\pi e_n (C_1 + C_S)} = \frac{4.1\mu V}{88nV} * 1.59Hz = 74Hz ;$$

Consequently, thermal generated noise as well as current generated noise has little or insignificant effect on the total noise in the 10Hz to 10kHz frequency band. Note that the 74Hz frequency decreases proportionally with increasing value of $\sqrt{R_1}$. The interesting point about R_1 is, that the current generated noise in the frequency range considered is unaffected and that a higher value reduces the thermal noise!

The conducted noise analysis clearly shows, that the charge amplifier's output noise density in the frequency range of interest is totally dominated by the noise voltage, $|E_{en}(j2\pi f)|$, generated by the TLC2201 op amp's input noise voltage, e_n. Calculating the total rms noise, $|E_n(rms)|$, on the output of the charge amplifier now becomes a simple task, as $|E_{en}(j2\pi f)|$ is constant from 10Hz to 10kHz. Integration of the noise density over the frequency band of interest can now be accomplished with a simple multiplication, yielding:

$$|E_n(rms)| = \sqrt{|E'_{en}(j2\pi f)|^2 * \text{Noise Bandwidth}} ;$$

Where $|E'_{en}(j2\pi f)|$ is equal to $|E_{en}(j2\pi f)|$ for $10Hz < f < 10kHz$. Inserting numbers gives:

$$|E_n(rms)| = \sqrt{|88nV/\sqrt{Hz}|^2 * (10kHz - 10Hz) * 1.11} = 9.27\mu V \text{ rms};$$

Re-arranging the transfer function (1) for the charge amplifier can now be used to determine the corresponding input accelerations, a_n:

$$a_n = \frac{E_n(rms)}{S_a} C_1 = \frac{9.27\mu V}{1pC/ms^{-2}} 100pF = 0.927mms^{-2} ;$$

Assuming a minimum 5dB S/N ratio, the typical lowest theoretical acceleration, a_{min} that can be measured is given by:

$$a_{min} = a_n * 10^{\frac{(S/N)dB}{20}} = 0.927mms^{-2} * 10^{\frac{5dB}{20}} = 1.65mms^{-2} \cong 0.17mg \text{ acceleration} ;$$

However, these figures are reduced somewhat if a worst case calculation is performed. The major additional noise comes from:

- Worst case TLC2201A noise voltage is 50% higher and equal to $12nV/\sqrt{Hz}$, which raises the flat noise floor.
- Worst case TLC2201 noise current over temperature is much higher than the typical 0.6fA @ 25°C, as it tends to double for every 10°C temperature increase. This temperature dependent effect results in an increasing low frequency noise with increasing temperature.
- Thermal noise from the feedback resistor increases with the square root of the temperature again adding to the low frequency noise.
- Noise sources from the succeeding gain op amp and filter contribute slightly to the total noise with the component values and gain chosen.

Notes

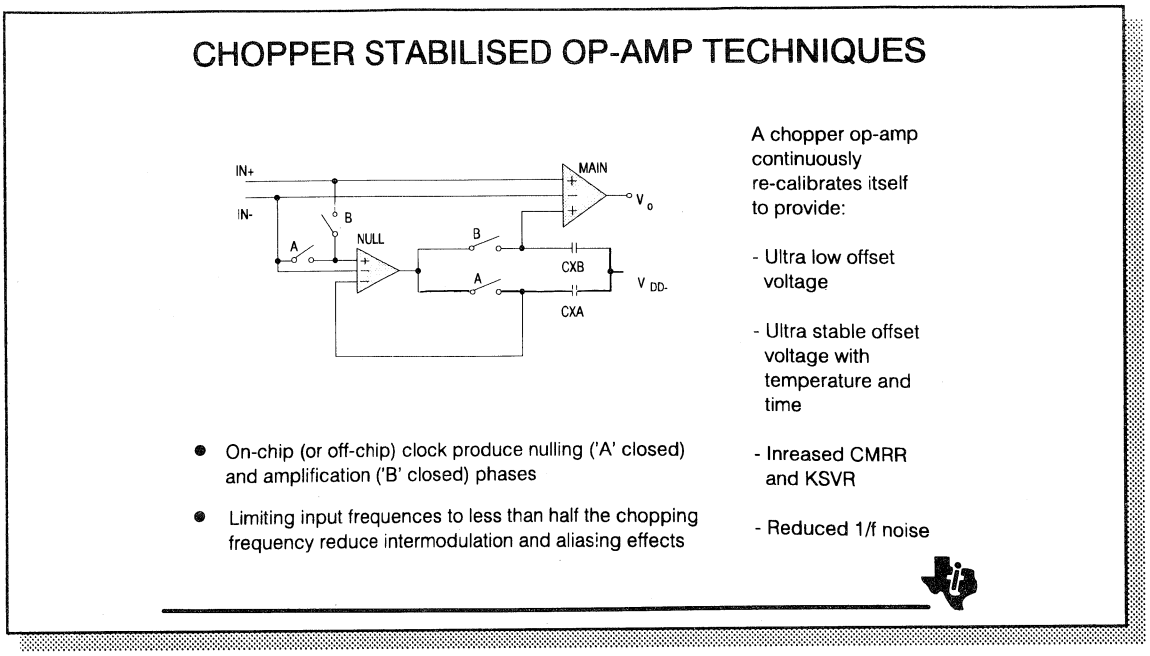


Figure 27 - TLC2652 Chopper Stabilised op Amps

Chopper stabilised operational amplifiers have been available for many years but when they were first released there was much resistance, by design engineers, to using them. It was felt they were too noisy as an op amp and also generated too much extra noise within a circuit. Recently however, engineers have started to appreciate the outstanding levels of performance that can be achieved by using a 'chopper'. It was realised that the so called noise problems were not such a real issue and that the performance and relative low cost of newer products was just too good to miss!

The ideal precision op amp would require; ultra low offset voltages with negligible drift, bias and offset currents as low as those achieved by FET input amplifiers plus open loop gains, PSRR and CMRR would be high and noise would have to be at a minimum. Chopper stabilised op amps *very nearly* achieve the required level of performance to be the ideal precision amplifiers! If bandwidth is limited to reduce noise errors, then the precision of a circuit is determined more by external components and parameters (board layout, temperature gradients etc) than the op amp itself.

Newer designs in particular are getting closer still to the ideal. The latest choppers released by TI are the **TLC2652/A and TLC2654/A** - both are **world leaders.**

The **TLC2652**, shown above, is a chopper stabilised op amp optimised for precision. The 'A' selection part has a **maximum offset voltage of just 1µV** and maximum drift specifications of **30nV/°C and 20nV/month**. Short and long term errors due to offset voltage are rarely a problem! The device is also CMOS so its bias currents are low causing minimal errors due to currents flowing in external resistors. A further benefit of chopper design techniques (see

Figure 26) , is that they also benefit from extremely high gains, Avd is 135dB, and both the Power Supply and Common Mode Rejection Ratios are 120dB. The device easily meets the requirements of an 18bit system.

If there is a limitation to choppers then it occurs in three areas: Noise voltage is typically high (although 1/f noise is practically removed) in most designs (see TLC2654, Figure 29, for something new!) and so care must be taken to limit the circuits bandwidth of operation. It should be noted however that with very low bandwidths, <0.25Hz, the noise from a chopper is often less than the noise of a bipolar op amp (this is because of their almost zero 1/f frequency). Secondly, because the devices are fabricated using CMOS technology then supply voltages are most commonly limited to +/- 8V. Thirdly, they are often just too good! Errors are typically introduced due to external factors (see Figure 32), and these must be carefully considered when depending upon the precision available from these parts.

If you are looking for a device that achieves outstanding levels of precision the TLC2652A should be seriously considered.

Notes

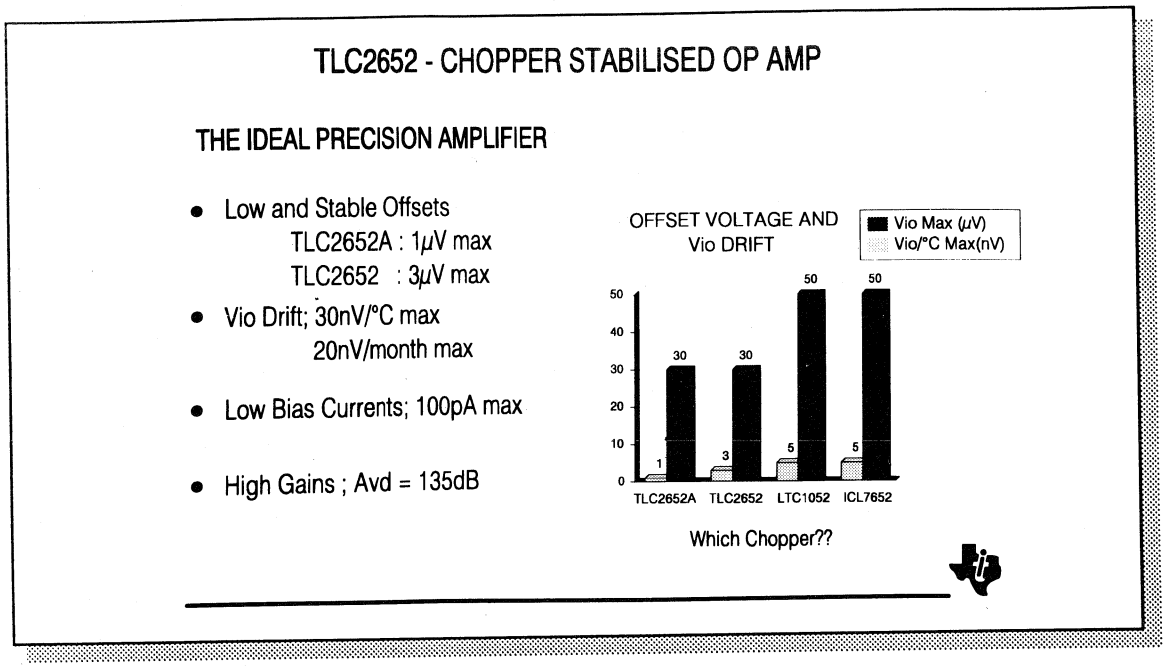


Figure 28 - Chopper Stabilised Op Amp Techniques

Chopper stabilised op amps offer the best DC precision of any op amp. This superior performance is the result of using two op amps - a main amplifier and a nulling amplifier - and also an oscillator, switches and two external or internal capacitors to create a system that behaves as a single amplifier. With this approach, the TLC2652 op amp achieves sub-microvolt input offset voltage, nanovolt input noise voltage, and offset variations with temperature in the nV/° C range.

The on-chip control logic produces two dominant clock phases; a nulling phase and an amplifying phase. During the nulling phase, switches "A" are closed, shorting the nulling amplifier inputs together and allowing the nulling amplifier to reduce its own input offset voltage by feeding its output signal back to an inverting input node. Simultaneously, external capacitor CXA stores the nulling potential to allow the offset voltage of the amplifier to remain nulled during the amplifying phase.

During the amplifying phase, switches "B" are closed, connecting the output of the nulling amplifier to a non-inverting input of the main amplifier. In this configuration, the input offset voltage of the main amplifier is nulled. Also, external capacitor CXB stores the nulling potential to allow the offset of the main amplifier to remain nulled during the next phase.

This continuous chopping process allows offset voltage nulling during variations in time and temperature and over the common mode input voltage range and power supply range. In addition, because the low frequency signal path is through both the null and main amplifiers, extremely high gain is achieved.

The low frequency noise of the chopper depends on the magnitude of the component noise prior to chopping and the capability of the circuit to reduce this noise while chopping. The low frequency noise is reduced by increased chopping frequency. Intermodulation from input frequencies above the chopping frequency cause errors 60-80dB below full scale.

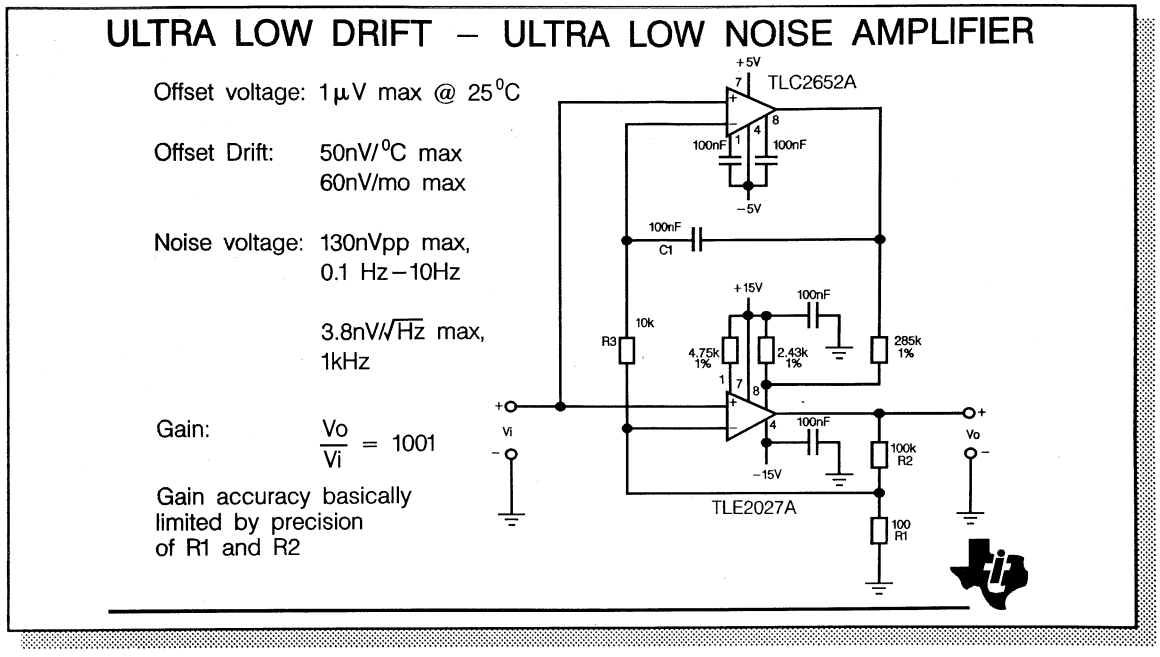


Figure 29 - Ultra Low Drift - Ultra Low Noise Amplifier

Applications requiring extremely high DC precision combined with low noise can benefit from this composite amplifier.

The TLC2652A measures the DC error at the TLE2027A's input terminals and biases its offset pins to force the offset to within 1μV. Similarly, the combined amplifier's offset drift with time and temperature is determined by the TLC2652A. The offset biasing at the TLE2027A is arranged such that the TLC2652A will always be able to find the servo point.

Notes

A 10kΩ value for R3 minimise the error caused by TLC2652A's input bias current and its drift. The 100nF capacitor, C1, rolls off the TLC2652A at low frequencies ensuring that any AC signals do not affect the offset cancellation. The TLE2027A handles all AC frequency signals.

The noise of the composite amplifier is determined by the TLE2027A. Keeping R1 as low as 100Ω reduces its thermal noise and eliminates the affect of input bias noise current from the TLE2027A.

If the amplifier is used for high frequency applications, an additional RC filter network at the non-inverting input of the TLC2652A would prevent high frequency common mode signals from unbalancing its input stage, which could then cause changes in the offset voltage.

The settling time of the composite amplifier is affected by the DC correction loop and can limit its applications for some high frequency circuits.

TLC2654 - LOW NOISE CHOPPER OP AMP

By Increasing the Chopping Frequency to 10kHz, Noise for the TLC2654 has been Significantly Reduced.

Increased Usable Bandwidth

Reduced Intermodulation Effects

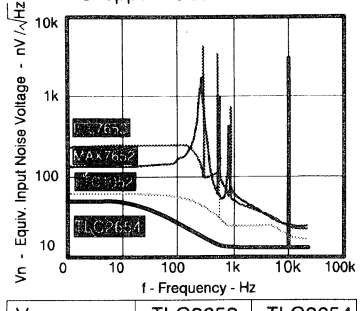
Precision Maintained:

Vio..... TLC2654A = 10μV max
TLC2654 = 20μV max

Vio Drift... 0.3μV/°C max
0.02μV/month max

(Still 4 years for 1μV of Vio Drift!!)

Chopper Noise Performance



Vnpp	TLC2652	TLC2654
DC to 1Hz	0.8	0.5
DC to 10Hz	2.8	1.5

Figure 30 - TLC2654- Low Noise Chopper Op Amp

Previous figures have discussed the limitations placed upon chopper stabilised amplifiers due to their relatively high noise voltage - at low frequencies the noise voltage of a typical chopper may be 100nV/√Hz, significantly higher than most amplifiers. In practice this means that the circuit bandwidth needs to be limited to ensure that dc errors are dominated by the offset voltage of the amplifier and not by the noise of the op amp. When using the TLC2652A with an offset voltage of 1μV the circuit bandwidth needs to be limited to 1Hz.

Realising that this can cause problems in some applications TI has put significant effort into developing a chopper with much lower noise - the TLC2654 was the result. By increasing the chopping frequency from 450Hz (for TLC2652) to 10kHz it was possible to reduce the total noise of the amplifier by a half. This has been tried in the past but has always proved unsuccessful due to the resulting large increase in offset voltage and drift. Patented techniques used in the TLC2654 however enabled offsets voltages to stay at a minimum - 10μV is the maximum for the TLC2654A. Drift is also low at 0.05μV/°C and 0.06μV/month. It is not surprising that the TLC2654 won the "Product of the Year" Award from the US magazine Electronics.

In practice, choppers are often used as much for their low drift as for their absolute offset. By using the TLC2654 precision can be maintained and the usable bandwidth of the device can be increased. In practice this means that precision measurement applications, like weigh scales, can be designed with much improved response times.

Notes

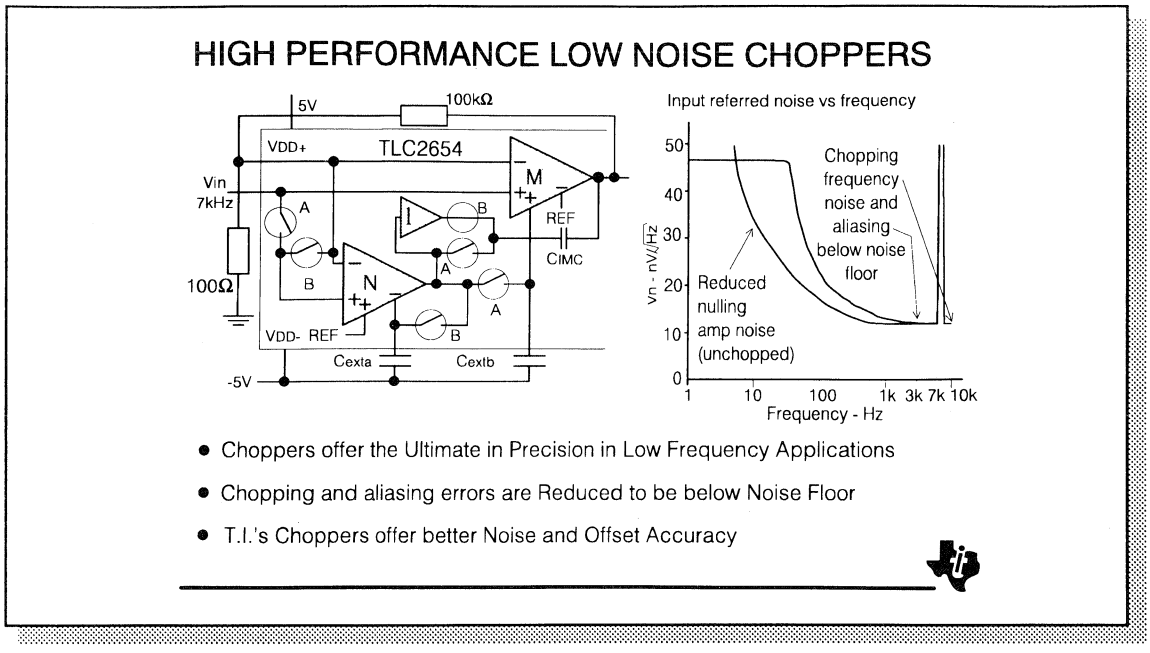


Figure 31 - High Performance Low Noise Choppers

Chopper op amps such as the **TLC2652** and **TLC2654** offer the very highest precision in terms of offset voltages and drifts. In addition to this they also offer very low noise spectral densities at frequencies below 1Hz.

The low offset voltage and drift is attained by continually measuring the offset of the main and nulling amplifier and using this to cancel out the offset voltages. This is done by a form of sampling, which can add noise to the system in a number of ways, and it this noise has limited the acceptance to choppers. This figure discusses the relative effects of the noise introduced by chopper op amps, and how they may be able to improve system performance.

Flicker Noise reduction

A chopper op amp sees its offset voltage and input noise voltage as very similar errors, which enables it to remove both the offset voltage and the low frequency noise voltage. At very low frequencies the noise voltage is dominated by flicker noise (having a 1/f characteristic), and it is this noise that the chopper sees as an offset, and is able to remove producing a flat spectrum. It should be noted, however, that the level of the noise at 50Hz has an amplitude higher than low noise op amps, but because of the removal of flicker noise at frequencies below 1Hz the noise level is in fact below most of the lowest noise op amps.

At very low frequencies, combination of the very small low frequency noise and the very low offset couple together to produce the highest accuracy solutions to high precision D.C. applications.

By continually nulling out the offset voltage of the op amp, noise produced from internal references are rectified and averaged out to produce a systematic offset which the chopper cannot null out. Texas Instruments' choppers use a special technique where the references' noise are not rectified and this reduces not only the systematic offset but also the wideband noise, shown on the figure. This reduced wideband noise enables Texas Instruments' choppers to reach noise levels that were previously unattainable by integrated circuit choppers. Another advantage of the techniques used within Texas Instruments' choppers is that because the systematic offset voltage has been reduced, they are able to chop at much higher frequencies, giving much lower noise voltages. Choppers in the past were limited to chopping frequencies below 500Hz. This is easily shown in the diagram above, chopping at 10kHz creates noise levels below $50nV/\sqrt{Hz}$, whereas chopping at 450Hz

Sampling and discrete time effects

As stated earlier, choppers are in effect sampling devices and this results in their spectra containing harmonics of the chopping frequency. The amplitude of these harmonics are normally in the nanovolt region, as shown in the spectrum analysis, and so normally the energy contained in them can be neglected.

Another cause of concern related to choppers is ***inter-modulation distortion***. During the chopping procedure the device is sampling and this can cause folding back of high frequency signals down to lower frequency signals. This is normally known as aliasing and can add errors into the frequency range of interest, thus reducing the dynamic range of the op amp. With the TLC2652 and TLC2654 any aliased signals will normally be attenuated to the order of the noise floor. This effect is also shown on the spectrum analyser plot. This is just one form of inter-modulation distortion and as all active devices are non-linear some inter-modulation distortion will be created. At best this distortion will be harmonics of the input signals, but poor performance devices can cause summation and subtraction of these harmonics. The latter effect is much more important in high end audio systems.

The chopper induced intermodulation distortion effects are removed by a special `intermodulation compensation network'. All choppers employ a form of "intermodulation compensation network", and its basic function is to reduce the a.c. gain of the nulling amplifier during the amplifying phase. Without this network aliasing between the input signal and the chopping frequency would occur.

Notes

During the amplifying phase an intermodulation compensation capacitor, C_{IMC}, is connected from the output of the nulling amplifier to the output of the main amplifier, so reducing the gain of the path through the nulling amplifier. During the nulling phase C_{IMC} is removed from the nulling amplifier's output and connected to another voltage source. This isolates the nulling amplifier from the main amplifier's output. When C_{IMC} is switched back, the change in voltage across it introduces charge and creates transients onto the main amplifier's input. C_{extb} integrates this injected charge, increasing the offset of the whole op amp. As the chopping frequency increases, minimising aliasing, more charge is injected increasing the offset created.

To reduce this problem, Texas Instruments has implemented a technique which minimises the voltage change across C_{IMC}. Driving C_{IMC}, during the nulling phase, with a buffered signal from the nulling amplifier reduces the change in voltage. This minimises any change in charge across C_{IMC} when it is switched back. Hence Texas Instruments' choppers have lower offset voltages and are capable of chopping at higher frequencies which produces less low frequency noise and also gives the added benefit of being able to operate with a wider range of input signal frequencies.

The curve shown above not only demonstrates the very low noise voltage characteristics but also demonstrates the effectiveness of the intermodulation compensation network. The aliased signal developed from a 7kHz sine wave is below the noise floor (at 3kHz equal to $12nV/\sqrt{Hz}$) of the chopper. The curve also shows the very large rejection of the chopping frequency; at 10kHz the spectral content is less than the noise floor of $12nV/\sqrt{Hz}$, which is again below the noise level of most choppers.

It is these characteristics that allow the choppers to be used in yet more applications where they were once considered to be too noisy.

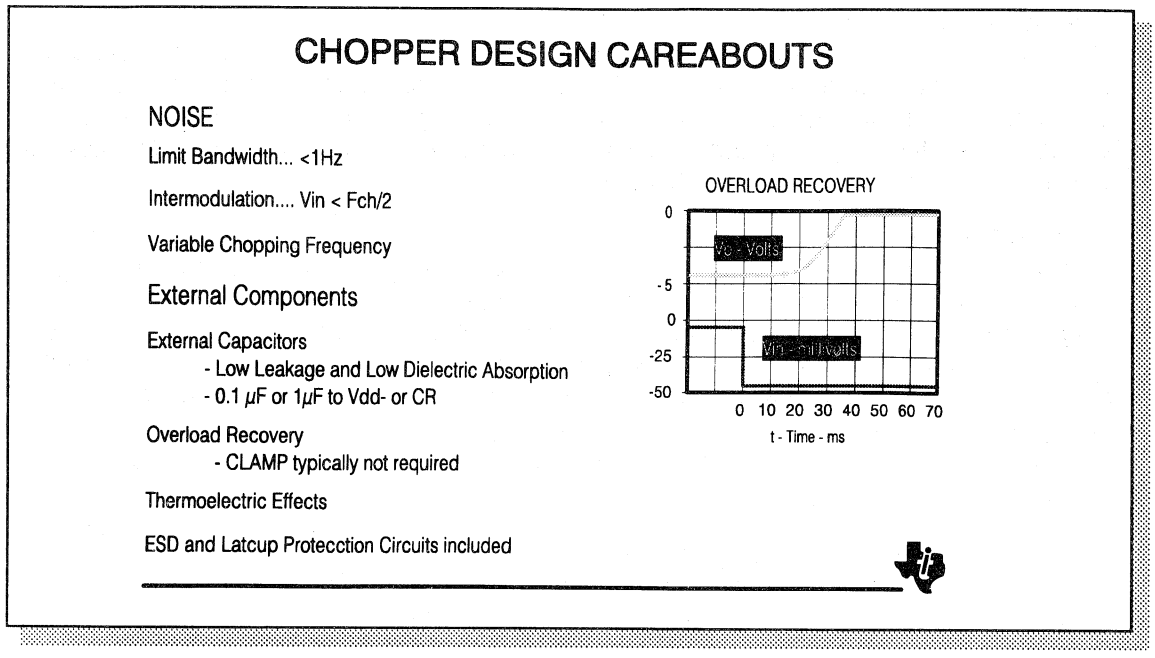


Figure 32 - Chopper Design Careabouts

When an application requires the absolute best performance from the chopper stabilised op amp, a number of factors and design considerations should be considered.

Noise

Noise has been discussed in detail in figure 29, but the key points to remember are;

Limit Bandwidth:
The bandwidth of the op amp should be limited to reduce DC errors associated with the relatively high noise voltage of the amplifier. Take advantage of the device's low 1/f frequency however, as over very small frequencies (<1Hz), the choppers noise are less than many bipolar op amps!

Notes

Intermodulation effects:
If an input signal has a frequency component equal to greater than half the chopping frequency then intermodulation errors may be caused. In practice, chopper design techniques have minimised these errors (<70dB down on input signal) but it may be necessary, depending upon the frequency and magnitude of input signal, to filter out these components using an extra filter stage before the chopper.

Chopping Frequency:
The standard selection chopper op amps are available in an 8 pin package and have a predetermined internal clock frequency which defines the noise performance and offset voltage of the op amps. There are however, options available in a 14 pin package which have the capability of changing the clock frequency by the use of an external clock. This external clock signal can be fed directly into the CLK IN input and the INT/EXT pin is attached to V_{DD-}. When operated in a single supply configuration the device can be driven directly by TTL or CMOS logic without the need for extra level shifting. Although not critical, the duty cycle of the external clock should be kept between 30% and 60%.

The advantages of being able to modify the clock frequency of these choppers are essentially two fold. Firstly the noise and offset of the op amp can be optimised for your particular circuit and secondly the clock frequency can be matched to other clock signals present within your circuit.

External Components

Choosing and using the Right Capacitors:
The external capacitors, C_{XA} and C_{XB}, should be carefully chosen to ensure best operation of the amplifier. Specifically, special attention should be given to the leakage and dielectric absorption of these components.

Degradation from capacitor leakage becomes more apparent with increasing temperatures. Low-leakage capacitors and standoffs are recommended for operation at T_A = 125°C. In addition, guardbands are recommended around the capacitor connections on both sides of the printed board to alleviate problems caused by surface leakage on circuit boards. Very thorough cleaning of the circuit board using alcohol or similar cleaning fluids is also recommended and errors can be further reduced by guarding the inputs of the amplifier with a ring connected to a low impedance node, normally ground.

Capacitors with high dielectric absorption tend to take several seconds to settle upon application of power, which directly affects input offset voltage. In applications where fast settling of input offset is needed, it is recommended that high quality film capacitors, such as mylar, polystyrene. or polypropylene, be used. in other applications, however, a ceramic or other low-grade capacitor may suffice.

The TLC2652 and TLC2654 have been designed to function with values of C_{XA} and C_{XB} in the range of 0.1µF to 1µF without degradation to input offset voltage or input noise voltage. These capacitors should be located as closely as possible to the C_{XA} and C_{XB} pins and returned to either the V_{DD-} pin or the C RETURN pin. Note that in many choppers, connecting these capacitors to the V_{DD-} pin will degrade the noise performance. This problem has been eliminated with these designs.

Overload Recovery Time/Output Clamp:
When large differential input voltage conditions are applied to the TLC2652 and TLC2654 choppers, the nulling loop will attempt to prevent the output from saturating by driving C_{XA} and C_{XB} to internally-clamped voltage levels. Once the overdrive condition is removed, a period of time is required to allow the built-up charge to dissipate. This time period is defined as overload recovery time. Typical recovery times are significantly faster for the TLC2652 and TLC2654 when compared to competitive products; however, if required, this time can be reduced further by using internal circuitry accessible through the clamp pin.
This Clamp circuit stops the output circuit from going into saturation due to a reduction in the closed-loop gain of the device (activated when the output is with 1V of each rail). The CLAMP pin is simply connected to the inverting input of the op amp, and it may however cause a slight degradation in the maximum output swing.

Thermoelectric effects:
To take advantage of the extremely low offset voltage drift of any chopper op amp, care must be taken to compensate for the thermoelectric effects present when two dissimilar metals are brought into contact with each other (such as device leads being soldered to a printed circuit board). Dissimilar metal junctions can produce thermoelectric voltages in the range of several microvolts per degree Celsius, which are orders of magnitude greater than the 0.003 μV/°C typical drift of the TLC2652).

To help minimise thermoelectric effects, careful attention should be paid to component selection and circuit board layout. Avoid the use of nonsoldered connections (such as sockets, relays, switches etc) in the input signal path. Cancel thermoelectric affects by duplicating the number of components and junctions in each device input. The use of low-thermoelectric-coefficient components, such as wire wound resistors, is also beneficial. It is also recommended to try and minimise excessive power dissipation and temperature gradients across a circuit board. Large power dissipating devices should be kept well away from precision components and air movement should ideally be kept at a minimum.

Electrostatic Discharge and Latchup avoidance:
Both these topics are discussed in detail in figure 14, but points to note are;
ESD - Care must be taken when using these devices, but both the TLC2652 and TLC2654 have been designed to withstand ESD voltages up to 2000V without causing functional damage.
Latchup - Both products have been designed to withstand 100 mA surge currents without sustaining latchup.
For more details on both see figure 14.

Notes

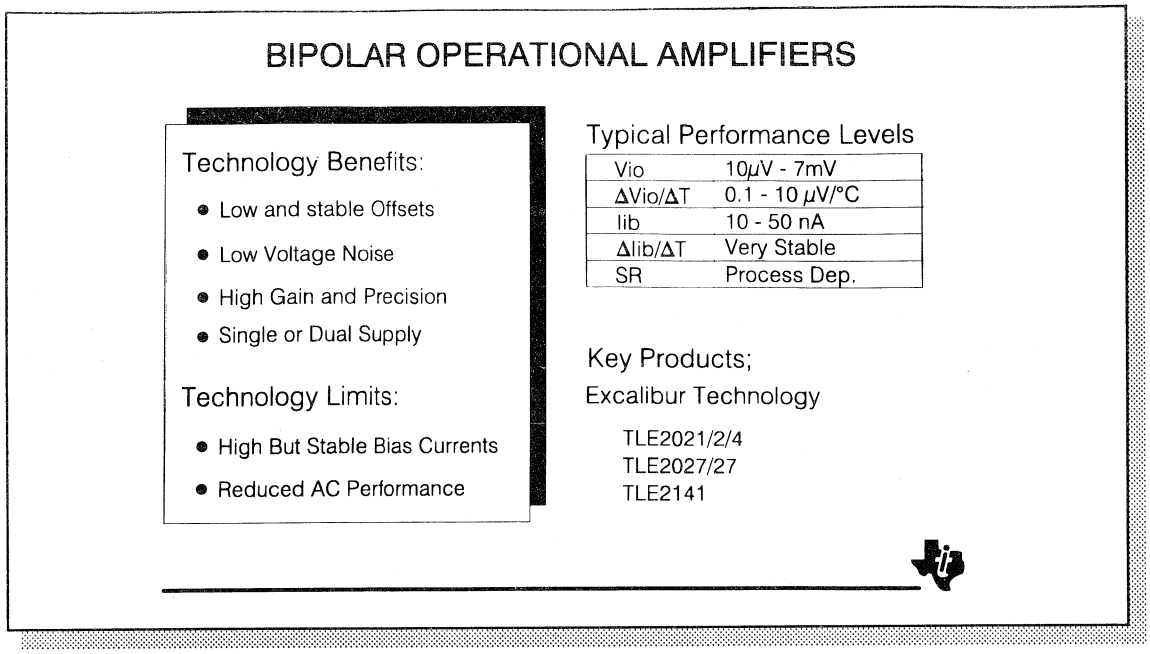


Figure 33 - Bipolar Operational Amplifiers

Bipolar is still by far the most popular technology used to develop operational amplifiers, and new, higher performance bipolar technologies are being developed continuously - the μa741 would not recognise the technologies being used today!

Devices designed using bipolar technology have a number of benefits over Bifet or CMOS products.

Bipolar Advantages

Low and stable offsets;
Because bipolar transistors are relatively easy to match and their behaviour due to temperature and current change is well understood, it is possible to develop operational amplifiers with low and stable offsets. Offset voltage errors are due to Vbe mismatches in the input transistors and the different currents flowing through the collectors of the input stage transistors. By using various trimming techniques, bipolar designs are now available with offset voltages as low as 10μV which drift less than 0.1μV/°C.

Low Noise;
A low noise voltage rather than low noise current specification is of most importance in the majority of applications (eg audio, telecom and many instrumentation systems). Bipolar op amps offer the lowest noise voltage performance among commercially available devices. The noise voltage from the input of a bipolar amplifier is dominated by the thermal noise from the base spread resistance and the emitter small signal resistance. Both of these, and other factors, can be optimised to achieve op amps with $<2nV/\sqrt{Hz}$ noise voltage specification, this

performance is impossible to achieve using a FET input amplifier. When interfacing to high impedance sources however, bipolar op amps become inferior to CMOS designs. Their high noise current specifications dominate noise errors.

High Gain;
The transconductance, gm, of the bipolar input stage is high and therefore the related open loop gain of the amplifier is also high. The benefit is the ability to design circuits which are much more 'accurate' than Bifet or CMOS designs. This high gain however does mean that an complicated compensation networks need to be used to ensure stability, a factor which lower gain JFETs have benefited from to achieve higher slew rates.

Bipolar Disadvantages

High Offset and Bias Currents;
Because of the bipolar input stage the bias currents of bipolar op amps is high (effectively it is the base current flowing into the input transistors). Various design techniques such as SuperBeta NPNs, or bias current cancellation circuits can be used to reduced these currents but it would be very unusual that, at room temperature, a bipolar device could compete with a FET design.

Bias currents for bipolar designs are however much more stable than for FET input designs. At high temperatures it is possible for a FET input device to actually have higher bias currents than a good bipolar design, particularly a super beta part.

Slow Lateral PNPs;
Lateral PNPs are much slower (and noisier) than the NPNs available from the same process. A typical technology would have PNPs with an FT (transistor bandwidth) of 3MHz, compared to NPNs which have an FT of 150MHz. As it is very difficult to design a device without using PNPs, the overall AC performance of an amplifier is severely limited.

Realising this many manufacturers have developed 'Complementary Bipolar Technologies' which have much faster PNPs who's FTs are similar to the NPNs. The result has been much faster bipolar op amps.

Excalibur is TI's new complementary bipolar process, but as well as having faster PNPs it includes a number of other features necessary for the development of performance amplifiers. This technology is discussed in detail in the next Figure.

Notes

TI's COMMON BIPOLAR OP AMPs

TLE2021	LM301	LT1001	OP07
TLE2022	LM307	LT1007	OP27
TLE2024	LM308	LT1007	OP37
TLE2027	LM311	LT1008	RC4156
TLE2037	LM324	LT1012	RC4138
TLE2141	LM339	LT1013	RC4558
	LM348	LT1014	RC4559
	LM358	LT1028	
	LM393	LT1037	
	LM2902	NE5532	
	LM2904	NE5534	

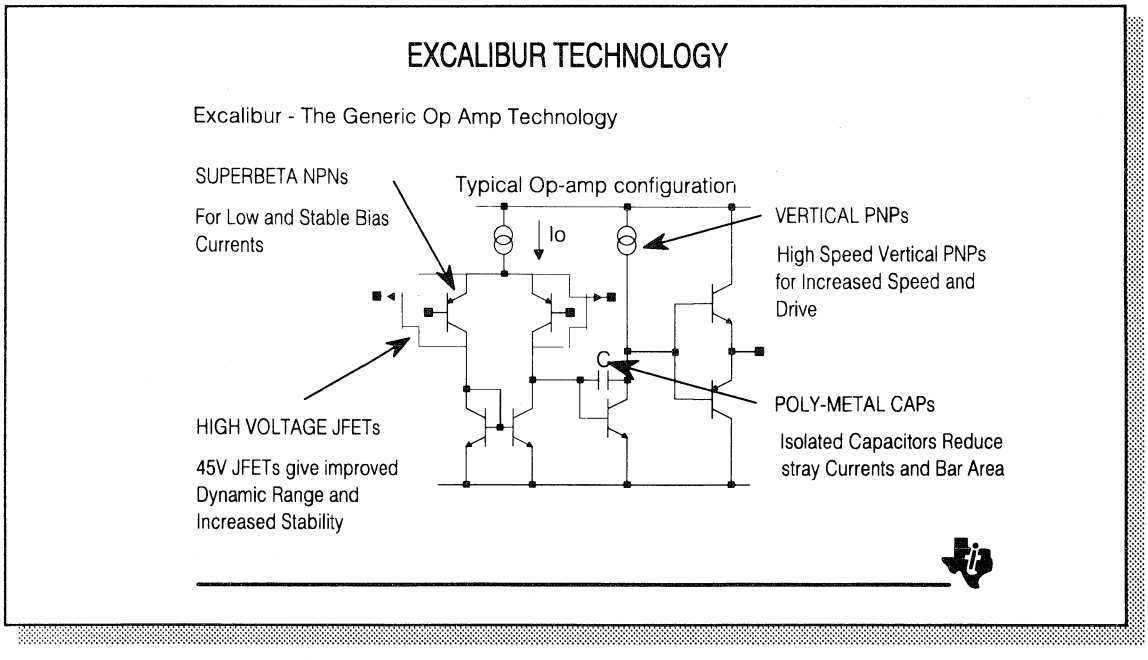


Figure 34 - Excalibur Technology!

TI has recently started releasing products designed using its new Excalibur technology - today 4 families are available with significantly more are under development. Everyone of these designs benefits from the significant features and process enhancements made available by Excalibur - a Complementary bipolar/Bifet technology optimised for the design of cost effective operational amplifiers.

Before developing Excalibur, TI analysed the latest system requirements for new operational amplifiers and the technology limitations which have restricted the desired levels of performance being achieved. Not surprisingly, the diverse range of applications meant a number of different process enhancements were identified, the ideal technology would therefore need to provide a range of improvements.

TI decided that the ideal solution would be to produce a technology which featured a number of different building blocks - developing a Complementary Process alone was not enough. A further, and important, benefit of a process that offers a wide range of different structures is that very different amplifiers can be developed by using only slightly different mask levels. Increased volumes would therefore enable more cost effective products!

The main areas of development and improvement are discussed below:

1) High Speed Vertical PNPs

It is difficult to develop an operational amplifier without employing PNP transistors (they are most commonly used in an amplifiers differential input stage or as current mirrors) and as a typical lateral PNP is 50 times slower than their equivalent NPNs, they have proved a severe limitation to the speed of an op amp.

Many companies have recognised this and have developed Complementary Bipolar technologies to improve the speed of PNPs and therefore the extend the AC performance of their op amps. By concentrating on improving the speed of both the NPNs and a new vertical PNP structure, Excalibur is significantly faster than previous processes. The NPN now has an FT(transistor bandwidth) of 450MHz, 3 times faster, and the PNP has an FT of 150MHz (50 times faster!). The result is that new op amps can be developed with much improved AC performance without any increase in supply current.

2) SuperBeta NPNs

A limitation of precision bipolar op amps is their relatively high bias currents and noise current specifications. A recognised technique of reducing these parameters is to use superbeta NPNs in the input stage of the amplifier. Excalibur's superbeta NPNs have an h_{fe} (transistor current gain) of 2000, 10 times higher than the standard structure. This enables a significant reduction in bias currents which because of bipolar's inherent current stability may at higher temperatures be lower than a FET input device.

3) JFET Transistors

Bifets will continue to be extremely popular op amp types and it was felt essential that Excalibur had the capability to produce performance Bifet amplifiers. A slight limitation to the JFETs used in todays op amps are their restricted supply voltage operating range. Most designs operate with maximum +/-18V supplies and therefore operation from higher supply voltages, such as the common +/-22V, is not possible. Excalibur JFETs were developed with breakdown voltages of 50V, enabling higher voltage Bifets to be processed. Applications now benefit from increased supply voltages and an improved common mode voltage range.

Notes

The offset voltage of Bifet op amps was also not forgotten. The lessons learnt from the development of the Enhanced TL05X and TL03X Bifet families have been introduced into Excalibur's structures. Offset voltages as low as 500μV, with high stability, are available from op amps supplied in a plastic package.

The TLE2061/2/4 family, discussed in Figures 9, 10, 11 and 12 were developed using Excalibur.

4) Isolated Capacitors

All compensated operational amplifiers use a minimum of one capacitor within a design. In many cases this capacitor takes up significant silicon area, and causes noise and switching problems by injecting spurious current into the substrate.

The capacitors used in Excalibur are made from a Polysilicon - Nitride - Metal layer and is isolated via Field Oxide, from the rest of the circuit. The result is a 4 times improvement in capacitance per unit area and a structure which does not disrupt other parts of the circuit. Improvements in both performance and cost are achieved.

The result

Not all these structures are used in every new design but having them all available as building blocks in the same process gives the IC designer a great deal of flexibility and choice in his circuit design. The end user benefits from performance amplifiers which, because they are made from a widely used process are truly cost competitive.

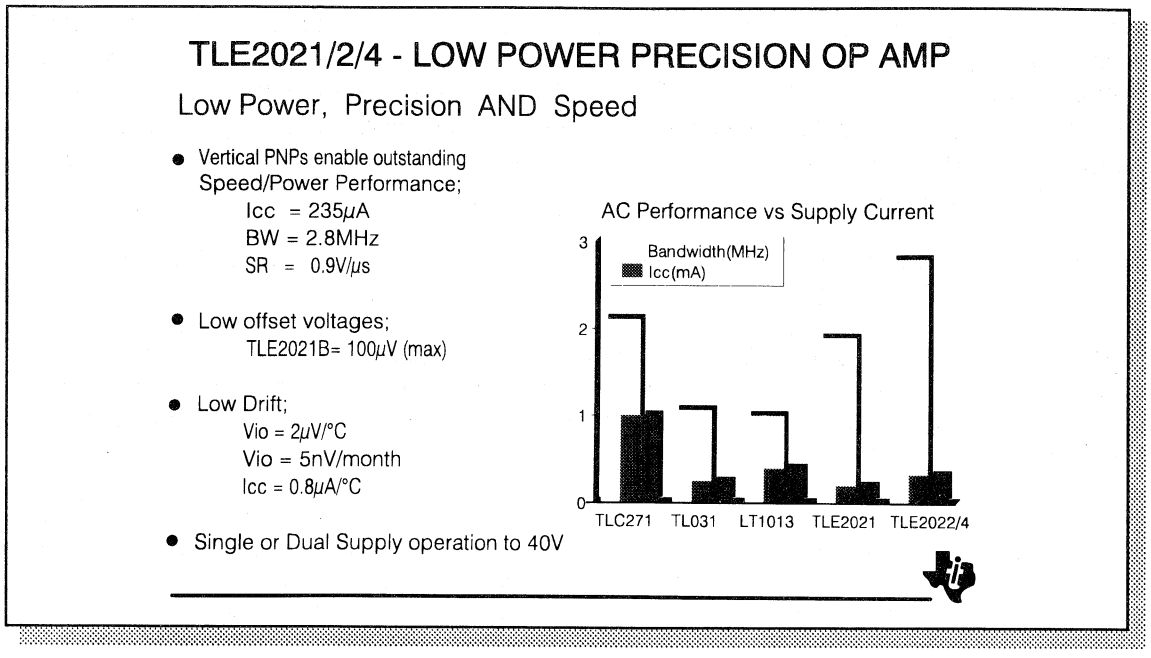


Figure 35- TLE2021 Low Power Precision Op Amp

The TLE2021, TLE2022 and TLE2024 were the first operational amplifiers to be processed using the Excalibur technology. These low power products were designed using the new high speed vertical PNPs available in Excalibur, and the result is a family of devices that offer significant AC performance with minimal supply currents.

Improved AC Performance - The graph above compares the Bandwidth and Supply current for a number of low power operational amplifiers. It immediately shows that all TLE2021/2/4 devices achieve much improved bandwidth without any increase in supply current. Performance in fact exceeds that of some Bifet and CMOS op amps.

Slew rate is also significantly improved (see figure 35) when compared to low power alternatives - typically 0.9V/μs from 235μA. The device is now a viable alternative to Bifet and CMOS designs which are often used for their improved AC performance.

Notes

Precision - What further makes this device stand out is its suitability for precision applications. The tightest selection has a maximum offset of just 100µV. This combined with a high Open Loop Gain (A_{vd} equals 120dB), and superior stability with time and temperature results in an amplifier ideal for low power instrumentation, test and measurement equipment. The op amps offsets will typically vary by 2µV/°C and 5nV/month - this equates to a V_{io} change of 1µV in 16 years!

The 'A' selection part has 200µV maximum offset voltage and the standard part has a Vio of 500µV.

Performance stability - In addition to low offset voltage drift, a patented bias circuit was designed using Excalibur's JFETs. The result is that the supply current varies typically by 0.08µV/°C (see Figure 35). In fact ALL temperature versions specify the same supply current spec at both 25°C and over the full range.

Supply current stability has a number of system benefits above its obvious advantage to low power circuits. Supply current impacts the performance of most op amp parameters, including gains, slew rate, bandwidth, offset voltage, bias currents and even the output drive capability. By maintaining a relatively constant supply current, the drift with temperature of these other specifications is also reduced. Well defined and constant system performance with temperature is very achievable.

Single or Dual Supply Operation - Using Excalibur's new PNPs, the devices have a common mode input range down to the negative supply (0V to 3.2V from 0V and 5V supplies) and so are the ideal choice for low level, single supply single conditioning applications. The absolute maximum voltage range is +/-20V, so applications with large supply voltages for increased dynamic range can also benefit.

Phase-Reversal Protection - All devices feature phase-reversal protection circuitry that eliminates unexpected change in output states when one of the inputs goes below the negative rail.

Applications - Low power systems will benefit the most from using the TLE2021 family of op amps. Several hand-held Telecom equipment gain a significant advantage from the combination of low power consumption and good AC performance, while portable test and measurement applications can take full advantage of the precision and stability of these designs. The parts have been used in magnetic sensors, process monitoring and control equipment, and also single supply instrumentation systems such as interfacing to a strain gauge.

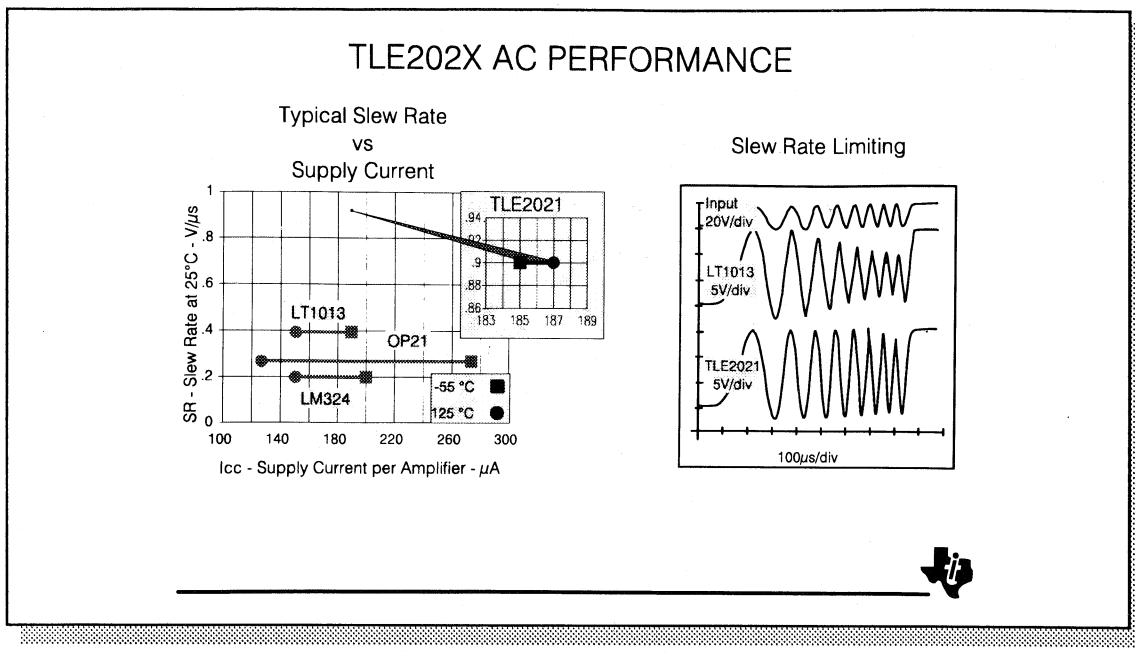


Figure 36 - TLE202X AC Performance

TLE2021 Slew Rate verses supply current.
It is unusual for low power bipolar operational amplifiers to achieve significant levels of AC performance, but by making use of Excalibur's high speed vertical PNPs, the TLE2021 family of precision op amps have achieved slewrates of up to 5-times higher than other low power bipolar designs. The graph above compares the AC performance of the TLE2021 against the LT1013, OP21 and the LM324

This graph also shows the supply current stability of these designs with temperature. By designing the current source using a patented circuit designed with Excalibur's JFETs, it has been possible to develop a part which has practically zero drift in supply current. Because supply current is a major factor in many other op amp parameters, this stability of Icc is also carried over to other specifications. The stability of everything from V_{IO} to slew rate is improved!

Notes

TLE2021 Improved AC performance

The second graph in this figure highlights how an improvement in slew rate can affect the actual signal clarity achievable from an op amp. A 20V pk-pk sine wave with a sweeped frequency is fed into a simple unity gain operational amplifier circuit. It can be seen that the LT1013 starts to slew rate limit at only 6kHz, causing signal degradation and a reduction in magnitude. The TLE2021 is still performing comfortably at 14kHz.

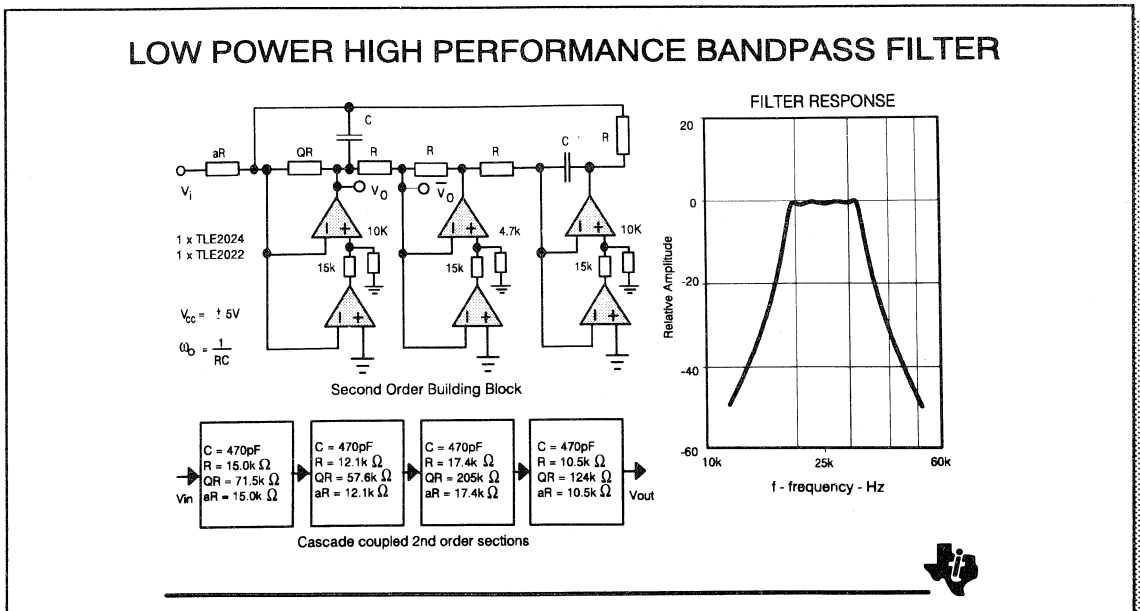


Figure 37 - Low Power High Performance Band-Pass Filter

High Q, High Frequency Filters

Designing active filters of high order requires high Q factors of each second order building block, usually cascade coupled, to achieve the overall wanted filter response. Simple second order building blocks constructed around a single standard 1MHz type op amp suffer from high Q sensitivity to passive components and op amp gain accuracy. If a Q of 10 has to be implemented the maximum frequency is normally restricted to below 1kHz. Some network topologies offer however little passive sensitivity but require more op amp open loop gain at the frequencies of interest. Multiple op amp second order filter building blocks are often the preferred solution for high Q high frequency filters as the Q sensitivity with respect to the individual op amps is reduced.

In resent years, active compensation of the op amp's first pole has been frequently described in articles. Such schemes allow standard 1MHz op amps to be used at frequencies up to a decade higher than with previous designs. However, the knowledge to the op amps exact dominant pole frequency is usually required in order to cancel its effect with a second op amp. Multiple monolithic op amps like duals or quads with their better matched frequency characteristics alleviate the problem to some extent and topologies compensating for both first and second effects in the op amps open loop frequency response exist too.

High Quality Bandpass Filter Building Block

Double integrator loop second order building blocks are most often used for high Q implementations. Circuit configurations exist offering simultaneously lowpass, highpass and bandpass outputs from the same three op amp structure. Adding a fourth op amp makes bandstop filter circuits possible.

The figure shows a high quality second order building block which has been designed for bandpass implementations only. Very desirable properties are available, such as both non-inverting and inverting outputs and a simple summing node option, allowing for use in active latter structures or leap-frog network applications.

Active compensation within the given double integrator loop occurs automatically without any critical matching requirements on the passive components, and without the need for matched op amps, which are in reality never obtainable. The pole frequency, $\omega_0 = 1/(RC)$ and the gain factor, $k = 1/a$, realised by the bandpass building block are both independent of the op amps gain-bandwidth products, so that the design equations become very simple, and gain-bandwidth product variations have no effect on the centre frequency of the overall filter. Convenient nominal values, R, C, QR and aR have been given for the passive components, but, neither the phase nor the magnitude compensation that occurs in the double integrator loop, is affected by deviations of the passive component values from the nominal suggested.

The transfer function can be derived as:

$$V_o = - V_i \frac{\frac{1}{Cs} \,||\, (QR)}{aR} - V_o \frac{1}{RCs} \frac{\frac{1}{Cs} \,||\, (QR)}{R} \qquad =>$$

$$\boxed{\frac{V_o}{V_i} = - \frac{1}{a} \frac{\frac{1}{RC} s}{s^2 + \frac{1}{RC} \frac{1}{Q} s + \frac{1}{R^2C^2}} = k \frac{\omega_0 s}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}} \quad ; \qquad (1)$$

The design equations become very simple:

$$\boxed{\text{Choose C;} \quad \text{Calculate} \quad R = \frac{1}{C\,\omega_0}; \quad RQ = \frac{Q}{C\,\omega_0}; \quad aR = \frac{1}{k\,C\,\omega_0}} \quad ; \qquad (2)$$

Notes

Higher Order Chebychev Bandpass Filter Design

A higher order bandpass filter can be realised by simply cascade coupling more second order sections using the building block just described.

When designing a Chebychev bandpass filter the following requirements determine the order, ripple, Q and ω_0 of the individual sections:

1. A Chebychev filter's normalised ($\omega_0 = 1$) lowpass frequency response, $|H(j\omega)|$ is given by:

$$|H(\omega)| = \frac{1}{\sqrt{1 + \varepsilon^2 \cosh^2 (n \cosh^{-1}\omega)}} ; \quad (3)$$

where $\omega = 2\pi f$, n = filter order and $\varepsilon^2 = 10^{\frac{\text{xdB filter ripple}}{10}} - 1$;

Once the acceptable pass-band filter ripple has been decided, and the required attenuation at $\omega = \omega_1$ (measured relative to the frequency, $\omega_H = 2\pi f_H$: which is the frequency where the amplitude versus frequency response leaves the ripple box) is given, the minimum low pass filter order can be calculated from (3) by solving the equation with respect to n:

$$n = \frac{\cosh^{-1}\left(\sqrt{\frac{|H(\omega_1/\omega_H)|^{-2} - 1}{\varepsilon^2}}\right)}{\cosh^{-1}(\omega_1/\omega_H)} ; \quad (4)$$

choose the normalised low-pass filter order as half the next whole even number greater than n.

2. The next step is to determine the bandpass filter's centre frequency, ω_{0BP} and bandwidth, B. Initially we consider the normalised bandpass filter with $\omega_{0BP} = 1$. A Chebychev filter's bandwidth is the difference in frequency between the highest frequency f_H where the amplitude versus frequency characteristic leaves the ripple box and f_L, the lowest frequency where the response leaves the ripple box. The normalised filter's bandwidth will be placed with logarithmic symmetry around the centre frequency of the filter, e.g.:

$$B = f_H - f_L = 10^X - 10^{-X} \Rightarrow 10^X = \frac{B}{2} + \frac{1}{2}\sqrt{B^2 + 4} ; \text{ where } f_H = 10^X \text{ and } f_L = 10^{-X} \quad (5)$$

3. Q_{LP} and ω_{0LP} for the individual filter stages of a n'th order normalised lowpass filter with the decided ripple is found in a standard filter table. These normalised ($\omega_0 = 1$) lowpass filter parameters are now transformed into normalised ($\omega_0 = 1$) bandpass filter parameters, Q_{BP} and ω_{0BP} by the following equations:

A first order low-pass section is converted into a second order bandpass section by:

$$Q_{BP} = \frac{\omega_o}{B\,\omega_{oLP}}; \qquad \omega_{oBP} = \frac{\omega_o}{2\,Q_{BP}}; \qquad (6)$$

A second order lowpass section is converted into a second order bandpass section by:

$$Q_{BP1} = Q_{BP2} = Q_{BP} = \frac{Q_{LP}}{\sqrt{2}} \sqrt{1 + \frac{4}{\delta^2} + \sqrt{(1 + \frac{4}{\delta^2})^2 - \frac{4}{\delta^2\,Q_{LP}^2}}}; \qquad (7)$$

$$\omega_{oBP1} = \frac{\omega_o}{2}\left[\delta\frac{Q_{BP}}{Q_{LP}} + \sqrt{(\delta\frac{Q_{BP}}{Q_{LP}})^2 - 4}\right]; \qquad (8)$$

$$\omega_{oBP2} = \frac{\omega_o}{2}\left[\delta\frac{Q_{BP}}{Q_{LP}} - \sqrt{(\delta\frac{Q_{BP}}{Q_{LP}})^2 - 4}\right]; \qquad (9)$$

Where $\delta = \frac{B}{\omega_o}\omega_{oLP}$; $\omega_o = \omega_{oBP1} * \omega_{oBP2} = 1$; (normalised bandpass filter).

4. Finally, relating the design to the actual described second order bandpass building block the component values can be determined from:

   Choose the value of the capacitors, C. Then calculate the resistors and include the de-normalising frequency transformation:

$$R = C * \omega_{oBP} * \omega'_o/\omega_o; \qquad (10)$$

   Where ω'_o is the de-normalised and total bandpass filter's centre frequency.

8th Order Chebychev Design Example

This section demonstrates a filter design example using the high performance second order building block and theory outlined in the previous sections.

Notes

We will construct a low power, bandpass filter with a centre frequency of 25kHz and a bandwidth of 12.5kHz. A maximum ripple of 0.5dB in the pass-band is acceptable and a minimum attenuation of 65dB below 10kHz and above 62.5kHz is required.

- Normalising the centre frequency of 25kHz to $\omega_0 = 1$ gives a normalised bandwidth, $B = 0.5$;

- From (3) : $\varepsilon^2 = 10^{0.05} - 1 = 0.122018$;

- From (5) : $f_H = 0.5/2 + 0.5\sqrt{0.5^2 + 4} = 1.2808$ and $f_L = 1/f_H = 0.7808$;

- Normalising the geometric symmetric frequencies, 10kHz and 25kHz gives 0.4 and 2.5 respectively. $\omega_1 = 2.5$ relative to f_H is then given by $\omega_1 / f_H = 2.5/1.2808 = 1.9519$;
  $|H(\omega_1/\omega_H)| = 10^{-65dB/20} = 0.5623 * 10^{-3}$;

- From (4) : $$n = \frac{\cosh^{-1}\sqrt{\frac{(0.5623 * 10^{-3})^{-2} - 1}{0.122018}}}{\cosh^{-1} 1.9519} = 7.16 ; \quad =>$$

  Normalised lowpass filter order = 8/2 = 4 => two second order sections;

- From a table of normalised lowpass Chebychev, 0.5 dB ripple filter parameters is found Q_{LP} and ω_{oLP} for a 4th order function:

Section	Q_{LP}	ω_{oLP}
A	0.705110	0.597002
B	2.940554	1.031270

- The two lowpass second order sections (A and B) transforms into four bandpass second order sections (1, 2, 3 and 4), for which we can now calculate the filter parameter values.

  From section A: $\delta_1 = \delta_2 = B\,\omega_{oLP} / \omega_0 = 0.5 * 0.597002 / 1 = 0.298501$;

  From (7): $Q_{BP1} = Q_{BP2} =$

$$\frac{0.705110}{\sqrt{2}}\sqrt{1 + \frac{4}{0.298501^2} + \sqrt{(1 + \frac{4}{0.298501^2})^2 - \frac{4}{0.298501^2 * 0.705110^2}}} ; \quad =>$$

$$Q_{BP1} = Q_{BP2} = 4.75072 ;$$

From (8): $$\omega_{oBP1} = \frac{1}{2}\left[0.29850\frac{4.75072}{0.705110} + \sqrt{(0.29850\frac{4.75072}{0.705110})^2 - 4}\right] ; \quad =>$$

$$\omega_{oBP1} = 1.11137 ;$$

From (8): $$\omega_{oBP2} = \frac{1}{2}\left(0.29850\,\frac{4.75072}{0.705110} - \sqrt{\left(0.29850\,\frac{4.75072}{0.705110}\right)^2 - 4}\right) ; \Rightarrow$$

$$\omega_{oBP2} = 0.899789 ;$$

From section B: $\delta_3 = \delta_4 = B\,\omega_{oLP} / \omega_o = 0.5 * 1.031270 / 1 = 0.515635 ;$

From (7): $Q_{BP3} = Q_{BP4} =$

$$\frac{2.940554}{\sqrt{2}}\sqrt{1 + \frac{4}{0.515635^2} + \sqrt{\left(1 + \frac{4}{0.515635^2}\right)^2 - \frac{4}{0.515635^2 * 2.940554^2}}} ; \Rightarrow$$

$$Q_{BP3} = Q_{BP4} = 11.7686 ;$$

From (8): $$\omega_{oBP3} = \frac{1}{2}\left(0.515635\,\frac{11.7686}{2.94055} + \sqrt{\left(0.515635\,\frac{11.7686}{2.94055}\right)^2 - 4}\right) ; \Rightarrow$$

$$\omega_{oBP3} = 1.28614 ;$$

From (8): $$\omega_{oBP4} = \frac{1}{2}\left(0.515635\,\frac{11.7686}{2.94055} - \sqrt{\left(0.515635\,\frac{11.7686}{2.94055}\right)^2 - 4}\right) ; \Rightarrow$$

$$\omega_{oBP4} = 0.777517 ;$$

Summarising the parameters of the normalised second order bandpass filter sections:

Section	**Q Bandpass**	ω_{oBP}
1	4.75072	1.11137
2	4.75072	0.899789
3	11.7686	1.28614
4	11.7686	0.777517

Notes

o The final component values can now be determined by chosing C = 470pF and using equation (2) and (10) to calculate the resistor values. $\omega'_o = 2\pi * 25kHz$, $\omega_o = 1$ and aR = R gives:

Section	C	R	QR	aR
1	470pF	Ideal: 15.05kΩ E96 std. value: 15.0kΩ	Ideal: 71.62kΩ E96 std. value: 71.5kΩ	Ideal: 15.05kΩ E96 std. value: 15.0kΩ
2	470pF	Ideal: 12.19kΩ E96 std. value: 12.1kΩ	Ideal: 57.90kΩ E96 std. value: 57.6kΩ	Ideal: 12.19kΩ E96 std. value: 12.1kΩ
3	470pF	Ideal: 17.42kΩ E96 std. value: 17.4kΩ	Ideal: 205.0kΩ E96 std. value: 205kΩ	Ideal: 17.42kΩ E96 std. value: 17.4kΩ
4	470pF	Ideal: 10.53kΩ E96 std. value: 10.5kΩ	Ideal: 123.9kΩ E96 std. value: 124kΩ	Ideal: 10.53kΩ E96 std. value: 10.53kΩ

Note: If unity gain is desired in the passband for the total filter, choose a = 1/Q => aR = R/Q.

Low Power Design Using The TLE2022 and TLE2024

By implementing the above design example using the Excalibur TLE2022 dual and TLE2024 quad op amps provide excellent AC performance for very little power consumption. Although the 8th order design example requires 8 * 6 = 48 op amps, the worst case total power consumption is only 12mA and 8.4mA typical. This is significant less compared to a realisation using four second order integrator filter blocks each implemented around three OP27 or LT1007 op amps adding up to a total of 24 op amps, consuming in worst case 96mA and 64 typical. In addition, the sensitivity to both passive and active elements would have been higher.

The TLE2022 and TLE2024's typical unity gain bandwidth of 2.8MHz for only 250μA supply current per op amp makes them ideal for low power filter designs - specially at low supply voltages. Operation is guaranteed and characterised down to ±2.5V. The only consideration for AC operation at high frequencies is their limited slewrate of 0.9V/μs. However, this is sufficient for operation to 35kHz with ±5V supplies and to 85kHz with ±2.5V supplies.

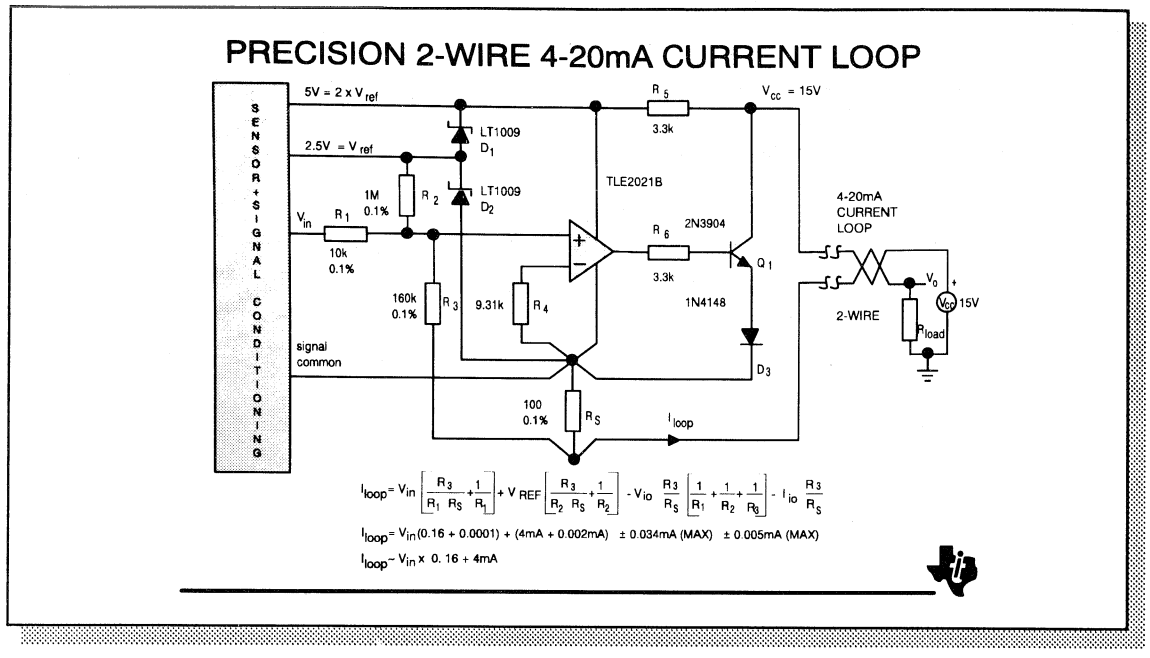


Figure 38 - Precision 2-Wire 4 to 20 mA Current Loop

What is a Current Loop?

Often information from an analog sensor must be sent over a distance to the receiving circuitry. For many applications, the most feasible method involves converting voltage information to a current before transmission. The most commonly used current loop interface standard consists of a minimum of two wires providing both the power supply for the sensor and signal conditioning circuit as well as transferring the information sensed in form of a current, which varies proportionally with the measured signal. The current in the loop varies usually from 4mA, corresponding to no signal, to 20mA for full scale - referring to the well known 4 to 20mA current loop. Up to 4mA of the loop current can be used for supplying the sensor, signal conditioning and voltage-to-current converter.

Notes

Precision 4 to 20mA Current Loop

The circuit presented provides a 4 to 20mA output current for a 0 to 100mV input voltage. By modifying R_1, R_2 and R_3 the input range or the output current can be adjusted. The total error is kept very low provided that the recommended precision components are used.

The employed Excalibur op amp, the TLE2021B, is a high performance op amp well suited for this type of application. The TLE2021B is here configured as a voltage-to-current converter, transmitting a very stable loop current, I_{loop}, proportional with the input voltage, V_{in}. The converter's transconductance or "gain" can be adjusted by R_1 and its current-offset varies with R_2. Resistor R_4 reduces the influence of the op amp's input bias current to that of its input offset current.

The loop current is divided up in three major paths: The primary current path is through transistor Q_1, whilst the secondary paths are via the reference and through the op amp. All current flowing through R_S is within the controlled and regulated 4 to 20mA current loop. The current flowing through R_3 is outside the loop control and contributes to the circuit's total error. This current can be taken into consideration in the design equations but with the chosen component values, its error becomes insignificant.

High system accuracy and stability is achieved without trimming by using two LT1009 voltage references in series producing a precision +5V reference. This implementation not only provides a stable 0.2% precision reference for the voltage-to-current converter but also ensures that picked up noise and hum from long loop wires are suppressed from the op amp supply by the reference element's low dynamic impedance. In addition, the reference and its +2.5V centre point are available for external signal conditioning circuitry, provided that a limited current is taken. The converter itself needs a minimum of 630µA (400µA for the reference and 230µA for the op amp), leaving (4 - 0.63)mA = 3.37mA to be used by additional circuitry. If really low power is required, the LT1009 voltage references should be replaced by LT1004s reducing the quiescent current consumption to basically that of the TLE2021B op amp or 240µA.

Why use the Excalibur TLE2021Op Amp?

- **Common Mode Input Voltage to Negative Supply Rail**
  By analysing the application it is seen that the input common mode voltage is zero volt.

- **+5V Single Supply Capability**
  This op amp feature eliminates the need for a third negative supply wire or a charge-pump creating a negative rail from the positive. Also, the low minimum operational voltage is utilized.

- **Output Swing Close to the Negative Rail**
  By analysing the circuitry it is seen that an output swing down to two V_{be} from the negative rail is required. Few dual supply op amps can actually swing that low.

- **Low Power Consumption**
  A total of 4mA is available for the converter and sensor interface. TLE2021 uses less than 230µA leaving more current for other parts of the circuit.

- **Low and Stable Input Offset Voltage**
  From the output current expression on the figure, it is clear that low input offset voltage is required. A 1mV offset voltage would contribute with a current error of 0.17mA. The TLE2021B with its maximum input offset voltage of 100µV (200µV max @ 5V supply) gives low error. Additionally, its offset voltage also remains stable with temperature and time featuring 2µV/°C and 5nV/month typical drift.

Design Details

Assuming that the voltage at the non-inverting input terminal of the TLE2021B is of zero volt relative to "Signal Common", and that $I_{Rs} = I_{loop}$, the sum of the currents at the non-inverting terminal gives:

$$\frac{V_{in}}{R_1} + \frac{V_{ref}}{R_2} - \frac{I_{loop}\,R_S}{R_3} = 0\ ;$$

Solving this with respect to I_{loop} gives:

$$\boxed{I_{loop} = V_{in}\,\frac{R_3}{R_1\,R_S} + V_{ref}\,\frac{R_3}{R_2\,R_S}} \qquad (1)$$

The design equations specifying the resistor values can be derived from (1). Assuming $V_{ref} = 2.5V$ and V_{in} ranges from 0- to 100mV, it follows:

(a) $I_{loop(min)} = V_{ref}\,\frac{R_3}{R_2\,R_S} \quad \Rightarrow \quad 4mA = 2.5\,\frac{R_3}{R_2\,R_S}\ ;$

(b) $I_{loop(max)} = V_{in(max)}\,\frac{R_3}{R_1\,R_S} + 4mA \quad \Rightarrow \quad 20mA = 0.1\,\frac{R_3}{R_1\,R_S} + 4mA\ ;$

Notes

Equation (a) and (b) have in in total four unknown resistor values. By chosing two of them the equations decide on the other two. The basic guidelines applied for the choice of the resistor set satisfying (a) and (b) are:

R_S should be small to minimise its voltage drop. Two problems are associated with a high voltage drop across R_S. Firstly, it causes variation in the reference diodes current with the loop current and hence affects their stability. Secondly, a high voltage drop increases the current flowing outside the control loop through R_3. However, very small resistor values are not available with high accuracy - say 0.1%, but a good compromise is 100Ω.

R_1's value is a compromise between minimising errors resulting from the op amp's input offset currents, I_{io}, to a level below that of the op amp's offset voltage, and simultaneously not loading the source. With I_{io}(max) = 3nA, a 10kΩ resistor gives only 30μV offset error compared with the op amp's 200μV (max) offset voltage at 5V supply. $R_4 = R_1||R_2||R_3$ ensures that only input offset current rather than input bias current contributes to the error.

R_2 should maximum be 1MΩ to allow a 0.1% high precision resistor to be used.

R_3 should be as high as possible to limit the current flowing outside the control loop but satisfy the same criteria as for R_2.

A set of values satisfying the above criteria and equation (a) and (b) is:

$R_S = 100\Omega$; $R_1 = 10k\Omega$; $R_2 = 1M\Omega$; $R_3 = 160k\Omega$; $R_4 = 9.32k\Omega$;

R_5 delivers the current required for the LT1009 shunt references, the op amp plus additional current for the sensor and its interface circuit. This current is stable with constant V_{in} but as the voltage drop across R_S varies with I_{loop}, the drop across R_5 varies as well. This in turn causes the current through the LT1009 references to shift accordingly. To avoid changes in the reference voltage this current must be kept fairly stable; hence the drop change across R_5 must be minimised placing constraints on a minimum power supply voltage and the value of R_{load}. Choosing $R_5 = 3.3k\Omega$ causes the current in the LT1009 references to vary by only 700μA, provided that $R_{load} = 50\Omega$. This choice also allows for up to 1.5mA reference current to be used for the sensor and its interface.

Error budget

The op amp's offset error, V_{io}, modifies the loop current, I_{loop}, of equation (1) as the voltage at the non-inverting input is $\pm V_{io}$ rather than zero volt with respect to Signal Common assumed for (1). If the op amp's input offset current, I_{io}, is taken into consideration, it should be summed with the other currents at the non-inverting terminal of the op amp. This yields:

$$\frac{V_{in} - V_{io}}{R_1} + \frac{V_{ref} - V_{io}}{R_2} - \frac{I_{loop} R_S + V_{io}}{R_3} - I_{io} = 0 \; ; \qquad \Rightarrow$$

$$I_{loop} = V_{in}\frac{R_3}{R_1 R_S} + V_{ref}\frac{R_3}{R_2 R_S} - V_{io}\frac{R_3}{R_S}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right) - I_{io}\frac{R_3}{R_S}\ ; \qquad (2)$$

An additional error source adding to I_{loop} of (2) is the current bypassing the control loop through R_3. All current passing through R_S is inside the control loop. In equation (1) we assumed that $I_{loop} = I_{R_S}$ but a more correct expression is:

$$I_{loop} = I_{R_S} + I_{R3} \quad \text{or} \quad I_{loop(3)} = I_{loop(1)} + I_{R3}\ ;$$

where $I_{loop(1)}$ is I_{loop} given by (1). By ignoring the insignificant effect from the op amp's offset error on the bypass current error: $V_{R3} = V_{R_S} = I_{loop(1)}\, R_S$ resulting in:

$$I_{loop(3)} = I_{loop(1)} + I_{loop(1)}\frac{R_S}{R_3} \quad <=> \quad I_{loop(3)} = I_{loop(1)}\left(1+\frac{R_S}{R_3}\right)\ ;$$

Substituting $I_{loop(1)}$ with I_{loop} of (1) yields:

$$I_{loop(3)} = V_{in}\left(\frac{R_3}{R_1 R_S}+\frac{1}{R_1}\right) + V_{ref}\left(\frac{R_3}{R_2 R_S}+\frac{1}{R_2}\right)\ ;$$

By adding the errors contributed by V_{io} and I_{io} in equation (2), ignoring the insignificant effect from the bypassed loop current on these errors, we have:

$$\boxed{I_{loop(3)} = V_{in}\left(\frac{R_3}{R_1 R_S}+\frac{1}{R_1}\right) + V_{ref}\left(\frac{R_3}{R_2 R_S}+\frac{1}{R_2}\right) - V_{io}\frac{R_3}{R_S}\left(\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}\right) - I_{io}\frac{R_3}{R_S}}$$

Notes

The difference between the worst case $I_{loop}(3)$ at 25°C and the ideal $I_{loop} = V_{in}$ 0.16 + 4mA is specified in the following error table:

Errors in 4- to 20mA Current Loop Circuit		Worst Case Error		
Error Source	**Tolerance Relative or Absolute**	**Low Level**	**Full Scale**	**Unit**
R_1, R_2, R_3, R_S	0.1%	12.0	60.1	µA
V_{ref}	0.2%	8.0	8.0	µA
V_{io}	200uV	34.3	34.3	µA
I_{io}	3nA	4.8	4.8	µA
I_{R3}	(R_S/R_3) I_{loop}	2.5	12.5	µA
Total Worst Case Error in I_{loop}		±61.6	±119.7	µA
Total Worst Case Error in % of Ideal I_{loop}		±1.5	±0.6	%

Note: Low Level = 4mA, Full Scale = 20mA.

The worst case untrimmed error of ±0.6% for full scale at 25°C is mainly dominated by resistor tolerances and the op amps input offset voltage. The chance of the individual errors being worst case and contributing in the same direction or adding up with the same sign is unlikely - so typically, the performance will be much better. However, by trimming R_2 for low levels (4mA) and R_1 for full scale (20mA) all of the above errors can be eliminated, reducing inaccuracy to drift with time and temperature of the same parameters. Such a trimmed circuit can achieve a similar accuracy as the untrimmed one at 25°C but over a 0°C to 70°C temperature range.

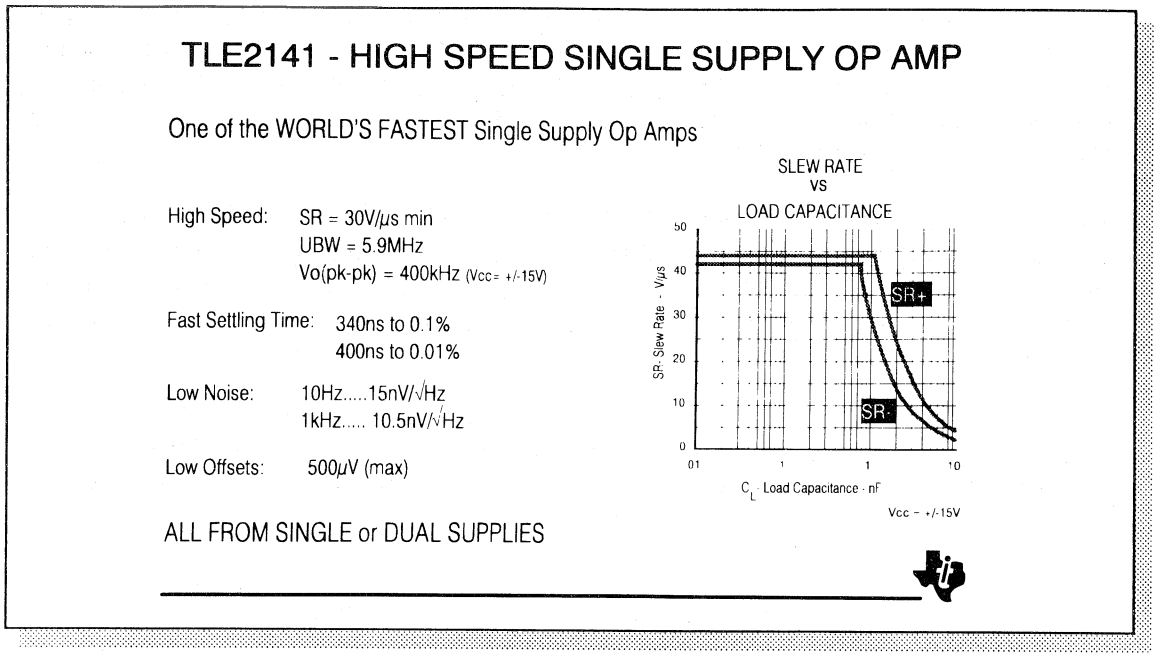


Figure 39 - TLE2141 - High Speed Single Supply Op Amp

The TLE2141 single operational amplifier is the latest Excalibur device. Like the other bipolar designs it uses Excalibur's high speed PNPs to enable it to achieve extremely high speed - it is probably the **Worlds fastest single supply op amp!** It combines a number of features which make it particularly well suited to high speed, precision applications particularly in control loops for system or process monitoring.

High Speed - The TLE2141 uses a double PNP input stage which enables it to operate from a single supply (ie its common mode input range includes ground). This technique has, in the past, limited the AC performance operational amplifiers - but by using Excalibur's high speed vertical PNPs and a patented input stage, the device has outstanding AC performance. The typical and symmetrical slew rate for the TLE2141 is **45V/μs** (30V/μs min) and its **settling time to 0.01%** is typically only **400ns**. These two parameters combined with a Gain-Bandwidth Product of 5.9MHz highlight just why this device is so well suited to control type applications. It should be noted that the TLE2141 is internally compensated.

Notes

Low Noise - Another parameter which one does not normally associate with a single supply, PNP input, operational amplifier is low noise. The TLE2141 however has a noise voltage specification in the audio band of **15nV/$\sqrt{\text{Hz}}$** at 10Hz and **10.5nV/$\sqrt{\text{Hz}}$** at 1kHz. This combined with the excellent AC performance and resulting low distortion makes the devices particularly well suited to hi-fi audio applications.

Output Drive - The NPN output stage has been designed to swing almost Rail to Rail (V_{CC-} +0.3 V to V_{CC+} - 1.8 V) without inducing phase reversal, and will happily drive 10nF capacitive loads. When this is combined with the 20mA (min) short circuit output current, then the device is extremely well suited to driving heavy loads such as long cables or for use in 4-20mA current loops.

Precision - This special design also exhibits an improved sensitivity to IC component mismatches that is evident by a 500µV offset voltage and 1.7µV/°C typical drift. The device also has the common mode and power supply rejection ratios set at a minimum of 85dB and 90dB respectively.

Applications - These wide range of features make the device extremely well suited to a number of different applications. High speed and fast settling time, combined with precision makes the device an ideal choice in fast actuator/positioning drivers or other control loop applications as well as performance audio systems. The accuracy, single supply operation (with rail to rail output) and low noise makes the TLE2141 particularly suitable for instrumentation and measuring equipment.

The device can also be configured as a comparator - both inputs can be maintained at Vcc+/- without damage and the typical open loop propagation delay with TTL inputs is 200ns.

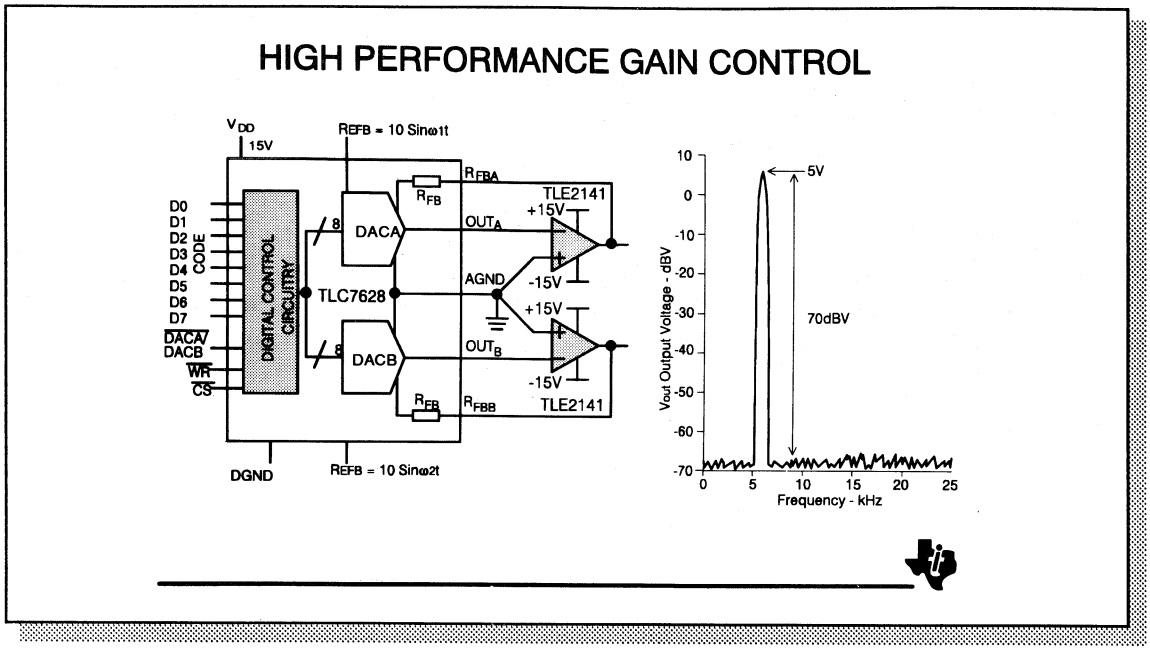


Figure 40 - High Performance Gain Control

In today's systems analogue systems are having to interface to more and more digital systems. This is applicable to the running of the engine in a car to the production of music in your Hi-fi.

Automatic gain control in the past was done by voltage controlled resistors or some other technique of altering the resistance in a feedback loop. Interfacing to digital systems, where the digital signal processor is the control element allows much more simple and reliable techniques for AGC. Multiplying DACs are one such solution.

A multiplying DAC multiplies its reference input voltage by the code fed into its digital inputs. This can be very useful where multiplication of an analogue and a digital signal is required and for AGC circuits. The **TLE2141**is well suited to these applications offering its high unity-gain bandwidth and slew-rates coupled with its low offset voltage and common-mode range down to the negative rail.

Notes

The configuration shown has numerous applications, one being as a digital audio gain adjust. With audio systems having bandwidths extending to above 20kHz the op amp used needs to have low distortion and a good unity-gain bandwith. Depending on the position of the op amp, it will also need a good low noise level. The TLE2141 has been designed to offer the high speed and high performance required at low noise levels.

The DAC used must also be capable of responding to the signal level required by the system. The TLC7628 is capable of operating from a 15V supply whilst maintaining TTL compatibility, and have reference input voltages to ±10V. The TLC7628 is the only one of its type to be able to interface directly to Texas Instruments' DSPs. The speed of the system will be limited by the DAC; the guaranteed resistor ladder value is 20kΩ this coupled to the maximum output capacitance due to the ladder of 120pF gives a 3dB bandwidth of 66kHz. This is more than ample for audio, for higher speeds of operation the feedback resistors R_{FB} can be made smaller; reducing the time constant and gain. The reduced gain may not be a problem as the DAC would essentially function as a digital attenuator, and so for noise optimisation would be preceded by a form of pre-amp.

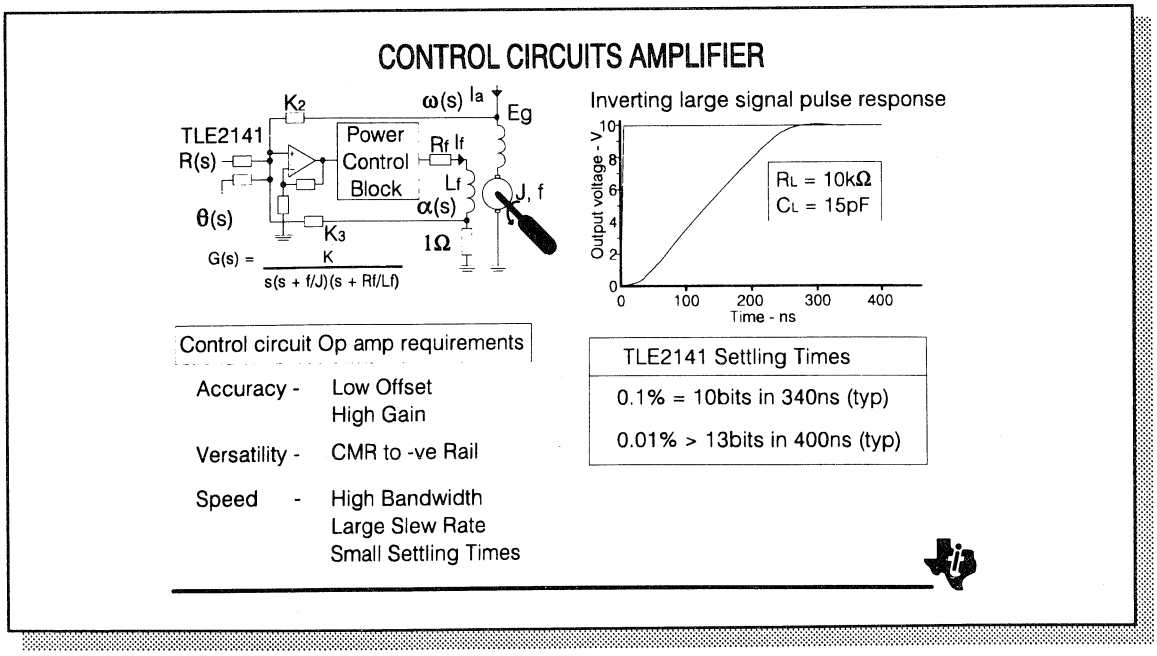


Figure 41 - High Performance Control Circuits Amplifier

A common linear function in which performance amplifiers are frequently used is in electronic control systems. An analogue measurement element requires signal processing before it is measured and fed back to the control element. In the past these systems were predominantly analogue, however DSP based systems are becoming increasingly common - in both cases linear signals must be handled and op amps are the main signal conditioning element.

This figure shows a typical analogue system, where the control element has to monitor and affect the position of a field controlled motor. The normal operation of the motor has a transfer

function of G(s) between the control input voltage, r(s), and the motor position θ(s). Stability of the system can be assured by measuring key variables within the system and feeding them back to the input. By sensing the field current, it is possible to evaluate the torque and/or acceleration of the motor (this is the second derivative with respect to time of the position of the motor). The back e.m.f. developed across the motor can be used to find its angular velocity (the first derivative with respect to time of the position of the motor). Feeding these signals back to, and comparing them with, the actual excitation of the sensor, makes it is possible to evaluate and control the position of the motor..

In the above, and other analogue systems, the signal processing modifies the open loop system gain, in a way similar to how an op amp's feedback changes its open loop gain. A technique called 'State Variable Feedback' (often used in active filter design), is frequently used in analogue systems - Here the control network uses differentials and integrals of the feedback signal in order to change the systems operation and ensure stability. It is in these functions that operational amplifiers are commonly used.

In Digital systems the signal conditioning circuits perform more of a typical function - signals are filtered, amplified and level shifted to ensure they are in a format suitable for an ADC. A form of State Variable feedback is also used in digital systems - known as PID (Proportional, Integral and Derivative) control, again measurements are taken of the control signal before they are fed back to the system.

The key factor however is that both systems require performance operational amplifiers. High speed and fast settling times reduce delays and improve response times, low offsets and high open loop gains improve system accuracy. While the ability to operate from single or dual supplies with wide common mode input and output ranges improves flexibility and increases dynamic range. All these factors were specifically considered when Texas Instruments developed the TLE2141, the latest op amp designed using the Excalibur technology. The part, developed for use in single or dual supply applications, has an impressive 45V/μs slew rate and very impressive settling times.

AC performance and fast settling times are critical parameters if an op amp is to be used effectively in a control system. An op amp can be approximated to a two pole model, the compensation capacitor splits the poles of the op amp creating a low frequency dominating pole. The op amp's feedback modifies the position of the dominating pole and raises it to a frequency similar to that of the second pole. When a pulse is applied to an op amp, it is the interaction of these two poles which give the characteristic exponential decaying sine wave superimposed upon on the pulse input. The position of the second pole determines the

Notes

stability of the pulse response - if it is too low (implying a poor phase margin), large overshoots and long settling times will occur. Large overshoots can cause a system to swing the 'wrong way' and poor settling time can result in the system not reaching equilibrium. An example of a critical system is a hard-disc drive - here response time is crucial and poor op amp stability could cause the reader head to crash into the disc. Therefore in high speed systems an op amp requires not only a fast slew rate but must also have a good settling time and large phase margin.

As highlighted, the TLE2141 provides a phase margin of 58°, 42V/µs slew rates and a settling time to 0.01%(12 bit or greater) of just 400ns. The slew rate therefore ensures a fast pulse rise time and the large phase margin will quickly damp the overshoot, making the part ideal for these form of applications. To minimise the overall steady state error the op amp must have a small D.C. error. The TLE2141's high open loop gain coupled with its offset voltage of 500µV provide the very small steady state errors required by many systems, including those where high speed might at first seem to be the only requisite.

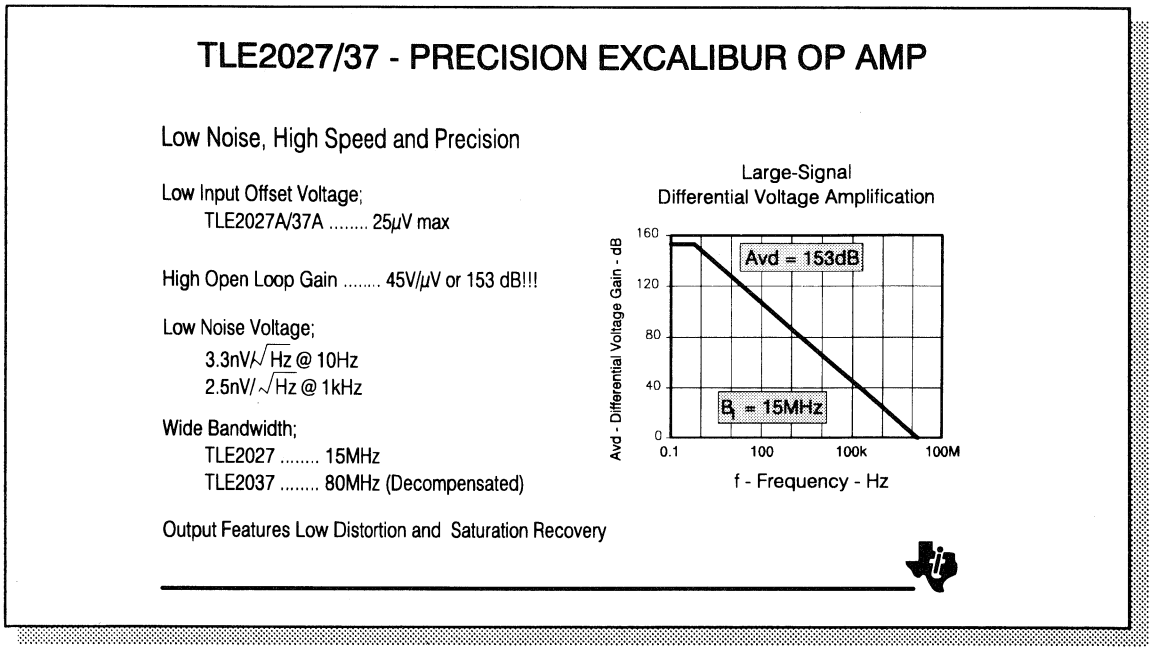


Figure 42 - TLE2027/37 - Precision Excalibur Op Amps

The TLE2027 and TLE2037 are among the most recent op amps to be developed and fabricated using the Excalibur technology. These devices have been optimised for precision and include a novel output stage that features a 'Saturation Recovery Circuit' which enables much improved small signal response and outstanding levels of distortion.

Precision - The parameters of most importance in a precision application are; Offset Voltage, Drift, Bias Currents and Open Loop Gain - both these devices have outstanding performance in all these areas. The TLE2027A and TLE2037A have a maximum offset voltage of only

25µV and a maximum offset voltage drift of **1µV/°C and 1µV/month**. A bias current cancellation circuit reduces bias currents to typically 6nA enabling larger external resistors without impacting overall DC accuracy.

An outstanding parameter of both devices is their open loop gain, **Avd; - at 153dB**, it is probably the **highest in the world!** The resulting improvement in the op amps circuits 'loop-gain' causes an increase in overall performance - everything from offset voltage, input impedance and distortion are improved.

AC Performance - The TLE2037 is a decompensated version of the TLE2027. It must be used with a minimum closed loop gain, Acl, of 5, but the unity gain bandwidth product for the **TLE2037 is 80MHz** (compared with **15MHz** for the TLE2027). Slew Rates for the TLE2027 and TLE2037 are 2.8V/µs and 7.5V/µs respectively.

Low Distortion - Linked to an increase in AC performance both devices feature a **Saturation Recovery Circuit** which improves the small signal response and enables the device to be used at much higher frequencies with increased output swings - see figure 38. A further advantage is the extremely low levels of distortion even when driving loads as low as **600Ω,** (see figure 39) which has enabled the device to be used in low noise applications such as Audio systems.

Low Noise - A large input stage, and clever design and layout techniques has given the device an extremely low noise voltage specification - **3.3nV/$\sqrt{Hz}$ at 10Hz**, and **2.5nV/$\sqrt{Hz}$ at 1kHz.** This is an obvious further benefit to precision measurement systems and audio applications.

Applications - The excellent AC performance and low noise makes the devices ideally suited to Audio and Telecom applications, whilst the low offsets and excellent overall precision has enabled the parts to be used in Instrumentation, Measurement and Test equipment.

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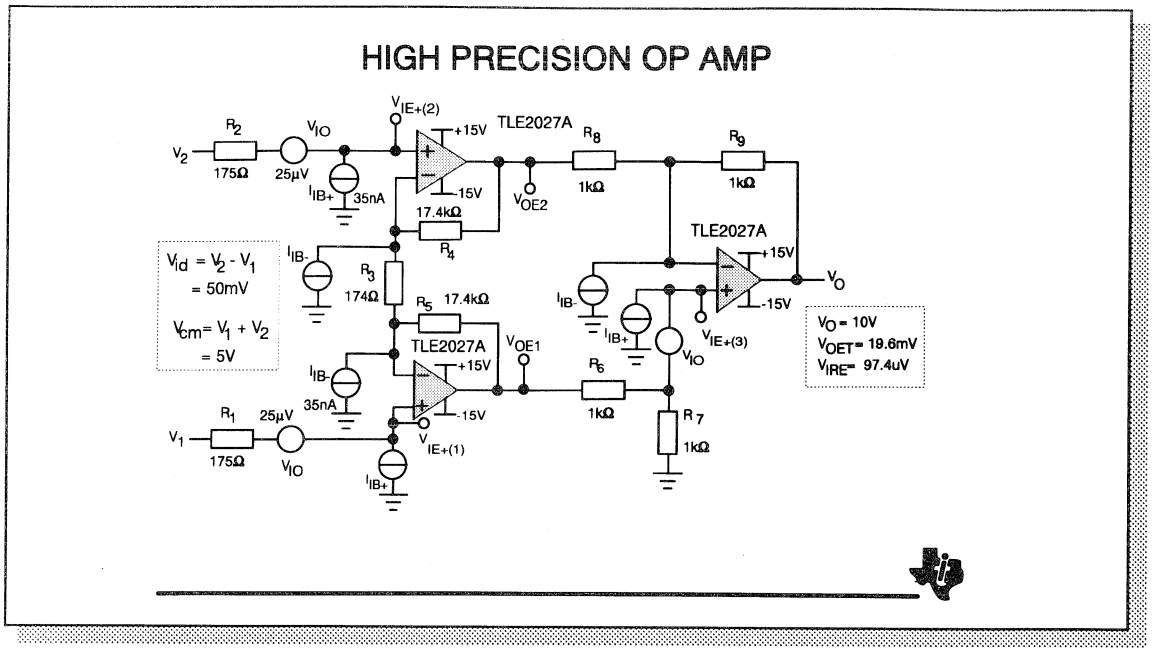

Figure 43 - High Precision Op Amp

As with any design, the input stage will have a significant effect on the overall performance of the system, particularly noise levels, DC accuracy and AC accuracy. One configuration which needs maximum performance is the instrumentation or difference amplifier, typically used in applications that require the ability to pick-out small differential voltages which are super-imposed on large common-mode signals. One op amp ideal for such applications is the **TLE2027A**.

The ideal instrumentation amplifier has infinite input impedance, large differential voltage gain and zero common-mode gain. The most simple instrumentation amplifier consists of a single amplifier configured as amplifier A3 above. This has major drawbacks in:-

1) The input impedance is not infinite, but is equal to the sum of R_6 and R_7 on the non-inverting input and varies with differential input voltage on the inverting input.

2) The common-mode gain depends largely on the matching of resistors R_6 and R_7 to R_8 and R_9.

These problems can be overcome by the configuration shown above. Amplifiers A1 and A2 provide high differential gain, and unity common-mode gain. Another advantage is that the input impedance of the instrumentation amplifier is now the input impedance of the amplifiers.

The choice of amplifier will now have the largest effect on the total performance of the system, and for optimum performance errors associated with each amplifier will need to be reduced. Op amps are always used in a feedback loop and due to their finite open-loop gain and finite

gain-bandwidth product, errors will be introduced. The feedback will reduce some of these problems and using a high performance op-amp will set most problems at a much lower level than others.

Op amp considerations.

One consideration is **input impedance**, which is the input impedance of the op-amp multiplied by its desensitising factor $1+A\beta$; An op-amp with a large open loop gain will increase the input impedance to the order of $10^{12}\Omega$. This means that the **bias currents** are a much more important problem, especially when considering performance over temperature. The TLE2027 implements bias current cancellation techniques, resulting in the op-amp having low bias currents coupled with high speed and large open-loop gain.

Common-mode and **power supply** effects are another source of error and should not be neglected. The op amps will normally be looking at very small differential signals superimposed on large common-mode signals, which means that to preserve performance and accuracy the op amp needs to have a large common-mode rejection ratio. The TLE2027 has a typical CMRR of 131 dB, which is equal to 282nV/V, and a PSRR of 144 dB equivalent to 63 nV/V.

The **gain error** due to the op-amp can introduce further system performance limitations, especially when operating at the high gains demanded by instrumentation amplifiers. The TLE2027 has an open loop gain of 45 million! - hence with a gain of 1000 the gain error is still only 0.0022%.

Drift of the op amp's offset voltage can limit the overall accuracy of the system, in particular with time and temperature, as this is one parameter which cannot be corrected or nulled out. The effects of both these are normally technology dependent, and as already discussed the excalibur process provides stability in both domains. The TLE2027A has a typical temperature co-efficient of input offset voltage, α_{VIO}, of 200nV/^{o}C. When considering the drift with temperature there are two aspects to take into account, the most obvious being the change in ambient temperature. The other is due to changes in junction temperature caused by self heating of the integrated circuit. The ultimate drift in offset voltage due to self heating will be package dependent due to differing thermal resistances.

Notes

Application errors

The configuration shown uses op amps A1 and A2 to provide a large differential gain (201) whilst providing a unity common mode gain. The errors associated with these op amps will be very similar.

The worst case values of CMRR and PSRR of the TLE2027 reduces errors associated with a common-mode voltage of 5V and a 15V supply (10% tolerance) to16.5 µV. The quiescent supply current dissipates a power of 141mW, this coupled with power dissipated in the output stages to drive the feedback and load resistors increases the offset voltages of A1 and A2 by 20.9µV and 27.5µV respectively. The cancellation circuitry for the bias currents reduces their related errors to 6.1 µV; while the open loop gain of the TLE2027 reduces any gain error to 252 nV (for a 50 mV differential input voltage).

Taking these into account the errors referred to the non-inverting input, V_{IE+}, is equal to:-

$$V_{IE+} = V_{IO1} + I_{IB+}*R_1 + \Delta T \alpha V_{IO} + V_{in1}* \text{CMRR} + 2V_{cc}*10\%*\text{PSRR}.$$

For A1 V_{IE+1} = 68.5µV and for A2 V_{IE+2} = 75.1µV.

The feedback network around each op amp ensures that the inverting input will be equal to the non-inverting input (the actual system input) plus or minus the errors, V_{IE+}, discussed above. This results in V_{IE+} also appearing as an input for the opposing op amp in the differential input pair. Therefore op amp A1 will multiply its offset errors by its normal non-inverting gain and it will also multiply the offset errors of A2 by its inverting gain, (the converse is true for A2). Op amp A3 with its differential gain will effectively result in the offset errors of A2 being multiplied by -201, and the offset errors of A1 multiplied by 201. The bias currents from the inverting input cause an offset voltage on the output of each amplifier equal to the bias current multiplied by the feedback resistor (R_5 or R_4), this can be referred to the input of the op amp by dividing by the non-inverting gain.

This results in the output of amplifier A1, V_{OE1}, being equal to:-

$$V_{OE1} = V_{IE+1} * \left(1 + \frac{R_5}{R_3}\right) - I_{IB-}*R_5 - V_{IE+2} * \left(\frac{R_5}{R_3}\right)$$

while the output of amplifier A2, V_{OE2}, will be:-

$$V_{OE2} = V_{IE+2} * \left(1 + \frac{R_4}{R_3}\right) - I_{IB-}*R_4 - V_{IE+2} * \left(\frac{R_4}{R_3}\right)$$

These equations ignore the very small gain error of the TLE2027. The inverting input bias current error, $I_{IB-}*R_5$, equals 609µV.

Op amp A3 should remove the common-mode signal still present on the outputs of A1 and A2. It will also introduce similar errors to A1 and A2 except that the bias current error will be greater due to the larger source resistors. Assuming true matching between resistors R_6, R_7, R_8 and R_9, the bias current error will be reduced to the offset current error. When using op amps with bias current cancellation techniques the benefits of matching source resistances are reduced and will actually reduce the performance for low noise applications. The input stage has special circuitry, using matched transistors, to provide the bias currents for the differential input transistors.

The errors introduced by junction temperature will also be different; the output of A3 will be approximately 10V while its inputs should be about 5V, resulting in its output sourcing 5mA which dissipates a further 25mW within its output. This extra power dissipation coupled with quiescent power will cause a drift of 21µV. Taking this drift and the offset current error of 15µV, 30nA x 500Ω, into account the error introduced by A3 will be 77.5µV; the non-inverting gain of A3 doubles this to yield 155µV, which in this configuration is negligible.

The non-inverting errors due to A1 and A2 are multiplied by 201. This results in an error due to A1 of

$$201 \times 68.5\mu V - 609\ \mu V = 13.16mV.$$

and an error due to A2 of:-

$$201 \times 75.1\mu V - 609\mu V = 14.49mV.$$

Due to the structure of the circuit the errors of A1 and A2 would normally subtract, but as these errors are related to separate integrated circuits they will tend to be uncorrelated, dual precision op amp would have most of these errors subtracted from each other. A way of minimising the probable overall error is to take a RMS sum of these errors. If this is done the error achieved is 19.6mV. Relating this error to the input of the instrumentation amplifier results in an offset error of only 97.4µV.

The large common-mode signal has increased the errors due to the opamps' finite common mode rejection ratio, and such a large common-mode signal applied to the third amplifier could add further errors caused by mismatching between resistors R_6 to R_9. Replacing R_7 with a trimming variable resistor allows for any further error adjustment.

Notes

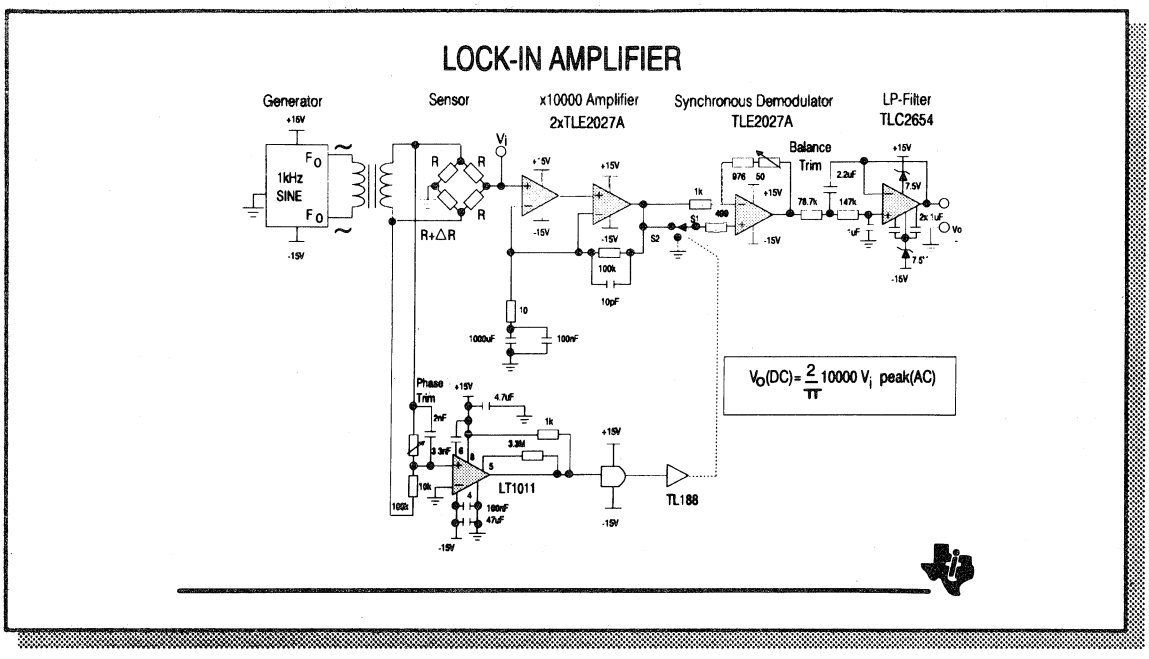

Figure 44- Lock-in Amplifier

Feeding a sensor bridge with an AC signal allows outputs from capacitive, inductive as well as resistive sensors to be measured. Additionally, the sensitivity can be very high and is usually only limited by the thermal noise of the sensor, the noise of the high gain sensor amplifier and the systems bandwidth. When the signal frequency is constant a very narrow bandpass filter following the high gain amplifier can extract sensor signals buried in noise. A further signal rectification and averaging gives a DC output proportional to the sensor change. However, to build a narrow bandpass filter with, for instance, a 1kHz center frequency and a 1Hz bandwidth requires very precise components to ensure frequency accuracy and stability. Similarly, the sinewave generator frequency must be very accurate and stable.

This application shows one way to get over the frequency problem. The principle is still based on an AC carrier approach converting a change in a sensor impedance to a DC voltage. The amplifier shown is followed by a synchronous demodulator that detects the amplified carrier modulated sensor signal. Because the desired signal information is contained within a carrier, the system constitutes an extremely narrow-band signal path. Non-carrier related components are rejected and the amplifier passes only signals which are coherent with the carrier.

The very high gain (x10000) AC amplifier is implemented by using a double TLE2027 amplifier block to achieve an impressive 160dB open loop gain at 1kHz. The composite amplifier provides a typical 3dB bandwidth of 150kHz with a very accurate closed loop gain of 10000.

The zero transition synchronized demodulator implemented by another TLE2027 shift its gain between +1 and -1 in phase with the 1kHz carrier. The "rectified" output signal is then

smoothed with a 1Hz active filter around the TL051A to provide a DC output, V_O, proportional to the sensor bridge output Vs.

The dynamic range of the circuit is from $1\mu V_{pp}$ to $1mV_{pp}$ at Vs. with $20V_{pp}$ across the bridge, the $\delta R/R$ sensitivity of the system is able to measure a change in the sensor from one part in a million fairly accurately.

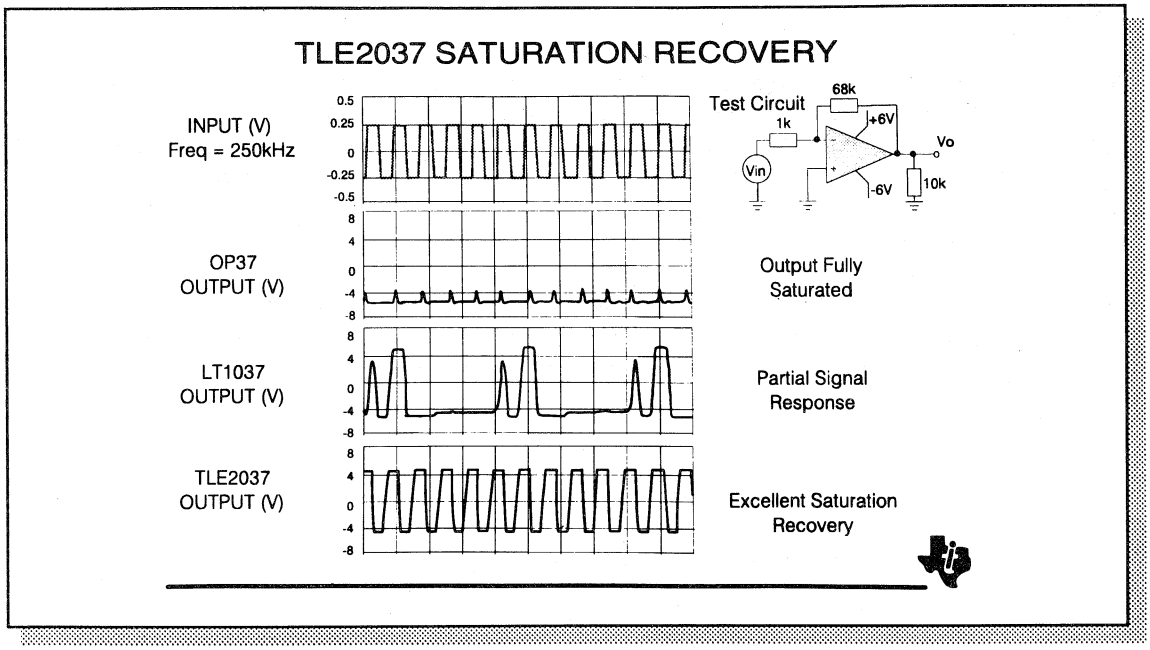

Figure 45 - TLE2037 Saturation Recovery

In conventional OP-27 type amplifiers the output voltage remains predictable only if it stays within the V_{om} (maximum Vout) specification. If an input signal is applied which tries to force the output voltage beyond the V_{om} limit, the output may not respond correctly to subsequent input signals until after a given amount of time has passed. This time is the "Output Saturation Recovery Time".

Notes

There are three things that can cause the OP-27 type amplifiers to exhibit output saturation recovery problems. First, in some of the amplifiers, the final common emitter gain stage is allowed to be driven heavily into saturation. the excess base charge built up on the device can only be removed via a high value pull down resistor. Therefore a finite time must pass before enough charge is removed to assume normal operation.

Secondly, the current sources in the class AB output stage are also allowed to saturate. These are not driven as heavily into saturation, but they will also take a finite amount of time to recover.

Thirdly, and perhaps most importantly, the bias generator for the entire circuit can be disturbed from its equilibrium point when the output stage current sources saturate. If disturbed enough, the bias circuit can shut off completely until the start-up circuit engages. If this happens the entire circuit loses power and the output signals will not become valid again until the bias generator recovers from its equilibrium point. This results in a huge output saturation recovery time.

In the TLE2027/37, special circuitry has been added to keep the final gain stage and the output stage current sources out of saturation. Therefore, no saturation recovery time is needed and the device continues to operate in a normal, stable and predictable manner.

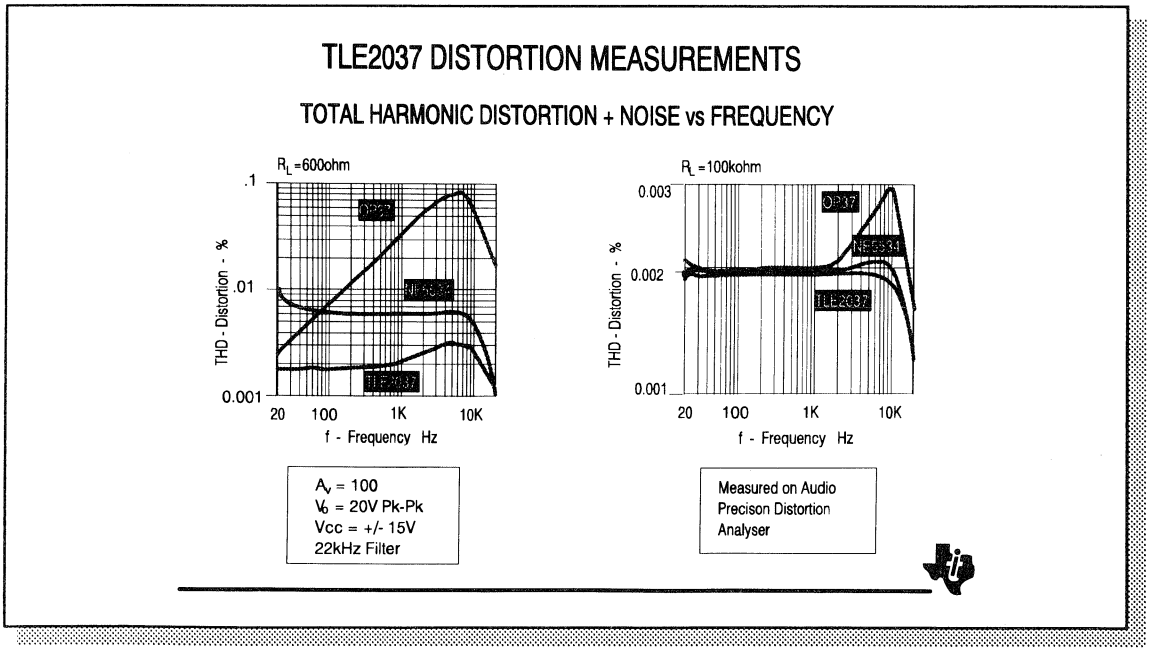

Figure 46 - TLE2037 Distortion Measurements

The graphs above compare the 'Total Harmonic Distortion + Noise' of 3 different op amps, over frequency, whilst driving 100kΩ and 600Ω loads.

The three amplifiers highlighted in the graphs (the NE5534, LT1037 and TLE2037) are all bipolar designs and have been chosen because of their specified low levels of noise and distortion. These graphs highlight the superior performance of the TLE2037 Excalibur op amp.

The THD of an amplifier is dependent upon many parameters, specifically the open loop gain, bandwidth, slew rate, load and the input signal magnitude. The circuit used to compare these three amplifiers emphasises many of these points. A non-inverting gain of 40dB has been chosen to highlight the importance of the loop-gain of the op amp. To ensure that noise does not conceal the THD of the op amps a 22kHz noise filter has been introduced - this explains the shape of all curves at high frequencies. This frequency is however wide enough to highlight any problems due to slew rate limiting.

Loop gain (the difference,$1+A\beta$, between the open loop and closed loop gain curves) is a crucial factor in low distortion circuits. This, combined with the obviously low levels of noise for bipolar op amps, explains why CMOS or Bifet designs suffer from relatively poor distortion compared to bipolar. The TLE2037 has a typical open loop gain of 153dB (45 million!) and so distortion is significantly reduced. Slew rate is another crucial factor in low distortion circuits as at high frequencies and high gains an op amp may not be capable of operating without clipping or distorting the output signal.

The second graph, examines how a load affects an op amps distortion. The impedance used in these measurements is 600Ω and it shows that the OP-37 device is really not suited for applications with loads as heavy as this. What the graph does highlight is the outstanding performance the TLE2037, it has significantly better distortion than its competitor, the OP-37 and also outshines the NE5534.

The TLE2037 is therefore an ideal op amp in applications driving high impedance nodes and can be used for driving cables as well as multiple parallelled loads. The overall low distortion of this part also makes it particularly useful in audio applications including microphone pre-amps, filters and equalisation circuits.

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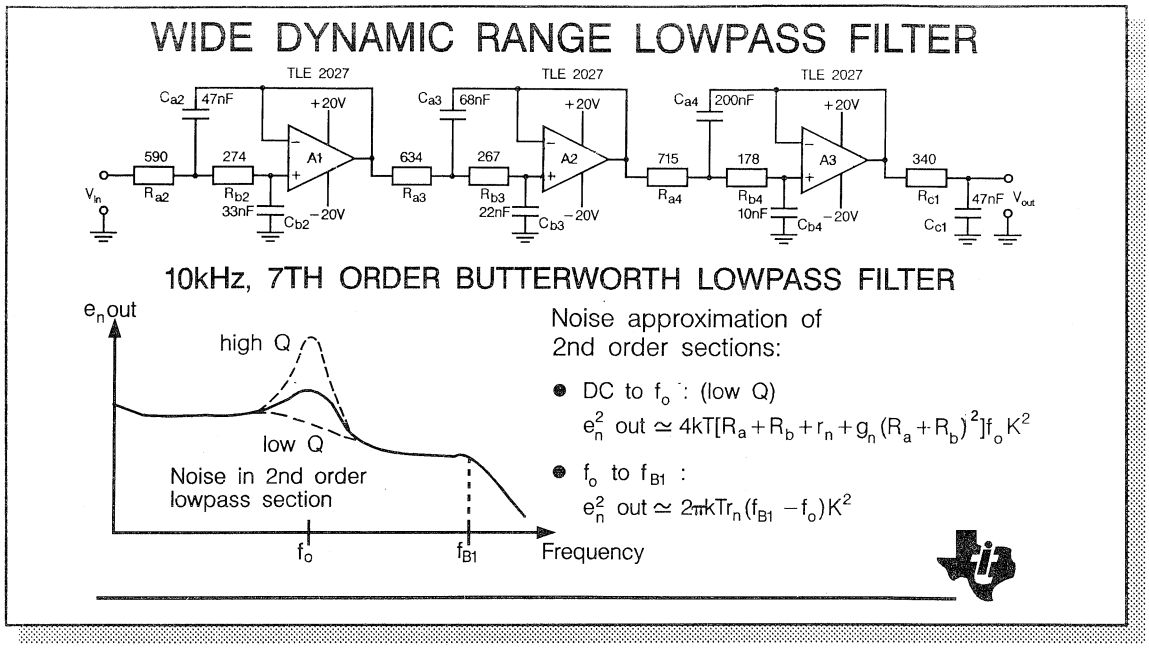

Figure 47 - Wide Dynamic Range Lowpass Filter

Low Noise Active Filter Design

The maximum signal-to-noise-ratio or dynamic range of an active filter is determined through its output noise spectral density and the rms noise voltage. The noise performance of each filter can be analysed by taking the sum of the squares of the individual noise sources and calculating their impact on the output voltage. This calculation is often complex as many noise sources are involved.

If an active filter is required with a wide dynamic range, the fundamental design considerations below must be followed:

- The dynamic range increases with extended supply rails. The Excalibur TLE2027 is capable of operation from ±22V supplies providing an output swing in excess of ±19V with a 2kΩ load.

- To benefit from the low input noise voltage performance of the chosen op amp, the noise from its source impedance should be less than the noise it generates itself. TLE2027's input noise voltage is equivalent to the thermal noise from a 380Ω resistor.

- The input noise current of the op amp multiplied by the impedance it is flowing through should be less than the thermal noise from the source impedance and less than the op amp's input noise voltage. With network impedances below 20kΩ seen by the input noise current sources, noise current is not likely to dominate a TLE2027 application.

- The impedance level of the passive network should be kept low enough to prevent the thermal noise it exhibits to exceed the noise contribution from the op amp.

- In higher order filters, the individual filter sections can be placed in an order to minimise noise by having the highest Q sections first, but this limits the filter's maximum input swing and affects the top of the dynamic range. A compromise should be made to ensure that all sections utilize the maximum dynamic range of the op amp.

- Current flowing in resistors produce excess noise in addition to the thermal noise due to inhomogeneity in the resistor material. Metal film type resistors produce less noise than carbon film resistors and should hence be employed. In addition, larger sized resistors are less noisier than smaller ones.

- Sensitivity of large capacitors to mechanical vibrations, microphonics or hum pick-up can be a problem although large capacitors are normally associated with low impedance levels. Dividing a large capacitor up in two makes it possible to cancel picked up hum by ensuring that magnetic fields passed through the two capacitors in opposite direction.

- Thermo-electrical voltage changes caused by rapid temperature variations across joints of dissimilar materials increase low frequency noise. The solution is to reduce air flow across the circuit.

- In low frequency designs, the op amp's flicker or 1/f noise must of course be considered. TLE2027 has a very low 1/f corner adding insignificant noise to filter designs above 100Hz.

- Use non-inverting op amp filter configurations in low gain applications, as their noise is less. In a unity gain configuration, an inverting amplifier produces twice as much output noise as a non-inverting amplifier.

Often, a compromise between several diverting requirements has to be made. One example is the necessity for a general low impedance level, which of course has to be considered together with the chosen op amp's drive capability.

2nd Order Lowpass Filter Section

Notes

To realise a higher order lowpass low noise filter, a standard Sallen and Key 2nd order filter block was chosen. Cascade coupling of three sections are used to implement the total filter shown. The chosen 2nd order block can be designed to provide excellent noise performance but exhibits relative high Q factor sensitivity to the op amp's gain accuracy. However, as long as a unity gain or follower op amp configuration is used, the gain can be made very accurate without the need for precision resistors. A further limitation is that the open loop gain left in the op amp at the highest frequency, f_o, of interest must be high enough to implement the necessary Q factor accurately. A guideline for the op amp's required unity gain bandwidth, $B1 > 300 * Q * f_o$.

By applying the fact that the sum of the current flowing into the junction between the two input series resistors and the feedback capacitor must be zero, the transfer function for the individual 2nd order lowpass filter section can be shown to be given by:

$$\frac{V_{out}}{V_{in}} = \frac{\dfrac{1}{R_a R_b C_a C_b}}{s^2 + \left(\dfrac{1}{R_a C_a} + \dfrac{1}{R_b C_a}\right) s + \dfrac{1}{R_a R_b C_a C_b}} = \frac{\omega_o^2}{s^2 + \dfrac{\omega_o}{Q} s + \omega_o^2} \qquad (1)$$

From this it follows that:

$$\omega_o = \sqrt{\frac{1}{R_a R_b C_a C_b}}; \quad \text{and} \quad \frac{1}{Q} = \sqrt{\frac{R_b C_b}{R_a C_a}} + \sqrt{\frac{R_a C_b}{R_b C_a}}; \qquad (2)$$

Design Procedure

Given ω_o and Q for the filter, the design steps can now be derived as follows:

1. Choose C_a
2. Choose $C_b = k * C_a$; where k = ratio between any two capacitors in a standard series, like E6, E12 or E24. A restriction for k that allows a solution of the resistor design equations is given by:

$$k < \frac{1}{4Q^2};$$

3. Calculate R_a from: $$R_a = \frac{1}{2 C_a \omega_o} \frac{1}{k Q} \left(1 \pm \sqrt{1 - 4 k Q^2} \right);$$

4. Calculate R_b from: $$R_b = \frac{1}{R_a k C_a^2 \omega_o^2};$$

Note that the values of R_a and R_b can be swopped.

Sensitivity

The sensitivity of Q and ω_o with respect to the filter parameter, x, is defined as:

$$S_x^Q = \frac{d(\ln Q)}{d(\ln x)} = \frac{x}{Q}\frac{dQ}{dx}; \quad \text{and} \quad S_x^{\omega_o} = \frac{d(\ln \omega_o)}{d(\ln x)} = \frac{x}{\omega_o}\frac{d\omega_o}{dx}; \quad (3)$$

Thus, S_x^Q gives the incremental change in Q due to an incremental change in x. For example if S_x^Q is equal to 0.5, then it implies that a 2% change in x will cause a 1% change in Q. For the given 2nd order block, the following sensitivities can be found by applying equation (3) on (2):

$$S_{R_a}^{\omega_o} = S_{R_b}^{\omega_o} = S_{C_a}^{\omega_o} = S_{C_b}^{\omega_o} = -\frac{1}{2};$$

$$S_{A_1}^{\omega_o} = 0 \text{ ; where } A_1 \text{ is the unity gain accuracy of the op amp.}$$

$$S_{R_a}^{Q} = -\frac{1}{2} + \frac{Q}{\omega_o R_a C_a};$$

$$S_{R_b}^{Q} = -\frac{1}{2} + \frac{Q}{\omega_o R_b C_a};$$

$$S_{C_a}^{Q} = -\frac{1}{2} + \frac{Q}{\omega_o C_a}\left(\frac{1}{R_a} + \frac{1}{R_b}\right);$$

$$S_{C_b}^{Q} = -\frac{1}{2};$$

$$S_{A_1}^{Q} = \frac{Q}{\omega_o R_b C_b};$$

Notes

Why Use the TLE2027

The High performance Excalibur op amp TLE2027 is well suited for low noise active filter applications because of its low noise voltage of $2.5nV/\sqrt{Hz}$ combined with its wide unity gain bandwidth of 15MHz. In addition, TLE2027's good output drive capability and low distortion allow for a low impedance passive network to be used, which in turn exhibits less thermal noise. In applications where a wide dynamic range is required, the TLE2027 offers operation from ±22V supplies. Particularly, in lowpass filter design as the one shown, it is possible to maintain excellent DC accuracy thanks to the Excalibur op amp's extreme low and stable offset voltage. Selections down to 25μV max. are available.

Low Noise Design Considerations

The noise of a 2nd order section can be analysed directly from the formula:

$$e^2_{n\,out} = \int_{-\infty}^{\infty} \left[\sum_{j=1}^{k} \left(|T_{i,j}(j\omega)|^2 i_{j,n}{}^2(\omega) \right) + \sum_{i=1}^{m} \left(|T_{e,i}(j\omega)|^2 e_{i,n}{}^2(\omega) \right) \right] d\omega \; ; \quad (4)$$

Where $T_i(j\omega)$ and $T_e(j\omega)$ are transfer functions from noise current and noise voltage generators having efficiency i and e respectively. The noise sources are easy to identify; however the transfer functions for the noise sources are more cumbersome. The real difficulties start when we want to integrate the noise over frequency to determine the total output noise. Computer calculations using Macro models that include noise for the op amp and added thermal noise sources for the resistors can give fairly accurate results. However, they don't allow for direct analysis of the contribution from the individual noise sources and circuit optimisation.

As long as we are discussing low noise lowpass filter design with low Q values, the analysis can be simplified by dividing the noise up into two frequency areas; below and above the filter's cut-off frequency, f_o. Assuming low Q factors, it can be shown from (4), that the noise density in the low frequency passband is constant and that the noise in the high frequency stopband is coming mainly from the op amp's noise voltage frequency limited by the op amp's unity gain bandwidth or the succeeding filter roll off. The approximated total rms noise voltage at the output of the 2nd order block takes then the form:

$$\boxed{e^2_{n\,out} \cong 4\,k\,T\,(R_a + R_b + r_n + g_n\,(R_a + R_b)^2)\,f_o\,K^2 + 2\pi\,k\,T\,r_n\,K^2\,(f' - f_o)} \; ; \quad (5)$$

Where $r_n = \dfrac{e^2_n}{4\,k\,T}$; (e_n, is the input voltage noise associated with the opamp used).

and $g_n = \frac{i_n^2}{4\,k\,T}$; (i_n, is the input current noise associated with the opamp used).

k = 1.38 * 10-23 J/K ; (Boltzmann's constant).
T = Absolute temperature in Kelvin ; (298 @ 25°C).
f_o = Lowpass filter's cut-off frequency.
f' = Unity gain bandwidth, B1, of the used op amp.
K = Filter gain.

The first term of formula (5) can be interpreted as broadband noise in the passband of the filter $0 < f < f_o$, while the second as a broadband noise in the stopband $f_o < f < f' * \pi/2$; assuming a first order roll-off noise bandwidth. Note that the stopband noise is determined by the op amp's input and that flicker noise is not included. Evaluating the noise using (5) makes it easy to compare the individual sources contribution to the total noise.

7th Order 10kHz Lowpass Butterworth Filter Design

For the shown lowpass filter a Butterworth approximation was chosen. This provides an accurate DC gain, which is often important in lowpass filter applications, where high DC performance is required. The impedance level of each passive network was chosen as low as possible to reduce thermal noise but simultaneously kept at a level where the op amp was capable of driving it.

Butterworth Filter Parameter Values

The composite 7th order 10kHz lowpass filter can be realised using three second order lowpass filter blocks and one 1st order simple RC network in a cascade coupled configuration. The Q factors and ω_o values for the normalised filter stages are available from a Butterworth filter table:

Stage	Q Factor	ω_o	Gain at ω_o	Max Gain
1	A real pole	1	-3.00dB	0dB
2	0.554958	1	-5.20dB	0dB
3	0.801937	1	-1.97dB	+0.22dB
4	2.246979	1	+7.03dB	+7.25dB

Notes

Calculation of Component Values

From a noise point of view it was decided to place the passive RC section, stage 1, last. This slightly limits the input swing and the top of dynamic range due to overshoot in stage 4, but significantly reduces the stopband noise. A disadvantage from this structure is the relatively high output impedance of the filter. However, if the filter is interfaced to the high impedance input of an A/D converter this should not present any problem. The order of the filter sections realised with the previous described 2nd order lowpass Sallen and Key building blocks becomes now:

Realised Stage Order:	2, 3, 4, 1
Table Stage Order:	1, 2, 3, 4

By using the design procedure for the second order blocks and performing the frequency transformation from the normalised $\omega_0 = 1$ to $\omega_0 = 2\pi * 10\text{kHz}$, follows:

Stage	C_a	C_b	R_a	R_b
2	47nF	33nF	Ideal: 594.2Ω E96 std. value: 590Ω	Ideal: 274.9Ω E96 std. value: 274Ω
3	68nF	22nF	Ideal: 635.8Ω E96 std. value: 634Ω	Ideal: 266.3Ω E96 std. value: 267Ω
4	200nF	10nF	Ideal: 708.3Ω E96 std. value: 715Ω	Ideal: 178.8Ω E96 std. value: 178Ω

The last stage in the cascade realisation is a first order pole formed by C_{c1} and R_{c1} to yield a 10kHz lowpass filter.

Design procedure: Chose C_c and calculate R_c from, $R_{c1} = 1/(2\pi * 10\text{kHz} * C_{c1})$. The final values are given in the table below:

Stage	C_{c1}	R_{c1}
1	47nF	Ideal: 338.6Ω E96 std. value: 340Ω

Sensitivities of Implemented Filter

From the previous discussed sensitivity equations, the sensitivity with respect to Q an ω_o for all stages was found as follows:

Stage	ω_o S_{R_a}	ω_o S_{R_b}	ω_o S_{C_a}	ω_o S_{C_b}	ω_o S_{R_c}	ω_o S_{C_c}	ω_o S_{A_1}	Q S_{R_a}	Q S_{R_b}	Q S_{C_a}	Q S_{C_b}	Q S_{A_1}
2	-0.5	-0.5	-0.5	-0.5			0	-0.2	0.2	0.5	-0.5	1.0
3	-0.5	-0.5	-0.5	-0.5			0	-0.2	0.2	0.5	-0.5	2.2
4	-0.5	-0.5	-0.5	-0.5			0	-0.2	0.5	0.8	-0.5	20.0
1					-1	-1						

Note the high Q sensitivity with respect to the op amp's unity gain accuracy in stage 4. The TLE2027's open loop gain of more than 60dB or 1000 at 10kHz, when loaded with the low impedance feedback network, gives however only a Q error of $20 * 0.1\ \% = 2\%$.

Noise Evaluation of Total Lowpass Filter

The equivalent noise resistance, r_n, of the TLE2027's typical input noise voltage, e_n, is given by:

$$r_n = \frac{e_n^2}{4\,k\,T} \cong 380\Omega\ ;$$

The equivalent noise conductance, g_n, of the TLE2027's typical input noise current, i_n, is given by:

$$g_n = \frac{i_n^2}{4\,k\,T} \cong 9.7\mu\text{Siemens}\ ;$$

Analysis of the noise current impact on the total output noise shows that it can be ignored with the chosen impedance level, hence it is left out of the calculations. Applying equation (5) on the individual 2nd order filter sections lead to a good approximation for the noise of the total 7th order Butterworth lowpass filter.

Notes

Stage 2. Ignoring contribution form g_n and assuming the stopband noise is completely removed by the succeeding filter stages, this section's contribution to the total output noise is given by:

$$e^2_{n\,out2} \cong 4kT\,(590 + 274 + 380)\,10 * 10^3 = 0.205 * 10^{-12}\ V^2;$$

Stage 3. Ignoring contribution from g_n and assuming that stopband noise is rolled off by 3rd order corresponding to a noise bandwidth of, $f_o * 1.05$, this sections contribution to the total output noise is given by:

$$e^2_{n\,out3} \cong 4kT\,(634 + 267 + 380)\,10 * 10^3 + 4kT\,380\,(1.05 - 1.00)\,10 * 10^3\ V^2;$$

$$e^2_{n\,out3} \cong 0.213 * 10^{-12}\ V^2;$$

Stage 4. Ignoring contribution from g_n and assuming that stopband noise is rolled off by 1st order corresponding to a noise bandwidth of, $f_o * \pi/2$, this sections contribution to the total output noise is given by:

$$e^2_{n\,out4} \cong 4kT\,(715 + 178 + 380)\,10 * 10^3 + 4kT\,380\,(\frac{\pi}{2} - 1.00)\,10 * 10^3\ V^2;$$

$$e^2_{n\,out4} \cong 0.245 * 10^{-12}\ V^2;$$

Stage 1. The noise of this stage comes from the thermal noise of the resistor, R_{C1}, which is band limited with a 1st order roll off given by R_{C1} and C_{C1}, hence this sections contribution to the total output noise is given by:

$$e^2_{n\,out1} = 4kT\,r_n\,\frac{\pi}{2}\,f_o \cong 4kT\,380\,\frac{\pi}{2}\,10 * 10^3\ V^2 = 0.088 * 10^{-12}\ V^2;$$

The total output noise of the filter, E_n can now be calculated from:

$$E_{n\,tot} = \sqrt{\sum_{j=1}^{4} e^2_{n\,out\,j}} \cong \sqrt{0.205 + 0.213 + 0.245 + 0.088}\ \mu V = 0.867\mu V;$$

In practise, a slightly higher noise level can be measured, as the simplified noise model don't hold for section 4 due to its relative high Q factor of approximately 2.25. This peak in section 4's transfer function results in increased noise around the filter's -3dB frequency. However, a total dynamic range in excess of 130dB can be achieved for this 10kHz, 7th order Butterworth lowpass filter.

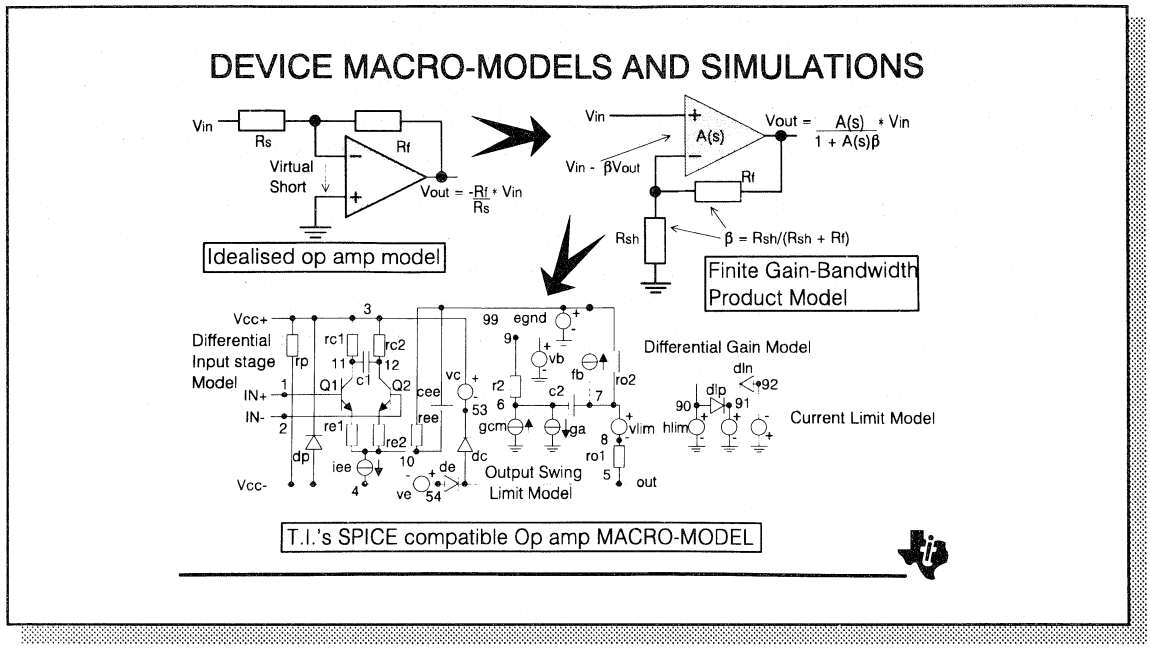

Figure 48 - Device Macro-Models and Simulations

Since the introduction of operational amplifiers, very much simplified models of their behaviour have been used to try and predict the output of the device when stressed with various forms of inputs.

The simplest of models is that of the virtual short between the inputs of the device. This assumes that the gain is infinite and has infinite input impedance. This model works reasonably well with high performance op amps with their high open loop gains of more than one million. It proves unsatisfactory when trying to consider other aspects in the performance of the op amp, such examples are the errors associated with its input and more importantly the device's frequency response.

For D.C. applications the high input impedance is normally a very good assumption, almost all op amps have impedances greater than 1MΩ and the gains frequently used, are low enough that the op amp is not used in open loop conditions. Taking into consideration all the offset

Notes

voltages and input bias and offset currents adds to the complications of the simplified model. Hence a more complete model has the virtual short across the inputs replaced with an offset voltage in series with the non-inverting input with biasing current sources connected to the inputs of the device. These are all D.C. effects, and can reflect the performance of the op amp reasonably well, but modelling most of the A.C. aspects of the op amp can be very difficult.

The op amp can be considered as operating as a low pass filter with enormous gain, the large gain minimises most of the low pass filter effects at low frequencies, but at higher frequencies these effects must be taken into account. The analysis can be made easier by use of the Bode plot, and relating the circuit's ideal gain to the op amp's actual gain. This will show the point where the open loop gain of the op amp takes over from the ideal gain.

The whole model can be improved by considering the feedback equation of any system:-

$$G_{CL} = \frac{A_{OL}}{1 + A_{OL}\beta}$$

Where G_{CL} is the closed loop gain, A_{OL} is the open loop gain and β is the feedback around the amplifier. Using this equation increases the accuracy of the model considerably but can also increase the complexity to beyond that of pen, paper and calculator, especially for systems using several op amps. The difficulty of A.C. analysis is compounded by operating the op amp with large signals, which can drive the device out of its assumed linear mode.

With the advent of modern day computers a much simpler way of analysing op amp circuits has arrived: Macro-models of the op amps. The macro-model is a simplified model of the op amp taking into account all of its key parameters. Texas Instruments has released macro-models of all its op amps and these are capable of operating with a wide variety of simulation packages, one example is Microsim's PSPICE™.

The macro-model is a derivative from Boyle's model, which uses real transistors to model the actual input stage of the op amp. The following stages via the input stage model the gain and its roll-off over frequency, along with bias current errors and further ac and dc limitations. Each of the parameters are derived from the specifications of the op amp and so simulate the performance of op amp to a much higher level of accuracy than the designer with only a pen and paper can. The macro-models, as with most things, provide a compromise between optimum performance with simulating speed, cost and ease of use. A full model of the device will give a better representation of the device but would take much longer to simulate and would also cost considerably more.

Plus another thing to consider is than no op amp manufacturer releases full spice simulation models of their devices, however, Texas Instruments has now released a Macro-Model Data Manual. This contains a Macro-Model for each of its op amps, except for the latest products which contain the model within their datasheets.

SECTION 3 .
DATA TRANSMISSION

DATA TRANSMISSION INDEX

Introduction

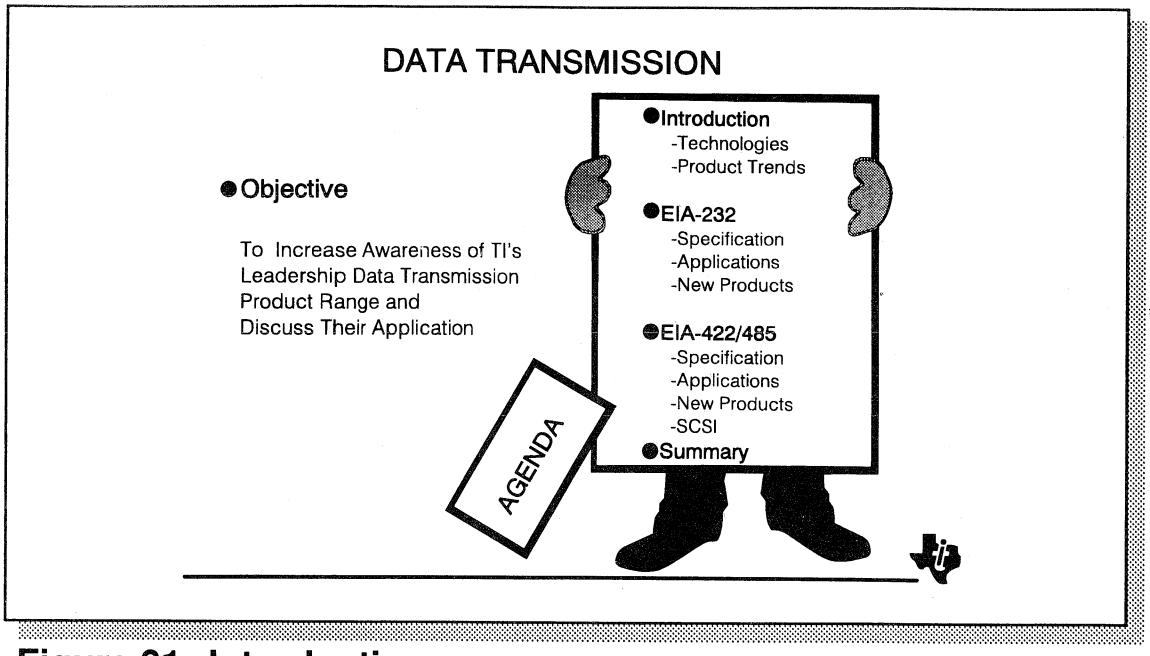

Figure 01 - Introduction

The following sections focus on a range of data transmission products supported by the linear department of Texas Instruments.

The requirement for specialised data transmission products originally arose from the need to send data over long lengths of cable, in conditions often susceptible to noise interference. Although TTL products can be used, they are far from ideal, and over the last ten years products optimised for the task of data transmission have been developed. These devices characteristically yield greater current output drive capability and/or wider operating voltage ranges, thereby offering improved noise immunity. Furthermore, Speed, power consumption and high levels of integration and robustness are becoming standard requirements.

With their considerable expertise in design and their range of technologies, Texas Instruments is the ideal choice as semiconductor vendor for data transmission products.

Texas Instruments has been a leading supplier of interface products for many years, and as you might expect is continually innovating new fields. Although the following sections are limited to the more common interface standards, TI is actively involved in many new emerging standards and markets. Such markets include; high performance backplane standards (IEEE.896 futurebus+), Home Automation, automotive multiplex wiring, Ethernet™ and custom design engagements. The reader is advised to consult the accompanying literature sheet or contact a TI representative for information on these product areas.

The following pages take a practical rather than theoretical approach, and attempt to give the practicing engineer a quick overview of products available for several of industries most commonly used standards; namely the Electronics Industries Association's (EIA) serial standards, EIA-232, RS-422 and RS-485. In each case the standards specification and it's merits are briefly discussed followed by overviews of Texas Instruments' key products and their application. To further aid the reader a glossary section contains information on transmission line fundamentals, a data transmission trouble shooting guide and a Small Computer Interface tutorial. Although both the EIA-232 and RS-422/485 sections contain a product selector the **1991 interface circuits data book** should be consulted for more comprehensive information.

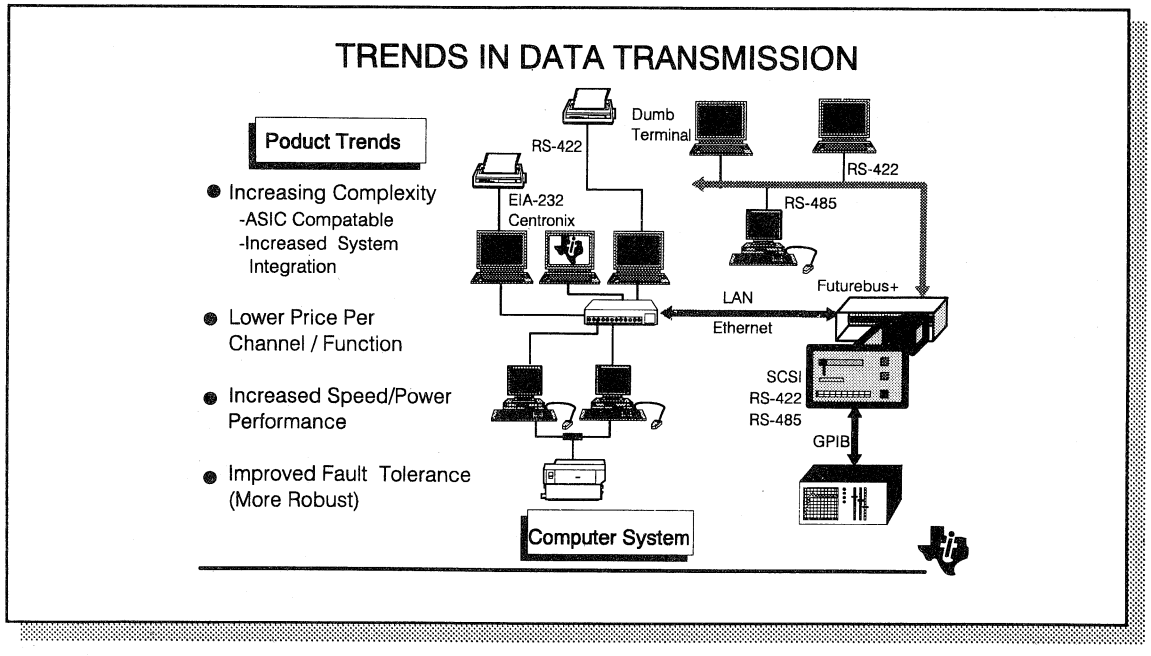

Figure 02 - Market Trends

The primary objective of any data transmission system is the distribution of information without error. Data transmission circuits are chosen primarily on the data rate, distance to be covered and system cost, whilst compliance with industry standards is necessary to maintain system compatibility.

Notes

This figure shows just one example of a data transmission network. It shows many different types of interconnect within a computer system. Although all are concerned with the exchange of data, the data transmission scheme used, types of cable and system capabilities vary enormously.

Parallel or Serial? / Single Ended or Differential?

Transmission schemes may be broken into two main categories, parallel or serial systems. These categories may be further classified by the type of interface circuitry used; Single ended or differential ended.

Differential techniques are generally used when noise interference could be problematic or when long distances are to be covered at high data rates. **Single ended** techniques are used when cost is an issue or where short distances are to be covered, this is typified by board level logic, back plane systems or short data link applications.

Parallel systems are generally used when large amounts of information are to be transmitted over relatively short distances but at high speed (parallel systems generally require one line or cable per digital bit.). The backplane or board level bus is the most general and widely used of the parallel bus types. Other examples are the microprocessor specific Multibus™ and VMEbus™. However, increasing need for even higher backplane data rates and optimised flexibility without being tied to a specific microprocessor architecture is solved by the rapidly emerging standard **Futurebus+**. SCSI (Small Computer System Interface) is also a parallel bus structure with increasing use for data transfer between PC/Workstations and memory storage systems including Winchester hard disk drives.

Finally, IEEE488 allows parallel data transmission between measuring equipment and the PC, thus allowing the user to set up automatised test routines.

Serial busses find their applications in longer length data transmission systems where the cost of running parallel cables would be cost prohibited. The most widely used, and known, serial data transmission standard is the EIA-232. Although originally developed for modem to terminal equipment interface it is widely used as an interface for nearly all PC peripherals. For longer line lengths and better noise immunity the serial buses RS-422 and RS-485 are preferred. The bidirectional RS-485 is a popular standard becoming extensively used in multi-station, high data rate applications - especially because of its close links to SCSI.

At the longest line length level are Local Area Networks (LAN), like Token Ring and Ethernet. TI has recently introduced a transceiver function to address the requirement of the Ethernet repeater function, with development well under way for a whole series of devices.

Other types of LANs can be found within the factory, factory automation, for interconnecting process controllers and sensors. On such developing standard is Fieldbus, which embraces electrical specifications as well as protocols.

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Other types of LANs can be found within the factory (factory automation) for interconnecting process controllers and sensors. On such developing standard is Fieldbus, which embraces electrical specifications as well as protocols.

Home Automation a domestic LAN is a growing area for future data communication. A standard like CEBus (Consumer Electronics Bus) is an example of a bus structure including more that just the electrical specification. The specification includes a robust protocol of interconnecting consumer appliances to form an intelligent network opening up a world of new possibilities in the home.

Also considered a key growth market is that of automotive multiplex wiring. The need for very robust and fault tolerant driving/receiving elements is never so apparent as in automotive applications, especially when used in safety critical systems. Emerging automotive standards like CAN, Controller Area Network, VAN and the U.S. S.A.E. J1850 standard are set to play a key part in this area.

Protocols are needed as well

The majority of the text in this section is concerned with the electrical aspects of the interface. However every interface needs some form of control, which provides a set rules to define the meaning and order in which data should be sent (this is dealt with briefly in the EIA RS-485 section). Termed protocols these rules can be implemented by the microprocessor, or increasingly by a dedicated communications controllers. In the past the electrical specifications have been kept separate from the protocol (which have usually been left to the systems engineer to devise) the consequence of which is system incompatibility. The trend today is to produce an all-embracing standard which covers, electrical, mechanical and logical (protocol is contained in this group) specifications. Examples of this can be found in many of the standards just highlighted.

The underlining requirements demanded by some if not all of these applications can be summarised;

i) Increasing complexity / Higher Systems Integration

The consumers ever increasing demand for improvements in system performance coupled with weight/size/cost reductions, lower running costs and reliability has led to a demand for more complex semiconductor chips. This is bourne out by considering almost any system, particularly in the computer industry, where whole functions are mopped up into ASIC's (Application Specific Integrated Circuits) or highly system integrated processors. For example a minimal microcomputer architecture requires a central processor, memory (RAM and ROM) and input/output (I/O) control , previously this would require several chips it now can be implemented in just one- the single chip micro. The interface circuitry is no exception,

Notes

consider the asynchronous communication element (ACE) which controls the serial interface between computer and peripherals. This has migrated from a multi-chip solution to a single dedicated controller, controlling up to 2 serial ports and one parallel port (TL16C552). It is quite clear that before long line driving/receiving functions will also be integrated along with the controller chip.

ii) Robustness

By including more functions on chip the system chip count is reduced, not only bringing benefits in terms board real estate savings but in system reliability. However, should a fault occur the increased complexity of these chips has made the task of fault identification more difficult, especially for the field service engineer. This has led to more robust design techniques and the inclusion of self test and diagnostic capabilities being included on chip. For example the SN75186 EIA-232 driver/receiver contains a loopback feature allowing self test and the futurebus+ chip set which will include JTAG capability.

iii) More functions Lower Price

Individual chips are now capable of performing tasks previously undertaken by several. However, from the chip manufacturers point of view, seldom will the price charged for this increased functionality be greater than the solution(s) it replaced.

The line drive/receive functions are also under price/function pressure. Particularly as integration increases from a single drive/receive cells to as many as six per device, system designers will not tolerate a six fold increase in price!.

iv) Increased speed/power performance

The old adage, 'You can't have high speed and low power' is no longer acceptable. High performance systems are now required either to operate permanently or temporally from battery cells, thus demanding low power consumption.

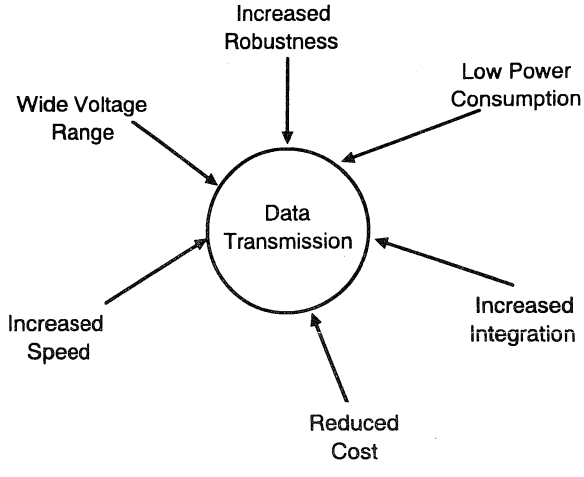


Figure 2a - Pressures on Data Transmission Products

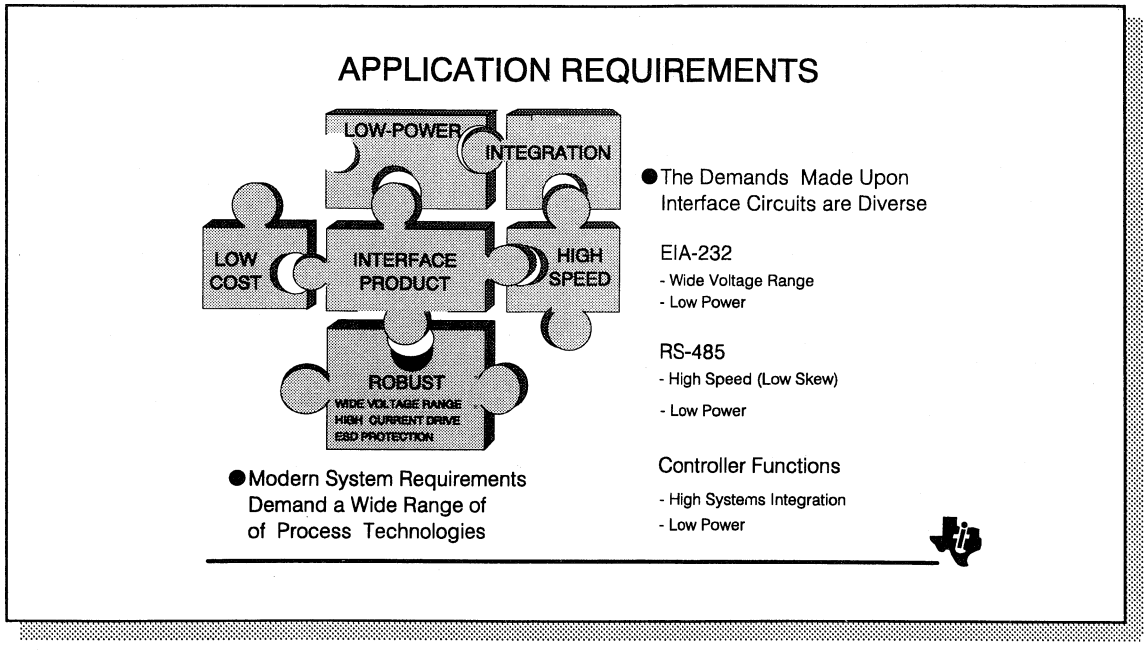


Figure 03 - Application Requirements

The diverse range of applications and the markets demand for increased functionality , robustness and low power, requires a broad range of technologies. Furthermore the choice of the most appropriate technology is not a trivial matter as needs are often conflicting, ie high speed and low power. However, the dominating factors are usually speed and voltage operating range. Although the list of technologies to choose from is seemingly endless, several key categories emerge with all others variation slight process modifications. The categories are;

i) Analogue Bipolar (operational amplifiers)

ii) Analogue CMOS (LinCMOS range of operational amplifiers)

iii) Digital CMOS (HCMOS '74 range)

iv) Digital Bipolar ('LS74 range)

Notes

Broadly speaking bipolar technologies offer speed and robustness, whilst CMOS technologies provide low power consumption and high packing density. The analogue process variations offer increased robustness often at the sacrifice of packing density. There are of course exceptions to every rule.

The following case studies highlight some of the key technologies and their suitability for a given application and function.

Controller Functions

Controller functions usually present a simple technology choice. The major requirements, irrespective of application, are for low power consumption and high integration. Robustness is not generally a major concern as the device is usually tucked safely away in the bowels of the equipment. High integration is important as systems designers strive to reduce chip-count hence saving board space and increasing reliability. This requires a technology with high packing densities and small geometries. A digital CMOS process, of which there are many variations, with 1µm geometry is the ideal choice.

i) EIA-232

EIA-232 is a single ended, serial standard commonly used to connect the computer to its peripherals, eg printer. Although it has a relatively slow data rate, 20kbaud, and can only be used only over short distances,<15 m, it is very low cost and easy to implement.

By far the most demanding requirements for the EIA-232 line drive/receive circuits is the ability to operate from dual supplies of up to ±15 V. As with all interface devices a high degree of robustness is demanded. Implementing on-chip ESD and transient protection circuits which can operate within such wide voltage ranges is difficult . The natural choice would be a wide voltage bipolar technology with its inherent robust structures (commonly used by operational amplifiers). In fact the vast majority of industry standard devices for EIA-232 have been designed using this process. However modern equipment increasingly requires battery operation (lap top PC's and hand held test equipment) thus low power consumption is also required. Generally a low power digital CMOS process would be incapable of withstanding the wide voltages required therefore a low-power bipolar or mixed bipolar and CMOS process (merged technology) is needed.

ii) Differential Applications

Termed a multi-point standard or mini LAN (Local Area Network) RS-485 allows up to 32 driver/receivers to be connected to a single line. The standard is fully differential, permitting greater line lengths (up to 1200m) at high data rates (up to10Mbaud) to be driven.

Since the cable travels long distances signals becomes very susceptible to cross talk and EMI, which although greatly reduced by the differential nature of the line, robust devices with wide voltage operation are still needed. High speed and low power are also major requirements, making a low-power bipolar technology with high speed transistors the logical choice. Such a technology is the Advanced Low Power Schottky process (ALS). For applications requiring further power reductions, particularly telecommunications, a mixed

bipolar and CMOS process would be needed. Generally a digital CMOS process would be incapable of handling the wide voltage common mode range of -7V to +12V for RS-485 applications.

iii) Futurebus+

Futurebus+ is a high performance standard for computer backplanes. A backplane is the main communications highway between the CPU and option cards. It allows the CPU to exchange data, status, address information with its sub system modules (memory, co-processors etc). The demands made by futurebus+ on processing technologies is enormous. Firstly it needs highly complex controller circuits to take care of bus arbitration and protocol control, and secondly it requires high speed low power transceiver functions to drive the backplane.

Backplanes are particularly difficult to drive, particularly as each card plugged into the system contributes a capacitive load to the system, thus requiring greater current from the drivers output stages.. Consequently devices with high current drive capability are needed, 80 to 100mA for futurebus+. As the voltage swing of a futurebus+ transceiver is only 2 volts then the wide voltage ranges offered by the analogue technologies are not required. A merged digital merged process could be used. This would also offer low power, which could be a significant factor when considering the number of devices required for a 32 bit+ bus.

The above case studies demonstrate that a serious supplier of data transmission devices needs to have a broad range of optimised technologies as well as merged technology capability.

Key Technologies

Although a detailed discussion of technologies is beyond the scope of this book, it is worthwhile briefly considering the key technologies and the benefits they offer for data transmission applications.

Until recently, semiconductor technologies used to manufacture line interface circuit devices have been based upon those technologies and processes used to build digital logic circuits. This resulted in circuits having mainly bipolar NPN structures. For example the change from ordinary bipolar to low power schottky (LS) and advanced low power schottky (ALS) technologies in digital logic devices, was closely followed by line circuit devices.

Notes

In recent years there has been a change in the digital logic field towards device structures based upon CMOS processes. CMOS offers the obvious attractions of low quiescent power consumption and operating speed comparable to that of many bipolar technologies. The same change in technology for line circuits has not been so fast. One of the primary reasons for this is the need to make output transistor stages very large in CMOS technology to enable them to source the required high currents (as much as 250 mA). The input capacitance of these large CMOS stages also require much higher drive currents from the bias circuits. At high frequencies of operation CMOS line circuits therefore lose some of their attraction because bias currents become so high. It is also difficult to build CMOS devices that could withstand the relatively high voltage levels used by some slower, older line interfaces, for example EIA-232. CMOS is particularly problematic when the externally applied voltages are taken outside its supply rails. This causes a phenomena called 'latch-up' to occur, and is due to a parasitic diode structure in parallel with the output transistor. Latch-up causes the device to draw increasing amounts of current until the device self destructs.

The most promising route forward in technology for line interface devices would appear to be through the use of a BiCMOS technology (a mixed digital CMOS and digital bipolar process). Such progress has again already been made in the digital logic field. BiCMOS technology combines the speed and high voltage capability of bipolar processes with the low supply currents and high input impedances of a CMOS process. This is now to available for line interface circuits with the development of the AM26C31/32. See the RS-422 section for performance comparisons. Another merged technology is the analogue LinBiCMOS process which combines an analogue bipolar process with an analogue CMOS process. Thereby enabling devices which are not only low power but are now extremely robust and have high speed capability.

The LinBiCMOS process is set to be a major technology for TI's new data transmission products, allowing bipolar high voltage capability to be merged with high density low power CMOS.

Another key advantage of the merged technologies is that generally they use a cell based approach For example cells developed for one device can be added quite easily to other devices. Thereby reducing device development time and increase the number of device options available.

A brief resume of Texas Instruments' key data transmission technologies is given below;

	OP-AMP	LS	ALS-Impact	EPIC -1A	IMPACT-CS	EPIC-IB/2B	**LinBiCMOS**
Process	Bipolar	Bipolar	Bipolar	CMOS	BiCMOS	BiCMOS	BiCMOS
Class*	i)	iv)	i)	iii)	iii) +iv)	iii) + iv)	i) + ii)
Geometry	10 µ	5 µ	2 µ	1.2 µ	1.5 µ	0.8 µ	2 µ
Application	EIA-232, RS-422 RS-485	RS-422 RS-485	RS-422 RS-485	Control	RS-422	Control	EIA-232, RS-422 RS-485
Voltage	30V	15V	15V	5V	15V	5V	30V
Introduction	'75	'77	'85	'88	'88	'88	'90

Notes:
Not listed in the box above is Texas Instruments' BiMOS process. This process is a derivative of a bipolar process with enhanced PMOS devices giving extremely low power. For example a power saving of 99% can be made over existing bipolar designs.

** See previous list for classifications*

Although the requirement for optimised proceses will continue, the trend towards merged technologies like LinBiCMOS will gain mommentum, especially when little or no compromise is encountered.

Notes

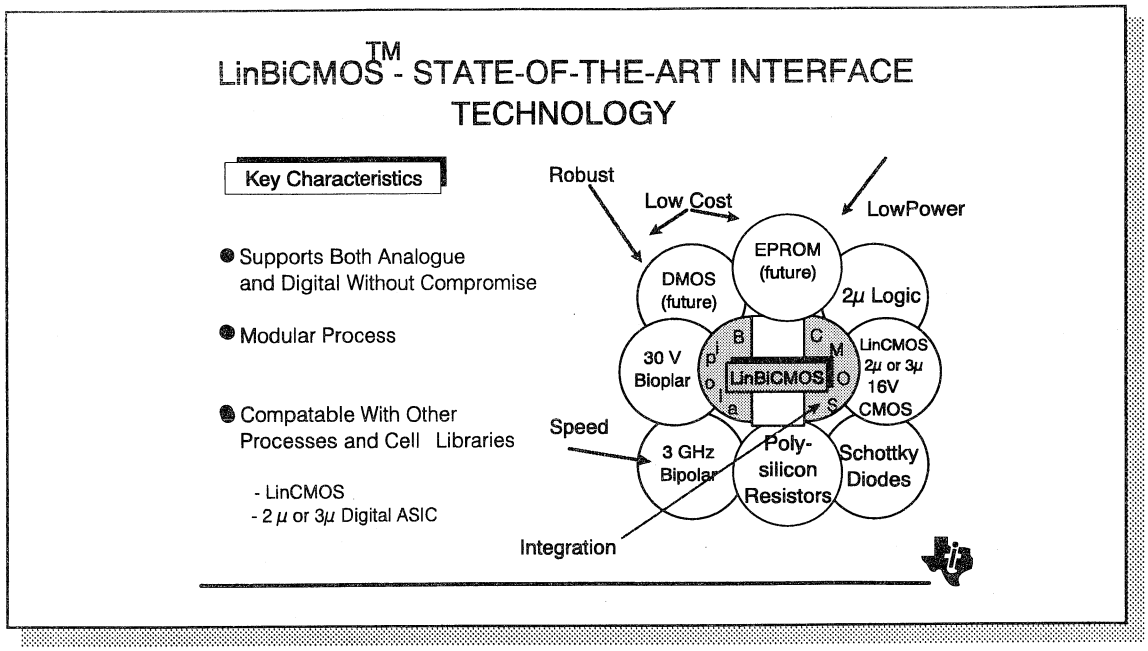


Figure 04 - LinBiCMOS, State-of-the-art interface technology

Although originally developed as a technology for designing mixed analogue/digital ASICs, LinBiCMOS now looks set to make a major impact in the field of interface devices.

LinBiCMOS is based on TI's highly successful LinCMOS process. LinCMOS is a 3μm pure CMOS technology with 16V capability, making it ideal for the design of low power analogue products such as op-amps and analogue-to-digital convertors (many examples of which are discussed elsewhere in this book). By shrinking the geometries to 2μm and adding a high performance 30V bipolar structure, a new "analogue" merged bipolar/CMOS technology has been produced.

Probably LinBiCMOS's greatest attribute is its modularity. When generating a new technology it is difficult to achieve a balance between performance and cost, as many "nice to have" features can make a process too expensive to address a wide range of opportunities. By making LinBiCMOS modular, only the process modules needed to address a particular application need be used, making it very cost effective.

Modules available for LinBiCMOS include high speed NPNs (with an f_T of 3GHz compared with 500MHz for the standard transistor), double level metal for better logic integration and current handling, isolated high value polysilicon resistors and schotttky diodes for clamping.

Another key benefit of LinBiCMOS is its compatibility with TI's ASIC 2μm logic cell library. This means that any logic required within a new design can be quickly designed and simulated as each of the cell are already very well proven.

By combining bipolar with CMOS it is possible to use each structure to its best advantage. CMOS is ideal for designing logic and for interfacing with external logic devices (controllers etc) whereas bipolar is well suited to high voltage/current areas such as the line output stage.

With its high voltage capability and good switching speed, LinBiCMOS is ideal to address standards such as EIA-232 and RS485. The RS485 standard for instance, demands that driver output can be shorted to +12V and -7V without damage, which is particularly difficult as only a single 5V supply is available, meaning that parts of the chip must be designed to operate well outside of its supply rails.

Development work on LinBiCMOS is still underway, and in 1991 TI expects to offer DMOS and EEPROM modules. EEPROM (electrically erasable programmable memory) offers some very exciting opportunities such as line driver/receivers with their own built in address.

To date LinBiCMOS has only been used for custom IC developments, but in 1991 several new interface catalogue products including a dual driver/receiver with on-board charge pump for single rail EIA-232 applications will be released.

Notes

The EIA and IEE Interface Standards

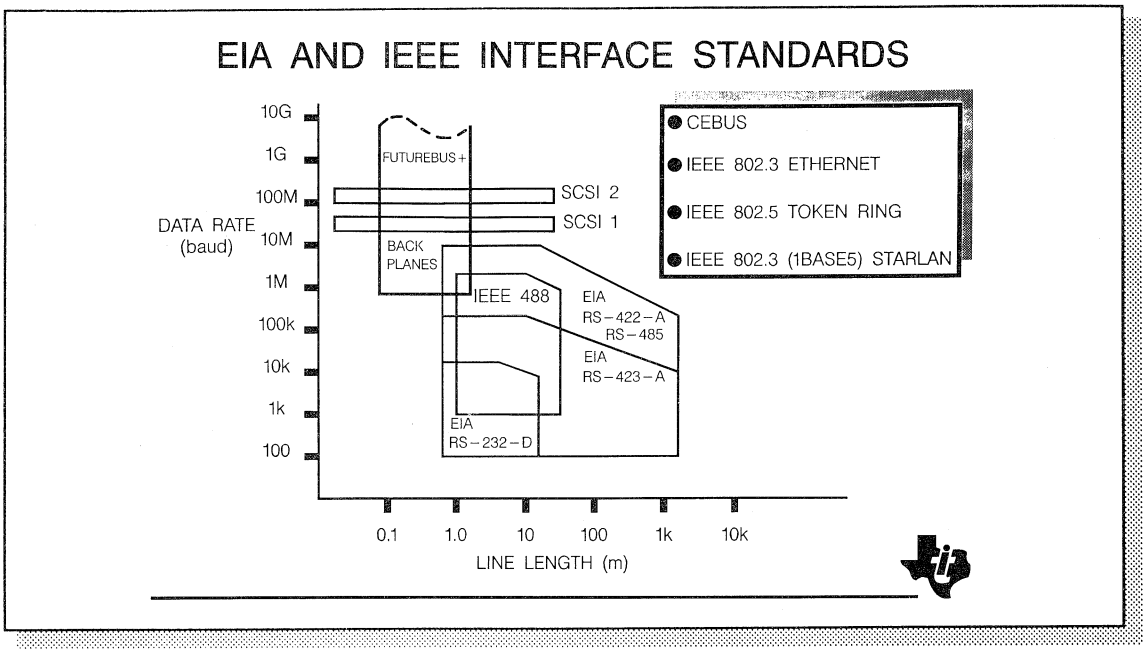


Figure 1A- EIA and IEEE Interface Standards

There are a wide range of standards available for implementing digital data links. Some are very sophisticated like the Consumer Electronics Bus, for home automation, and futurebus+, high performance backplane. These embrace specifications for protocol (timing and control) as well as the electrical and mechanical aspects of the interface. Others, such as the EIA-232 interface contain only basic timing information while the RS-422 and RS-485 specifications contain only electrical information.- although the timing and control of the interface still needs careful consideration.

The choice of standard is made primarily on the distance and data rate to be covered with environmental constraints also a key governing factor. The EIA was among the first to recognise that industry needed standard guide lines from which to design. Prior to standardisation there was (and still will be) a whole plethora of propriety interface standards, most of which are incapable of communicating not only with other vendors equipment but in some cases with their own!. Obviously this caused problems for the end user, since they became locked into specific manufactures making their choice for add-on boards/software or upgrades severely limited.

Although TI is involved in the manufacture of a wide range of products for many standards, shown in the figure and discussed previously, only the more commonly used standards have be chosen for further discussion.

These standards are the serial single ended EIA-232 and the serial differential bus standards RS-422 and RS-485. Since the RS-485 standard is referenced as the electrical specification for many other standards, these where appropriate will be briefly discussed also, ie the ANSI Small Computer System Interface, SCSI.

The following table gives a summary of the common EIA standards;

PARAMETER		EIA-232	RS-423-A	RS-422-A	RS-485
Mode of Operation		Single-Ended	Single-Ended	Differential	Differential
Number of Drivers and Receivers		1 Driver 1 Receiver	1 Driver 10 Receivers	1 Driver 10 Receivers	32 Drivers 32 Receivers
Maximum Cable Length (m)		15	1200	1200	1200
Maximum Data Rate (baud)		20k	100k	10M	10M
Maximum Common Mode Voltage (V)		±25	±6	6 to -0.25	12 to -7
Driver Output Levels(V)	Unloaded	±5	±3.6	±2	±1.5
	Loaded	±15	±6	±5	±5
Driver Load (Ω)		3k to 7k	450(Min)	100 (Min)	60(Min)
Driver Slew Rate		30V/µs(Max)	External Control	NA	NA
Driver Output Short Circuit Current Limit(mA)		500 to V_{CC}	150 to GND	150 to GND	150 to GND 250 to -7 or 12V
Driver Output Resistance- High Z State (Ω)	Power On	NA	NA	NA	12k
	Power Off	300	60k	60k	12k
Receiver Input Resistance (Ω)		3 to 7	4	4	12
Receiver Sensitivity		±3V	±200mV	±200mV	±200mV

Notes

Single Ended Data Transmission Standards

EIA-232-D Specification

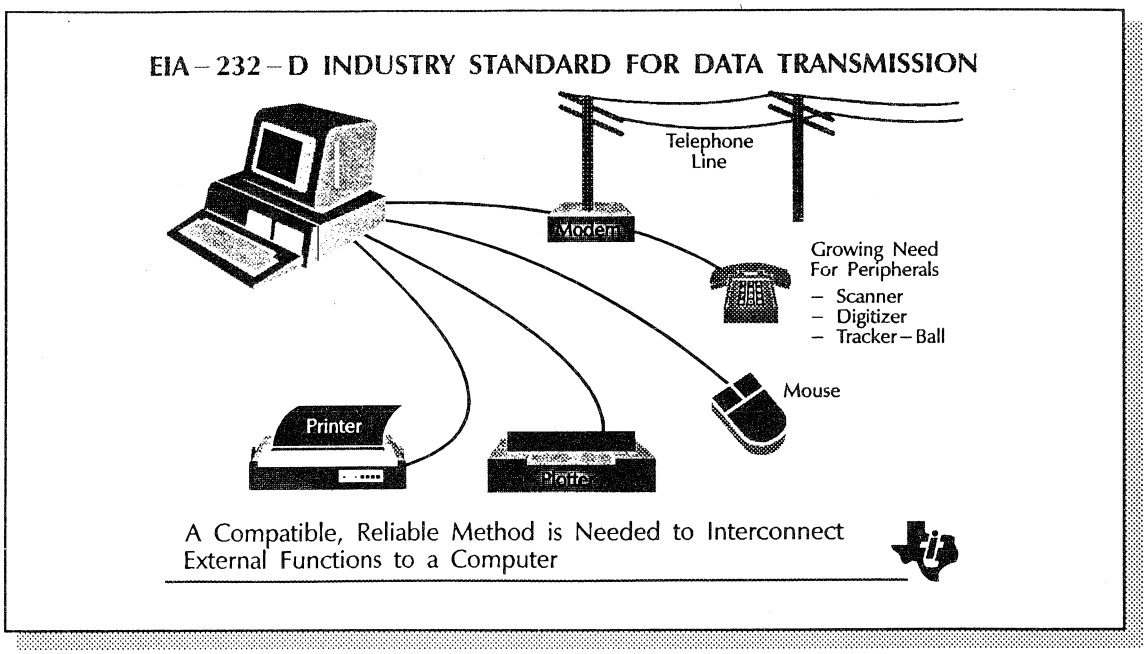


Figure 01 - EIA-232-D Industry Standard For Data Transmission

The Electronic Industries Association (EIA) introduced the EIA RS-232 standard in 1962 for the purpose of standardizing the interface between Data Terminal Equipment (DTE) and Data Communication Equipment (DCE).

Although emphasis was then on interfacing between a modem unit and a data terminal equipment, this standard is also applicable to serial binary interfacing between various types of data terminal equipment.

The growing use of PCs has created many new EIA-232 application areas. Namely the EIA-232 standard has been adopted as the low cost interface to peripherals such as the mouse, plotter, scanner, digitizer, printer and tracker-ball in addition to the modem unit.

Using a common standard allows widespread compatibility plus a reliable method for interconnecting a PC to peripheral functions.

The revised standard of 1969, EIA RS-232-C has now been superseded by EIA-232-D (1986) which brings it in-line with CCITT V24, V.28 and ISO IS2110. The latest revision reflects the addition of mechanical specifications for the interface connector, loopback and test modes as the major changes.

Although an "old" standard with problems like high noise susceptibility, low data rates and very limited transmission length, EIA-232 provides a low cost communication solution and new products are being developed with a rate faster than ever.

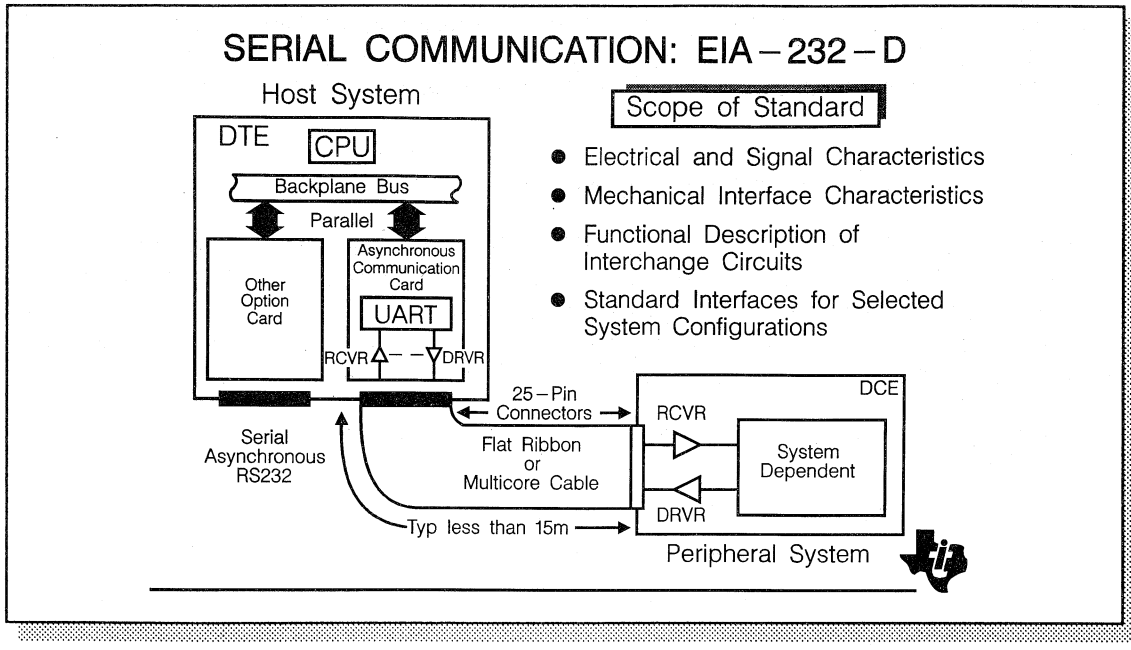


Figure 02 - EIA-232-D Serial Communication

Scope of Standard

i) Electrical and Signal Characteristics

Electrical and signal characteristics of the signals and associated circuitry in terms of signal levels, impedances and rates of change.

ii) Mechanical Interface Characteristics

Mechanical Interface Characteristics defined as a 25-way "D" connector, with dimensions and pin assignments specified in the standard. Although the standard only specifies a 25 pin D type connector, most laptop PCs, today, use a 9 pin "DB9S" connector.

Notes

iii) Handshake Information

Functional Description of the Interchange Circuit which enables a fully interlocked handshake exchange of data between equipments at opposite ends of the communication channel. However, V24 defines many more signal functions than EIA-232, but those that are common are compatible. 22 of the 25 connector pins have designated functions, although few, if any, practical implementations use all of them. The most common used signals are:

SIGNAL GROUND (7) - Interface ground reference

TRANSMITTED DATA (TX) (2) - From the DTE to the DCE. Data must be transmitted only when REQUEST TO SEND, CLEAR TO SEND, DCE READY, and DTE READY are all in the 'ON' state (positive interchange voltage). A common reason why "standard" EIA-232 devices fail to work together is that one device implements only some of these four handshake signals, but the other is expecting them all.

RECEIVED DATA (RX) (3) - From the DCE to the DTE.

REQUEST TO SEND ($\overline{\text{RTS}}$) (4) - The DTE telling the DCE it wants to transmit. Also used to control direction of communication in half duplex system.

CLEAR TO SEND ($\overline{\text{CTS}}$) (5) - The DCE telling the DTE, in response to REQUEST TO SEND and its own ready condition, that the DTE may transmit.

DCE READY ($\overline{\text{DCR}}$) (6) - The DCE telling the DTE that it is connected to a communications channel and all dialling, talking, testing etc is over. (Also called Data Set Ready.)

DTE READY ($\overline{\text{DTR}}$) (20) - The DTE telling the DCE that it is ready to transmit or receive data.

RECEIVED LINE SIGNAL DETECTOR ($\overline{\text{DCD}}$) (8) - The DCE telling the DTE that it is receiving valid signals over the channel. Sometimes called Carrier Detect.

RING INDICATOR (RI) (22) - The DCE telling the DTE that a ringing signal is being received on the communication channel. (Used in auto-answer systems.)

iv) Standard Interface Connections for Selected Equipment Configurations

Standard Interfaces for Selected System Configuration outlining the use of interchange signals for different applications.

Note, that EIA-232 has not been optimised as a standard for interface between computers and printers, although it often is used as such (this explains the multitude of pin designations). Also, EIA-232 is not only limited to asynchronous communication . In fact it

contains provisions for synchronous communication if desired. EIA-232 does not specify a communication format. The good old "one start bit, eight data bits and two stop bits" is not a part of the standard, although it is the most common application. Finally, EIA-232 is a single ended transmission standard where only one receiver is connected to each driver. Recently developed devices (LT1080 and LT1030 from Texas Instruments) with tri-state driver and receiver outputs allow for multiple access to a single line, but there is no provisions for local area networks in the EIA-232 standard.

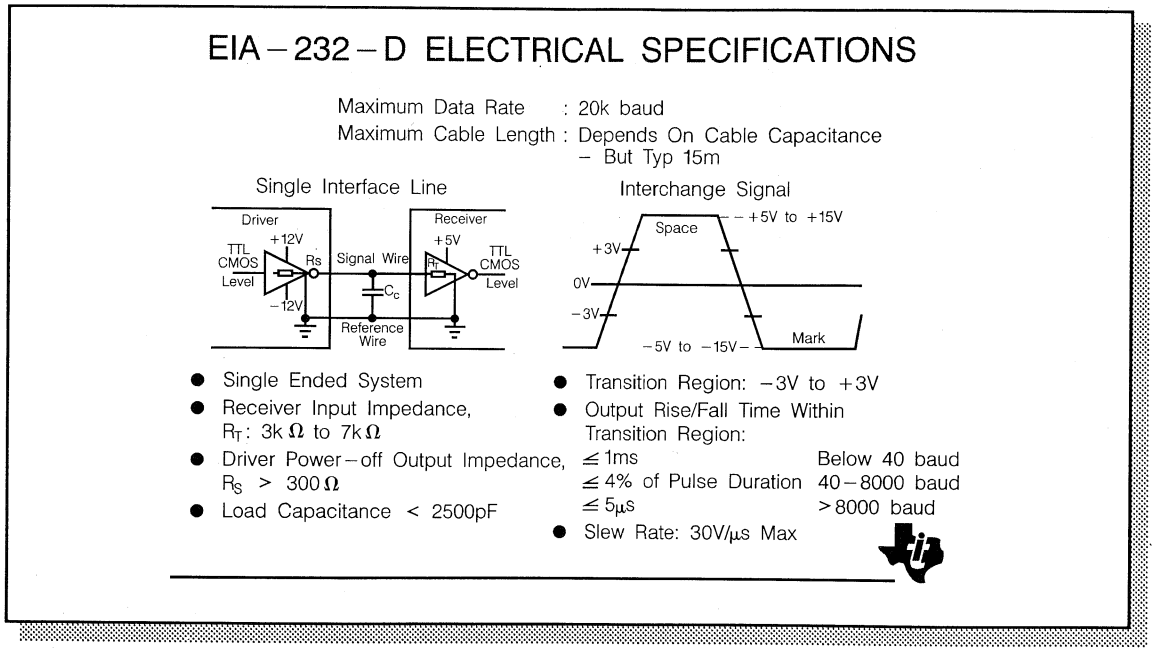


Figure 03 - EIA-232-D Electrical Specifications

Data transmission using EIA-232 is relatively slow. The EIA-232 standard specifies a nominal upper limit for the data signalling rate of 20,000 bits per second (20kbaud). Transmission line effect at such data rates and short line lengths can be ignored, hence load resistance and capacitance can be regarded as lumped parameters.

Some applications use however data rates well beyond the recommended maximum of 20kbaud but faster transmission standards such as RS-423, RS-422 and RS-485 must be recommended.

Notes

The cable length as specified in RS-232C is to maximum 15metres. A limit on the cable length is not specified in the 'D' revision, but rather a maximum load capacitance of 2500pF. As the typical cable capacitance is in the order of 150pF/m, then the maximum cable lenght is generally around 15m. The combination of the driver's output current capability, the load capacitance (cable length) and the standard's switching requirements should be considered in every design. This is particularly true when conforming to the more stringent CCITT V.28 specification.

A driver converting a TTL/CMOS signal to EIA-232 levels is usually supplied from +/-12V. A receiver converting EIA-232 levels to TTL/CMOS levels requires only a single +5V supply. The receiver input impedance, specified to be in the range from 3k to 7kΩ, combined with the signal levels dissipate considerable power - even if no transmission takes place.

A receiver treats a signal above +3V as a logic zero, a "space" or an "ON" condition. A signal below -3V is treated by the receiver as logic one, a "mark' or an "OFF" condition. The band between -3V and +3V is the transition region. The generator or driver must provide a minimum of +5V and a maximum of -5V at the interface point (any point between driver and receiver).

EIA-232 is a single ended transmission system and as such makes the transmission line susceptible to induced noise and common mode signals. Additionally, single ended systems can radiate Electro Magnetic Interference (EMI) and switching noise (cross talk) into adjacent systems. The latter effect, cross talk, can be minimised by limiting the period of time the signal can stay within the transition region; This time is dependent upon the data rate and reduces susceptibility to noise during transitions as well providing a defined signal for asynchronous applications. A maximum dV/dt of 30V/µs minimizes cable crosstalk, high frequency switching emission and interference with other signals.

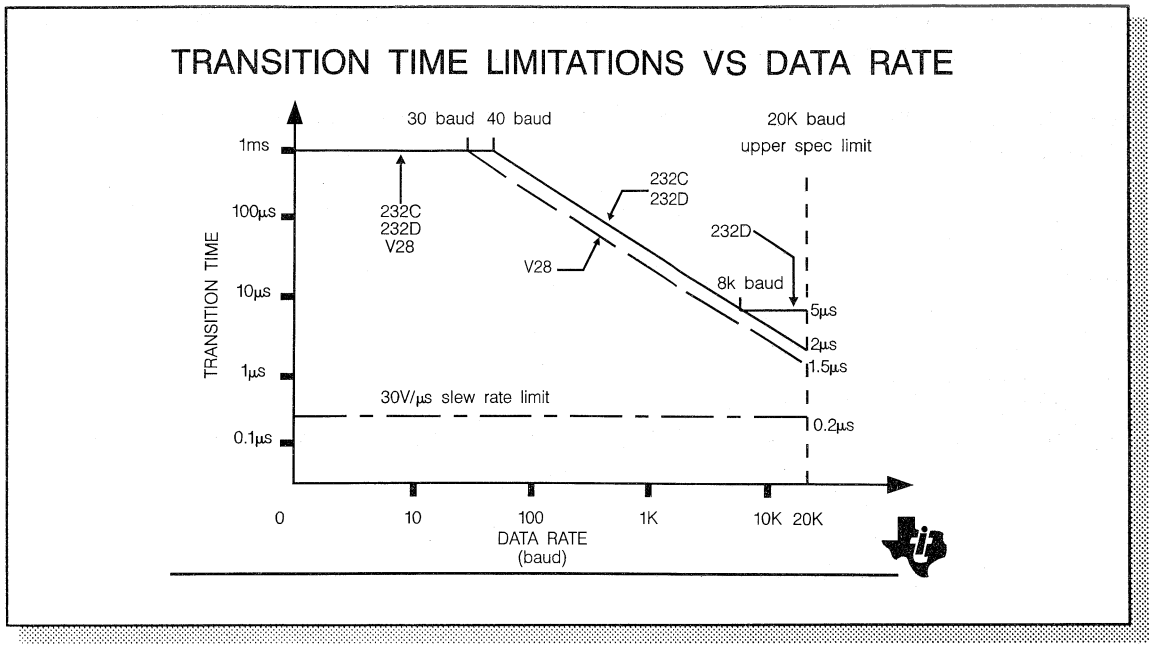


Figure 04 - Transition Time Limitations vs Data Rate

The figure shows the time required for data and timing signals to pass through the -3V to +3V transition region versus data rate for the standards: EIA RS-232-C, EIA-232-D and CCITT V.28. The 30V/us maximum slew-rate and the upper data rate of 20kbaud limit are also added, restricting the signal transition to a well defined area. The transition time for control signals should not exceed 1ms.

Note that the requirements of the CCITT specification V.28 are stricter than either revisions of "232". V.28 states that "the time required for a signal to pass through the transition region during a change should not exceed 1ms or 3% of the nominal element period on the interchange circuit, whichever is less".
RS-232-C allows the transition time to be 4% of the duration of a signal element. EIA-232-D represents a relaxation at data rates above 8kbaud where the maximum transition time becomes flat at 5µs. This means that all devices meeting V.28 and RS-232-C will also meet EIA-232-D.

Notes

The practical implications of these timing limitations relate the driver's maximum output current to the maximum cable length at a given data rate.

A basic equation can be derived to calculate the necessary driver output current for a given data rate;

$I = C\ dv/dt$

Where;

I = Current limit (min)
C = Cable capacitance
dv = Transition region (-3v to +3V = 6V)
dt = 3 or 4% of nominal element period depending upon standard (Previously described)

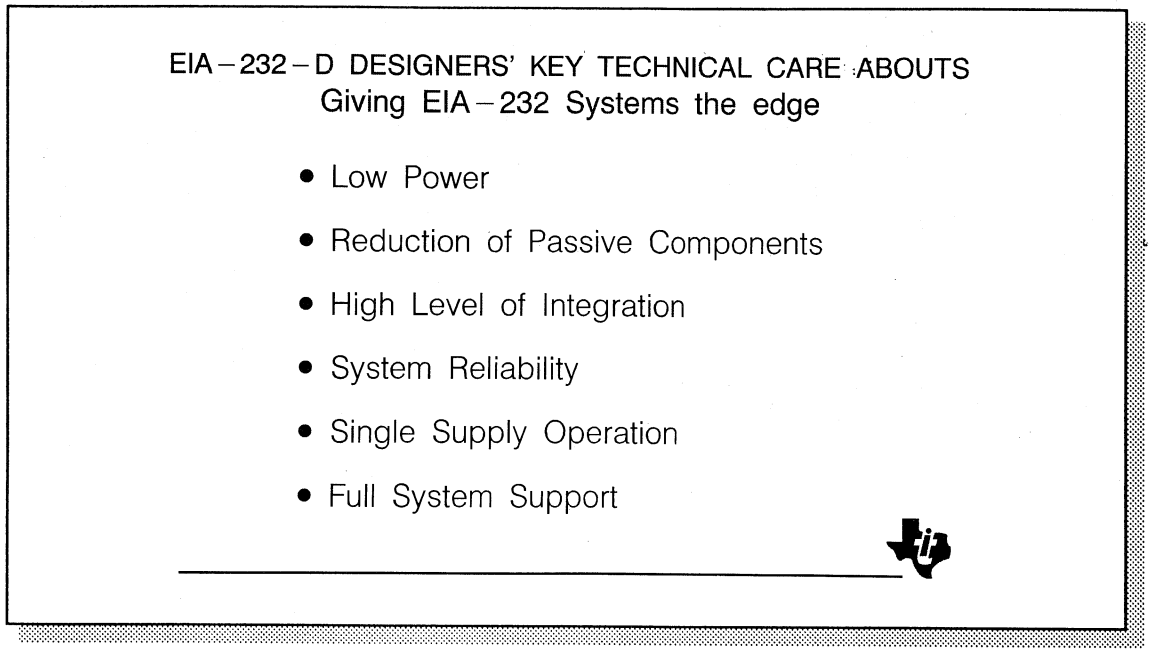


Figure 05 - Designers Key Technical Requirements

The principle requirement of any device designed for operation in an EIA-232 application is in its conformance to the standard's specification. Seemingly this would leave little room for product differentiation. However by taking into consideration the key points listed in the accompanying figure it is apparent that semiconductor manufacturers can differentiate their products, thus allowing original equipment manufacturers to differentiate their's.

The ever increasing use of lap-top and portable, battery backed equipments employing the EIA-232 interface, demands lower-power devices than previously available. Also the increasing integration of modems, PCs and peripherals coupled with the necessary reduction

Notes

in board space requires the elimination of external passive components. Ultimately expensive power supply components used to generate the necessary ± voltage supplies can be discarded in favour of drivers and receivers (available on the same ic) containing charge pump circuitry. Although not required in computers containing disk drives, since ± supplies are already available, this feature is required for many handheld test and medical equipments.

In systems like host terminal controllers or server systems where multiple EIA-232 lines are used, system down time is expensive and difficult to diagnose. Therefore added reliability and robustness must be built into these system, furthermore employing self test capabilities will greatly simplify fault finding diagnosis.

Most EIA-232 systems use asynchronous data transfer which requires a communications controller for the parallel-to-serial data conversion (and visa.versa) to control the flow of data, to add/delete the start/stop bits and for error checking. Although the microprocessor can be used for this purpose dedicated controllers are generally preferred to off load the mundane interface activity from the processor, reserving its use for number manipulation.

Texas Instruments provides the complete EIA-232 solution, having on offer industries widest choice of EIA-232 products, including both line driver / receiver functions and communication controllers.

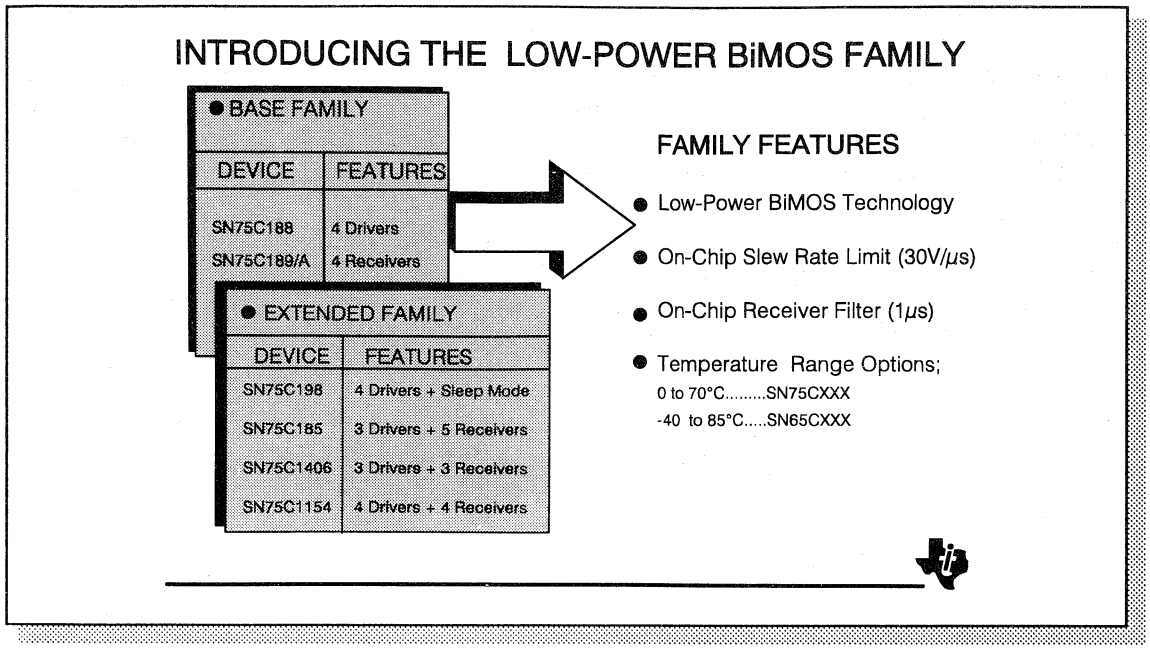


Figure 06 - Introducing the Low-Power BiMOS Family

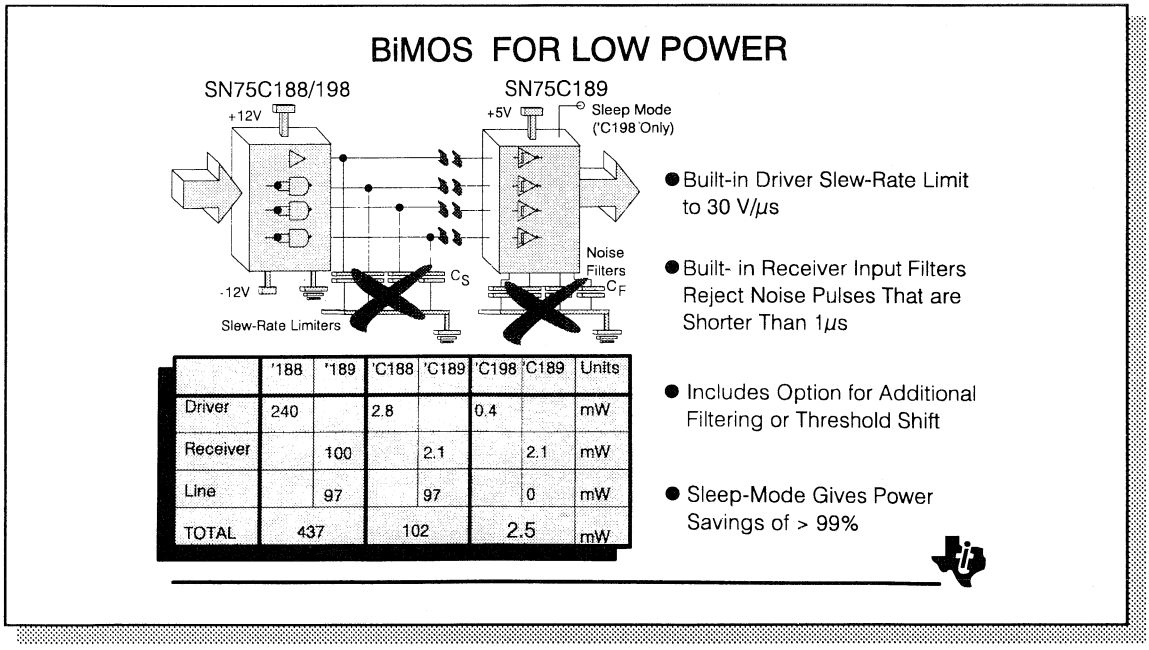
TI has been a leading supplier of EIA-232 products for many years, in fact Bipolar devices such as the quad driver SN75188 and quad receiver SN75189 have become synonymous with EIA-232 designs. Although these products (see Interface Circuits data book for complete range) continue to enjoy popularity, and are still being selected for today's designs, the emergence of battery backed and portable equipments has led to a need for devices yielding much lower power consumption than the old bipolar technology can give. Consequently TI looked towards one of its many new technologies - BiMOS.

BiMOS is a low-cost, low-power process capitalising upon the benefits from both bipolar and the low-power consumption of PMOS structures. Using this process in EIA-232 designs can yield as much as a 99% saving in power consumption.

Notes

The new generation of BiMOS devices are shown in this figure, along with the key family features. In essence all devices have been designed with the power and space restrictions imposed on modern equipments in mind. Namely each device in the family, in addition to having low-power, contains the necessary capacitive components for receiver filter implementation and driver slew-rate limit. The extended family of devices are optimised for particular usage of EIA-232 handshake lines, for example the SN75C185 is optimised for IBM®compatible serial ports.

Naturally all devices are offered in either surface mount packaging (SO) or in the plastic dual-in-line package (DIP). Temperature ranges available are; Commercial, 0°C to 70°C, or industrial, -40°C to 85°C, Selected by SN75Cxxx or SN65Cxxx respectively.



	'188	'189	'C188	'C189	'C198	'C189	Units
Driver	240		2.8		0.4		mW
Receiver		100		2.1		2.1	mW
Line		97		97		0	mW
TOTAL	437		102		2.5		mW

Figure 07 - BiMOS for Low-Power

Most devices used today like the MC1488/SN75188 and MC1489/SN75189 are fairly old designs cc suming a lot of power. New developments like the SN75C188 and SN75C189 have yielded low power devices offering insignificant quiescent power consumption ***when*** compared with the line current. (Line current flows from the driver output through the receiver input impedance, typically 5kΩ, down to ground). This current flows even when no data is transmitted.

One way to reduce this line current in data off periods is to employ a driver with a tri-state output feature like the SN75C198. By disabling the output the power consumption can be reduced to only 1% of the old SN75188/SN75189 system.

Most industry standard devices require capacitor by-passing to ground, on all the lines, to ensure the maximum slew-rate limit of 30V/μs specified by the standard. The capacitor value, C_S can roughly be estimated from the maximum driver output current and the cable capacitance. The cable length and capacitance is usually not a fixed parameter, however with a maximum output current of 12mA from SN75188 a 400pF capacitor for C_S will ensure operation within the standard even without a loading cable.

When communicating between the elements of a data processing system in a hostile environment spurious data, caused by ground shifts and noise, may be introduced. Therefore it can become difficult to distinguish between a valid data signal and those introduced by the environment. To overcome this problem in systems using older devices, a RC receiver filter is formed by a part of the receiver's resistive input impedance and an external capacitor, C_F giving a single pole roll-off. This adds up to a total of 8 capacitors required per quad driver and receiver pair for proper operation.

The new SN75C188, SN75C198, SN75C189 and SN75C189A designs feature built-in slew-rate limitation that meets the standard under all load conditions. Furthermore a unique built-in receive filter rejects all signals below 1μs of duration, regardless of voltage amplitude, and accepts all signals longer than 4μs as valid data.

Obviously, the new designs eliminate 8 external passives per driver/receiver pair.

Notes

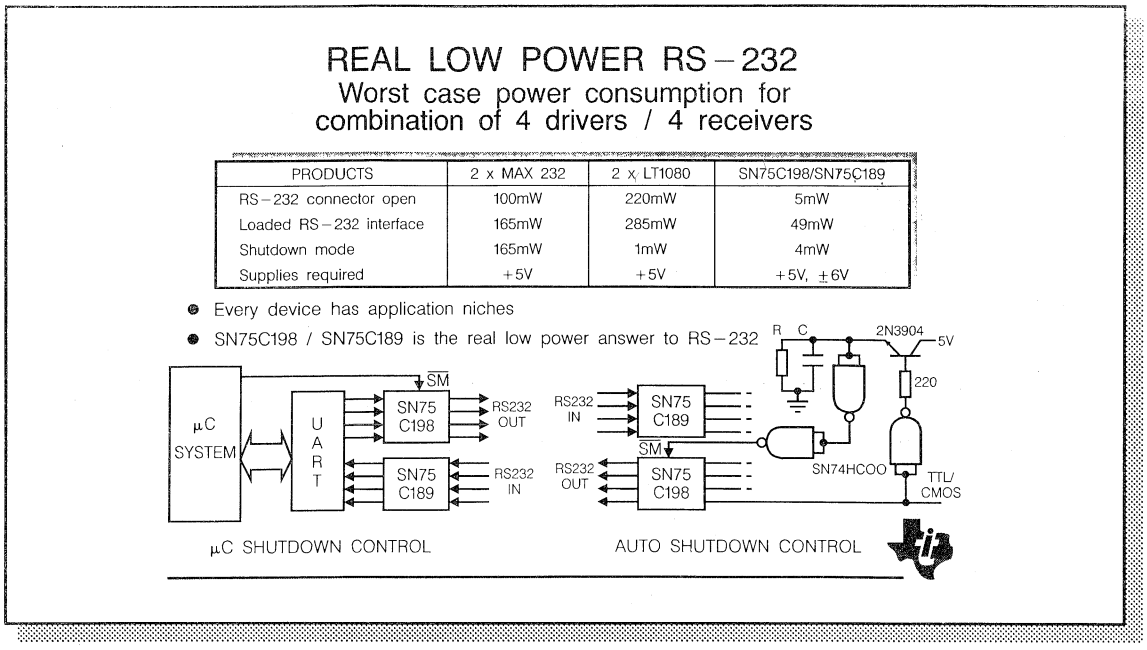


Figure 08 - Real Low Power EIA-232

EIA-232 devices with an on-chip charge-pump generate dual supplies for the EIA-232 driver function from a +5V logic supply voltage. Because of this they are gaining increasing popularity. However, for power conscious applications such as laptop/notebook PCs, their peripherals and for battery driven industrial equipment, the SN75C198 and SN75C189 combination significantly reduce the power supply demands. Even when taking into account the low efficiency of dual voltage supply generation these devices are clearly the best solution.

Comparison of Alternatives

The worst case power consumption for different driver/receiver combinations forming four EIA-232 driver lines and four EIA-232 receiver lines are given in the table. All devices are available from Texas Instruments. Minimum supplies required to meet EIA-232-D requirements are used.

	4 Driver and 4 Receiver Functions with 3-State Output or Shutdown Mode			4 Driver and 4 Receiver Functions		
Function/ Parameter	SN75C198 SN75C189	2 x LT1080	LT1030 SN75C18 9	2 x MAX232	2 x LT1081	SN75C188 SN75C189
Charge-pump	No	Yes	No	Yes	Yes	No
Required Supplies	±6V(min) +5V	+5V	±7V(min) +5V	+5V	+5V	±6V +5V
Max Icc No Load	160µA (±6V) 700µA (+5V)	44mA	1mA (±7V) 700µA (+5V)	20mA	44mA	160µA (±6V) 700µA (+5V)
Max Icc Shutdown	40µA (±6V) 700µA (+5V)	200µA	150µA (±7V) 700µA (+5V)			
Total Active Power Consump. No Load #	5.4mW	220mW	17.5mW	100mW	220mW	5.4mW
Total Active Power Consump. 3kΩ Driver Loads	49mW	285mW	78mW	165mW	285mW	49mW
Total Shutdown Power Consump.	4mW	1mW	5.6mW			

No Load condition refers to the situation where no EIA-232 cable and receiver is attached.

Notes

For continuous data transmission or under no load conditions, the combination of SN75C198/SN75C189 or SN75C188/SN75C189 has the lowest power consumption. However, if a EIA-232 link is established which has periods where no data is being transmitted, the required average power consumption can be further reduced by taking advantage of the SN75C198's 3-state output (or sleep-mode function). Thus avoiding wasting power dissipated into other receivers input impedances. This makes the SN75C198/SN75C189 combination the most attractive solution for real low power systems with data off periods of less than 99% of the total time. If data is submitted less frequently than 1% of the total time, the LT1080 solution becomes more favourable but a higher peak power demand is required from the power supply when transmitting.

Although requiring three supply voltages, ±12V and +5V, the SN75C198/SN75C189 solution can easily beat the power consumption of +5V charge-pump systems, even when the efficiency of generating the additional ±12V is taken into consideration. If an additional centre tap winding is added to the existing +5V switch mode power supply's transformer, simple rectification with schottky diodes and ripple smoothing is usually enough to provide the ±12V supplies, as no strict stabilization requirements exist. If needed low drop out regulators can however perform further stabilisation without too much power loss.

Shutdown Control Methods

Microcomputer controlled shutdown is simple to implement under no data conditions by bringing the SN75C198 quad driver in to Sleep-Mode (pseudo 3-state output) condition. Using Sleep-Mode in this manner can also be used to prevent 'garbage' from being transmitted during device power-up.

Power savings can also be obtained in existing systems or where no extra µP port is available for control purposes by an auto shutdown control. This is implemented by simply adding a low power SN74HC00 logic gate, a transistor and an RC time constant to form a simple mono stable multivibrator. The SN75C198 is enabled as long as its Sleep Mode pin is kept high by sensing a low TTL/CMOS level on a EIA-232 data or handshaking transmit line. Enable time is prolonged by the time it takes to discharge C through R to the CMOS gate's threshold level.

An alternative automatic scheme can be implemented by using a TLC555 timer configured for edge triggered mono stable operation. If the TLC555 trigger input is AC coupled to the TTL/CMOS input of the EIA--232 driver being first activated during a transmission, the timer enables the SN75C198. The TLC555 keeps the EIA-232 driver active for a time equal to 1.1 * RC, where R and C are the timers external resistor and capacitor in its mono stable configuration.

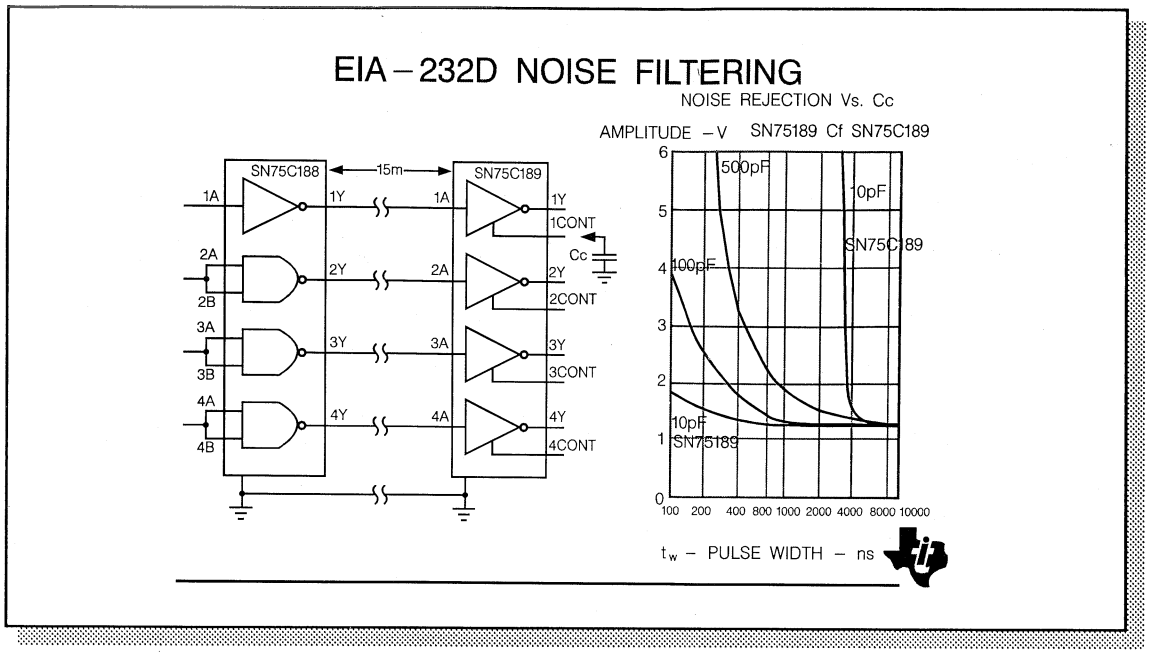


Figure 09 - Noise Filtering for EIA-232-D Interface

The standard states a maximum line cable capacitance of 2500pF, which corresponds to an approximate line length of 15m. As the interface line gets longer it becomes more susceptible to noise pick-up from the surrounding environment. This pick-up is due, in part, to the inductive nature of the line. As the signal switches, a rapidly changing magnetic field induces noise currents into the line thereby corrupting signal data.

The level and cause of this noise will dictate the nature of solutions or precautions that should be taken.

For operation at high data rates the use of a differential line might be the best solution. If however, a low cost and simple single ended solution is required then standard EIA-232 devices can be modified to give noise protection. This is achieved by slowing down the response of the receiver's input stage, making them too slow to respond to fast switching noise pulses.Even small levels of input noise can falsely trigger the receiver. The maximum

Notes

data rate specified in the standard is 20kbaud, corresponding to a minimum pulse period 100μs. Therefore in normal applications, most devices are far faster than the specification requires

To slow down old bipolar receivers, such as SN75189s, a capacitor, C_C, needed to be placed on each of its response control pins. This meant an additional four capacitors per device, which can be awkward and costly. The effect of this response control capacitor is to set up a low pass filter on the receivers input, shown in the figure. In order to provide large pulse rejection the capacitor needs to be quite large. Furthermore the filter response is very asymmetric, affording protection against positive noise voltage spikes only, and will tend to attenuate rather than reject short noise pulses.

The receivers in T.I.'s new BiMOS driver/receiver family possess on-chip filtering, which reject fast transient noise pulses. Implementing the filters on-chip allows precise filters to be implemented without significantly altering the receivers response. These filters are totally symmetrical offering protection against both positive and negative noise pulses and with the ability to reject rather than attenuate short noise pulses. To approach the level of filtering offered by the BiMOS receivers the standard receivers require much larger capacitors, and even then fall well short of filtering requirements.

In summary the advantages of these internal filters, are in improved quality and reliability of filter operation which can operate over the entire EIA-232 baud rate range.

CTS; Having driven its own CTS input high the first DTE is now able to transmit the data it wished to send.

This is one such arrangement which allows one DTE to communicate with another DTE, there are however many such arrangements. Each one of these arrangements put a greater control of the flow of information on one of the key signal lines, and are quite frequently dependent upon the type of DTE used.

The 'C1154 integrates a further driver/receiver pair into the chip, making it suitable for further EIA-232 applications. For example the extra receiver input will allow the 'C1154 is to monitor the Ring Indicator (RI) input from a modem or other similar type of DCE.

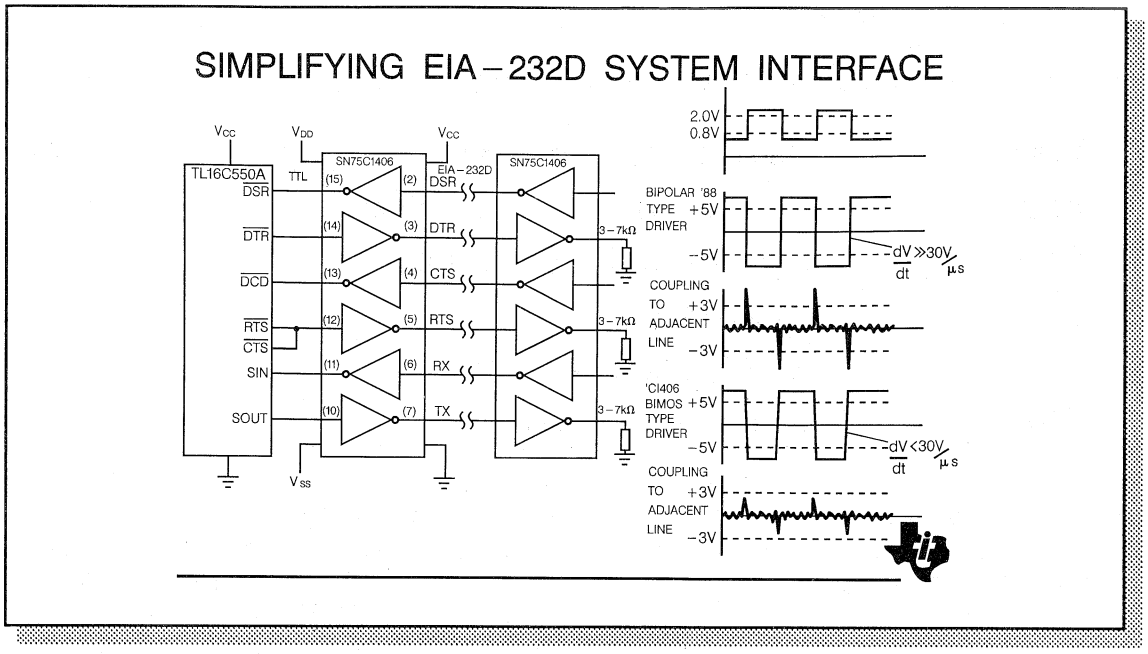


Figure 10 Simplifying System Interface

As the digital logic within systems become more integrated and operate from lower power supplies, it is logical that the interface circuits also need to be more integrated and consume less power. The BiMOS range of devices use low-power design techniques to integrate multiple driver/receiver elements into a single chip thus meeting both these requirements.

The following text describes the advantages of using single chip multiple receiver/driver functions for common EIA-232 applications. The devices highlighted are the SN75C1406 (3 drivers/3 receivers) and SN75C1406 (4 drivers/4 receivers).

Notes

Minimal EIA-232-D interface

An absolute minimum system for EIA-232-D requires only six lines;

$\overline{\text{RTS}}$	**Request to Send. DTE to DCE**
$\overline{\text{DTR}}$	**Data Terminal Ready. DTE to DCE.**
$\overline{\text{TX}}$	**Data Transmission line to DCE.**
$\overline{\text{RX}}$	**Receive line**
$\overline{\text{CTS}}$	**Clear to send. DCE to DTE**
$\overline{\text{DSR}}$	**Data Set Ready. DCE to DTE.**

The **SN75C1406** and **SN75C1154** are low power BiMOS EIA-232-D integrated circuits containing three driver/receiver pairs and four driver/receiver pairs respectively. This makes them better able to provide the necessary interface signals within the same integrated circuit. The EIA-232 standard was devised for modem (DCE) to PC (DTE) interactions, but the applications of the interface signals have been expanded to include PC (DTE) to printer (DTE) interfaces.

When considering the latter case the triple driver and receiver pairs of the 'C1406 make it an ideal choice. In these applications only one extra signal will normally be applied; the Data Carrier Detect (DCD) signal, which can be amalgamated with the CTS signal. This gives only six interface lines plus the signal ground wire. The common term for this application is DTE-DTE zero modem, and enables to DTEs to communicate without a DCE.

The timing of this operation is as follows;

DTR; One of the DTEs states that it is connected to the line, driving the DSR pin of the opposing DTE.

DSR; The opposing DTE replies in the same way, announcing that it itself is connected.

DCD; The DTE then checks the state of its DCD input. A low state implies that the opposing DTE's RTS output is low and so not wishing to transfer information.

RTS; The DTE is then able to drives its RTS input high; driving the opposing DTE's DCD input high and its own **CTS** input high.

A better solution is to place the slew-rate limiting within the chip itself. Using similar techniques to those employed for slew rate limited operational amplifiers, the slew rate of line drivers can also be limited. Using the miller capacitance multiplying effect, the slew rate of the driver can be slowed down. The on-chip capacitors are normally in the order of 5pF, while the currents driving the on-chip capacitor are the order of microamperes, thus reducing power consumption within the device. The biasing current to the output transistors

is unaffected by this technique and will be more than sufficient to drive the 3kΩ load as offered by the receiver.

In summary, both the SN75C1406 and SN75C1154, as do all the BiMOS family of EIA-232-D devices, have on-chip slew rate limiting. Thus offering increased system integration and lower power dissipation solutions for modern EIA-232-D applications.

Like all their BiMOS counterparts the 'C1406 and 'C1154 offer high performance at very low power dissipation. All the receivers contain the same receiver filter as in the C189 receiver, so making them less sensitive noise induced onto the line. Another advantage with these devices is their drivers' on-chip slew rate limiting.

Slew Rate Limiting

When driving short lines fast changes in the voltage on one line can induce charge into an adjacent line. This can cause problems, especially when using short line lengths and can limit the speed at which data can be sent. The figure shown compares the performance of a bipolar '188 type device to the SN75C1406 device. It clearly shows the importance of slew-rate limiting when trying to maintain performance of the whole system.

The faster the driver output voltage is switched, the greater the amount of charge induced into the adjacent line. This charge will be converted into a voltage, and if the charge is large enough, the voltage on the line could cross through the receivers input voltage threshold region, causing the receiver to falsely trigger. As the capacitance of the line increases, with longer interface line lengths, these slew rate related effects become reduced.

The EIA-232-D standard specifies a maximum slew rate through the transition region of **30V/µs**. Relating this to capacitance and current; only 100µA of output current , into 30pF load capacitance, is needed to exceed the slew rate limit; All devices are capable of supplying more than 5 mA. Therefore if the slew rate limit is not to be exceeded, the switching speed of the drivers output stage needs to be reduced. An established solution is to place loading capacitors on the output of the driver. The value of loading capacitor required will depend upon the line length, but is generally in the order of 330pF. The effect of this capacitors is to cause the output transistors to saturate causing it to short circuit current limit, thus preventing fast switching edges.

Notes

There are some major problems with this established process; One being the variance in current at which the output short circuit current limit operates, especially when taking temperature changes into consideration. Again the value of capacitance placed on the line will depend upon the drivers output short circuit capability as well as line length. For example a device capable of sourcing 10mA will need a total capacitance of 330pF placed on its output to meet the 30V/µs s;slew rate limit, while placing this value across a device capable of sourcing 4mA will have its slew rate limited to less than 12V/µs.

Another problem encountered is the increase in power dissipation through the output stage. The output voltage of the driver will normally be close to one supply rail, so when it tries to switch to the other, the active transistor will have almost all of the supply voltages across it. The extra external capacitor will clamp the driver 's voltage close to the supply voltage causing the output transistor to source large amounts of current. The combination of a large source current and large voltage cause it to dissipate large amounts of power.

Operating at these prolonged bursts of high current will ultimately increase the chip temperature which in turn can affect the long term life of the device. Bipolar technologies are normally much better able to withstand such effects.

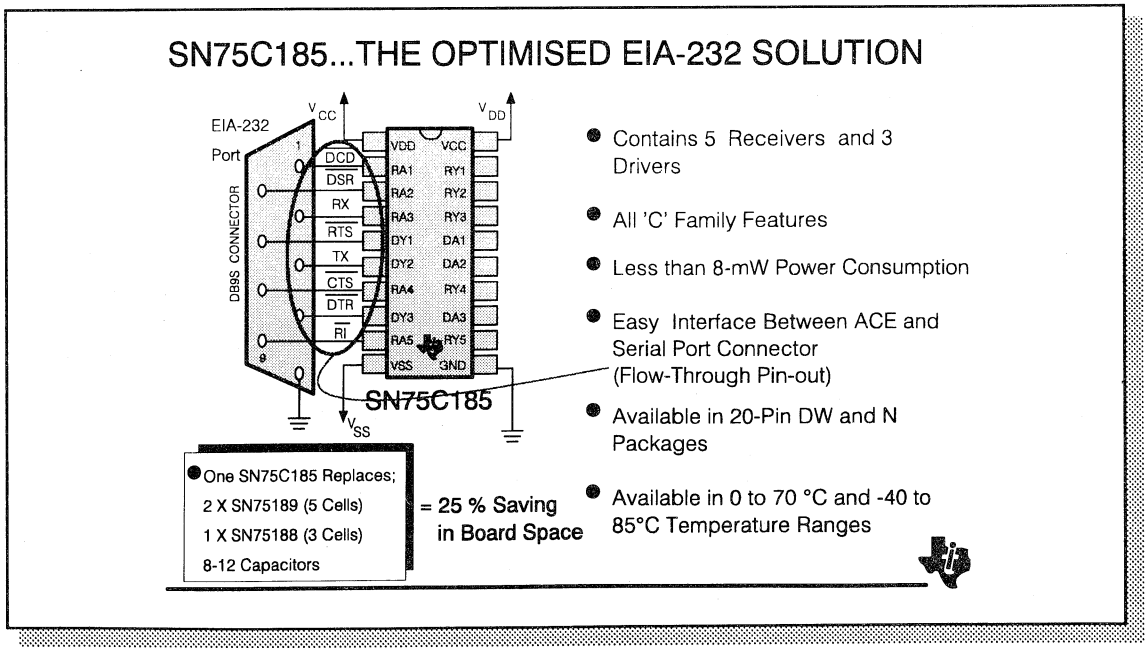


Figure 11 - SN75C185...The Optimised Solution

The SN75C185, driver/receiver is further testimonial to Texas Instruments' commitment to the EIA-232 standard. Designed specifically for today's low-power applications, this device provides the designer with higher levels of system integration, reliability and optimisation than previously available. This figure sets out the key features of the SN75C185.

The need

The ever increasing use of portable/battery backed equipments such as the lap-top PC, hand held test and medical equipment has confronted the designer with many new challenges, namely; restricted power supply capacity, weight, battery operation and restrictions in enclosure space. This situation is further aggravated by the consumers ever increasing demand for higher performance solutions.

By providing the exact combinations of driving and receiving elements, along with the necessary passive components, a highly optimised solution can be provided - the SN75C185 provides just this. The SN75C185 integrates three drivers and five receivers and includes the necessary capacitors for driver slew-rate limit (30 V/µs) and receiver filter implementation all in a single 20-pin package

The rationale for integrating three drivers along with five receivers is easily understood by looking at common implementations of the EIA-232 standard. Although twenty two signal lines are designated within EIA-232, far fewer are used in practice. The large number of handshaking lines and the absence of standard guide-lines has led to a multitude of EIA-232 implementations. - A fact not lost on EIA-232 users!, as invariably the EIA-232 compatible PC will not communicate with its EIA-232 compatible printer!.

In an attempt to eliminate this problem industry has formed a de-facto standard around the combinations of handshaking lines shown in figure 1. This is further illustrated by a casual look at the back of any lap-top PC or hand held test equipment which will reveal an ever increasing use of the 9-pin (DB9S) connector, rather than the space consuming 25-pin (DB25S) connector.

The designer's dilemma is eased further still by the use of a flow-through pin-out architecture. By aligning one side of the SN75C185 with the pins of the DB9S connector and the other to industry standard ACEs PCB layout can be greatly simplified.

Notes

Low -Power as well

In common with all of Texas Instruments' BiMOS products these devices combine the benefits of Bipolar's drive capability and robustness along with the low-power consumption of CMOS. This power saving when compared to the alternatives is calculated in the following pages and is illustrated graphically in the following figure.

Available in either a single 20-pin wide-bodied SO pack or N pack, the SN75C185 offers designers greater than 25 % saving in board space when compared to alternatives.

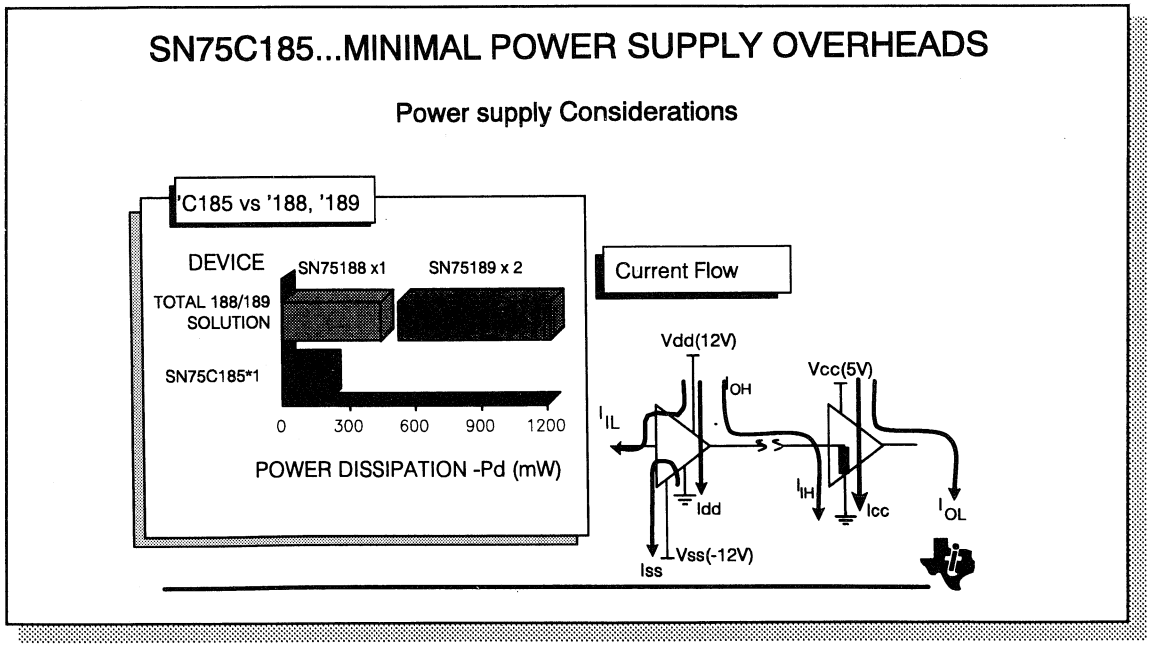


Figure12 - SN75C185... Power Considerations

System power consumption is often considered very late in the design cycle. Of even more concern is that the power consumption of the interface circuitry, being the least attractive circuit to design, is often totally overlooked. The consequences of this can be catastrophic especially, when using devices in confined spaces. These areas will normally have very poor air circulation causing the ambient temperature of the whole system to increase. These types of problems are particularly difficult to diagnosis as failure can often be intermittent as devices pass into and out of thermal shut-down.

For these reasons low quiescent power devices are becoming a necessity for modern applications. As digital technologies advance their power consumption decreases, making the interface circuits the limiting factor as far as system power consuption is concerned.

The **SN75C185** was designed with power consumption in mind. In addition It offers matched pin out to industry standard sockets and ACEs, as well as offering on chip slew-rate limiting and on-chip noise filtering. Another benefit is that it contains three drivers and five receivers which is the minimum DTE requirement to interface to the EIA-232-D standard.

Interface Power Consumption Calculations

Before the availability of the SN75C185 common implementations of EIA-232 require one quad driver package and two quad receiver packages; in the driver chip one device is redundant, while the receiver chips three devices are redundant. These devices would, however, still be taking their quiescent current and hence wasting power. So in order to provide the interface signals, three integrated circuits were required while only two thirds of the capability was being used. The calculations below set out demonstrate this difference;

When comparing the 'C185 solution to that provided by the '88 and '89 devices the power saving is enormous.

Both implementations require three supply voltages; a 5V and ±12V supplies. The power dissipated, P_{dis}, within each device will be the quiescent power of the device, P_q, plus the power dissipated in the input stage, P_{is}, and the power dissipated in the output stage, P_{os}, (when it is driving the line). Hence,

$$P_{dis} = P_q + nP_{is} + mP_{os}$$

Where n is the number of active input stages and m is the number of active output stages.

SN75188/SN75189 Combination

Using an SN75188 for the driver, the quiescent power consumption would be 576mW. In addition to this would be the power dissipated in the input stage, P_{isd}:-

$$P_{isd} = V_{CC} * I_{IL}$$

$$= 12 * 1.6 \text{ mW}$$
$$= 19.2\text{mW}.$$

This will be multiplied by four to take into account all four drivers, putting the fourth driver into a defined state so as to reduce any noise problems which could be introduced by leaving the input floating.

Notes

The power dissipated in the output stage, P_{osd}, will be:-

$$P_{osd} = (V_{CC} - V_{OH}) * \frac{V_{OH}}{R_L}$$

$$= (12 - 9) * \frac{9}{3} \text{ mW}$$

$$= 9\text{mW}.$$

This figure will be multiplied by three to take account of the active three drivers driving the interface line. These sum up to give a total power dissipation of

$$P_{dis} = 576 + 4 * 19.2 + 3 * 9 \text{ mW}$$

$$= 680 \text{ mW}.$$

The junction temperature of a DIP device would have risen by 74°C.

Using the SN75189 receivers, a quiescent power of 130mW would be dissipated by each package. This would be multiplied by two to take into account both chips.

The power dissipated in the output stage has a similar equation to that of the driver, so:-

$$P_{osr} = V_{OL} * I_{OL}$$

$$= 0.45 * 10 \text{ mW}$$
$$= 4.5\text{mW}$$

This power dissipated will be multiplied by 5 to take into account the 5 receivers being used. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the ic will however cause the junction temperature to rise. So the power dissipated in the input stage, P_{isr}, equals:-

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$

$$= \frac{9^2}{3} \text{ mW}$$
$$= 27\text{mW}$$

This power dissipation will also require multiplying by 5 and the remaining receivers will require tying into a state where they will not be susceptible to noise, which could cause interference. Tying them to the 5V supply increases the power dissipation by a further 8.3mW per receiver.

Assuming 3 receivers in one '189 is being used and 2 receivers in the other, the power dissipated for the first receiver is:-

P_{dis} = 130 + 4 * 27 + 3 * 4.5 mW

= 233mW.

The power dissipated in the second receiver is:-

P_{dis} = 130 + 4 * 27 + 2 * 4.5 mW

= 210mW.

This would raise the temperature of the first and second receiver by 25°C and 23°C respectively.

The total power dissipated by the SN75188/189 combination is the sum of these three powers, equalling 1.12W.

Using the SN75C185

The power dissipation of the 'C185 can be calculated in a similar manner. The quiescent power consumption of the 'C185 is equal to:-

P_q = $V_{DD} * I_{DD} + V_{SS} * I_{SS} + V_{CC} * I_{CC}$
= 12 * 200 + -12 *-200 + 5 *750 µW
= 8.55mW

The power dissipated in the input stage of the driver is:-

P_{isd} = $V_{DD} * I_{IL}$

= 12 * 1 µW
= 12µW.

This will be multiplied by three to take into account all of the drivers.

Notes

The power dissipated in the output stage of the driver, P_{osd}, is:-

$$P_{osd} = (V_{DD} - V_{OH}) * \frac{V_{OH}}{R_L}$$

$$= (12 - 10) * \frac{10}{3} \text{ mW}$$

$$= 6.67\text{mW}.$$

This will be multiplied by three to take account of the three drivers driving the interface line, giving a power dissipation of 20mW.

The power dissipated in the output stage of the receiver has a similar equation to that of the driver, so:-

$$P_{osr} = V_{OL} * I_{OL}$$

$$= 0.4 * 3.2 \text{ mW}$$
$$= 1.28\text{mW}$$

This value will be multiplied by 5 giving a total of 6.4mW of power dissipated in the receiver's output stages. The input stage will also dissipate some power, but this power will not be supplied by this part of the interface system. The power dissipated within the chip will however cause the junction temperature to rise.

So the power dissipated in the input stage, P_{isr}, equals:-

$$P_{isr} = \frac{V_{OH(d)}^2}{R_L}$$

$$= \frac{10^2}{3} \text{ mW}$$
$$= 33.3\text{mW}$$

This power dissipation will also require multiplying by 5. Giving a total input power dissipation of 167mW.

Summing all the power contributers the total power dissipation is given by;

$$P_{dis} = P_q + 3P_{isd} + 3P_{osd} + 5P_{isr} + 5P_{osr}$$

$$= 8.55 + 3 * 12*10\text{-}3 + 3 * 6.67 + 5 * 33.3 + 5 * 1.28 \text{ mW}$$

$$= 201\text{mW}.$$

The total power dissipated by the SN75C185 is 201mW

This is a tremendous power saving especially when considering that the line is still being driven. The temperature rise within the C185 would only be 22°C enabling it operate much more reliably and with higher ambient temperatures.

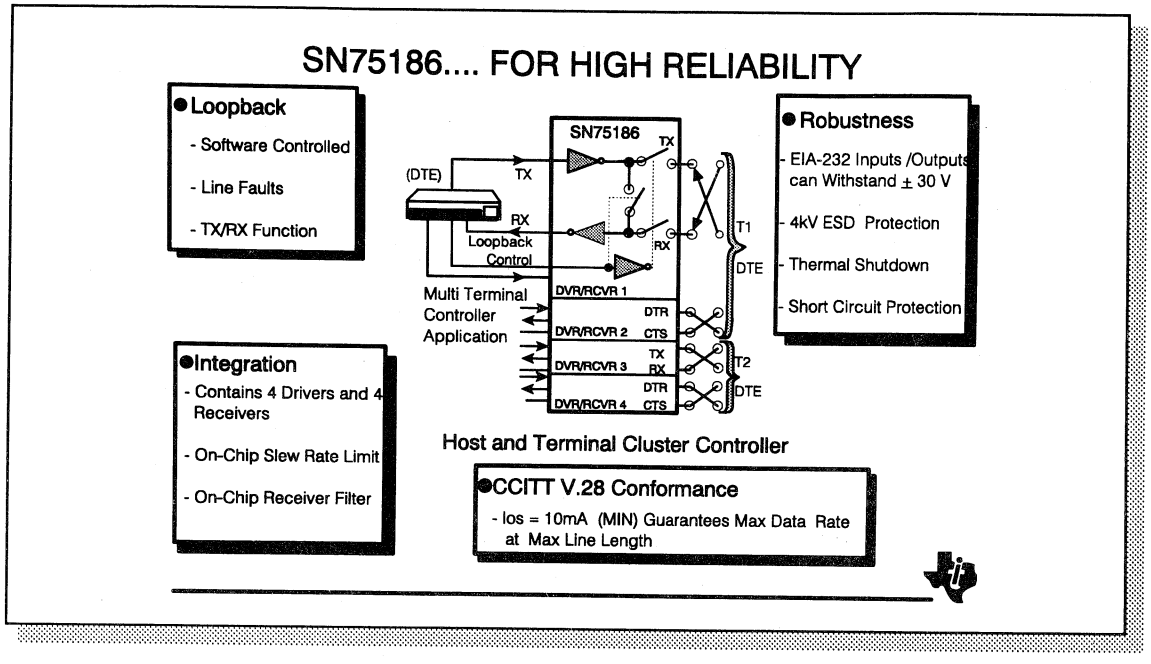


Figure 13 - SN75186...For High Reliability Designs

In systems where a central host communicates with several terminals a large number of EIA-232 devices are used. In this situation system failures can be difficult to identify resulting in the system down time whilst the host is down, which can be expensive. The interface circuits close proximity to the outside world, via the edge connector, makes the EIA-232 devices particularly vulnerable to failure, often caused by excessive external signals being applied to the transmission line or incorrect insertion of connectors and cables..

Notes

The major consideration for EIA-232 devices in such applications is robustness and the ability to test themselves under software control from the host (without the need for disconnecting cables and manually inserting a loopback connector). Such a feature could facilitate faster fault diagnosis and significantly reduce equipment down time.

These requirements have driven the need for the SN75186, an extremely robust quad driver and receiver with loopback self test capability. The device includes the usual on chip driver slew-rate control and receiver filter. In addition, this device features a high minimum short circuit output current allowing it to fully comply with the CCITT V.28 transition time requirements at full capacitive load and maximum data rate. This drive capability is unique in the market.

The device's robustness is borne out by an ESD rating of 4kV, a rating which can not be met by standard devices in the market, and the ability to withstand +/-30V at any EIA-232 input or output whilst powered or un-powered. Its loopback feature allows software controlled testing of nearly 100% of the device's circuitry as well as short circuit to ground or either supply rails. Loopback testing of a single driver/receiver pair is initiated by activating its loopback control pin. This disconnects the EIA-232 line and feeds the driver output back through the receiver input for comparison within the host to determine if the functional operation of the driver and receiver together is correct.

Flexibility of this control is ensured by each driver/receiver having its own loopback control input. In the case of a permanent output short or other problems resulting in a very high chip temperature, a thermal shut-down facility protects the device against damage. During this thermal shut-down mode the output goes into a high impedance state and the receiver is held in a logic high (marking) state.

The application shown, details the interface between a single SN75186, the host and two connected terminals - both host and terminals operate as DTEs. A very simple host to terminal interface is employed using only two handshake lines: CTS and DTR in a cross connection.

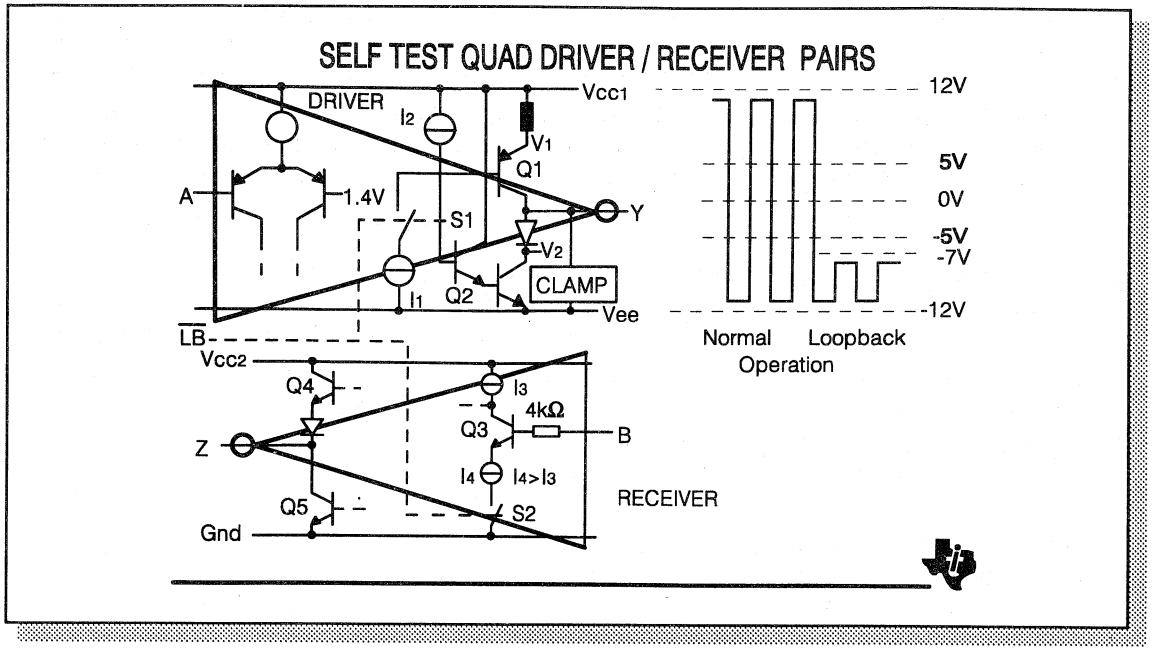


Figure 14 - Self Test Quad Driver Receiver Pairs

The SN75186 operates in one of two modes;

a) normal independent driver and receiver pairs
b) driver receiver self-test pairs.

In **mode a** operation of the loopback circuits are transparent and the device will operate as a normal driver/receiver.

Mode b is commonly referred to as **loopback** mode where the driver and receiver makes a self-test **loop** which is fed **back** to the digital controller. When operating in loopback mode the SN75186 is able to test over 90% of its components, the remaining parts of the SN75186 have a low probability of failure and have been strengthened to make their failure even more remote.

Notes

Loopback can be independently introduced on the four driver/receiver pairs by bringing the relevant LB pin low. This then switches out the receiver input stage and connects the driver to the receiver's secondary input stage via switch S_2 and transistor Q_3. Before entering loopback mode the driver should be brought into a negative, mark, state. This is to prevent contention, when first entering loopback, between the driver output and the loopback signal. It also removes the possibility of false data being sent to the opposite receiver at the end of the line.

When in loopback mode the input of the driver will be toggled (brought high and then low again) to test the operations of the driver and most of the receiver. As the input is toggled switch S_1 controls the flow of current sources I_1 and I_2 causing transistors Q_1 and Q_2 to alternately turn on and off respectively. The input signal will cause the output of the driver to toggle. By sensing the voltages at V_1 and V_2 it is possible to measure the workings of the output stage. The voltages at V_1 and V_2 also control switch S_2 which drives the output of the receiver.

The output of the driver has been designed so that when in loopback mode the output of the driver can vary from the negative supply voltage up to a maximum of -7V. If the device is functioning properly and there are no faults on the interface line the receiver should toggle in phase with the driver input. A fault will be detected by the receiver if the output voltage of the driver increases beyond -7V or decreases below the negative supply rail. If the output goes too low then there is strong probability that the drivers output is shorted to the negative supply. On the other hand if the output voltage of the driver goes above -7V it would appear that a either short to ground exists or a short to some other higher voltage. These problems would be indicated by the receiver output staying in one state. The receiver is an invertor and hence if the driver output voltage is too low the receiver output will be high. The opposite is true if the driver output voltage is too high.

The minimum output swing of a driver is specified as 5V. The SN75186 has a minimum output swing of ±7V enabling it to more than match the standard's requirements. If the receivers at the other end of the transmission line are not to be affected by loopback, the output voltage of the driver cannot pass through the transition region. As the driver cannot be disconnected from the line and still check its output's performance a clamp is applied to the output of the driver, thus preventing the output voltage of the driver from passing through the receiver's transition region. This clamp enables the driver's output to swing from very close to the negative rail up to -7V. It is due to this clamp that when entering the loopback mode of operation the driver should be in a `mark' state, that is its output should be low. This will remove any slight chance of contention problems.

While the driver input is toggling, its output should be toggling between -12V and -7V, implying the driver is functioning properly. If the receiver is also toggling it should be functioning properly. If the receiver ceases to toggle in phase with the driver input then a fault is present. The state of the receiver output can give the user an insight into the fault but SN75186 cannot give a direct cause or reason for the fault.

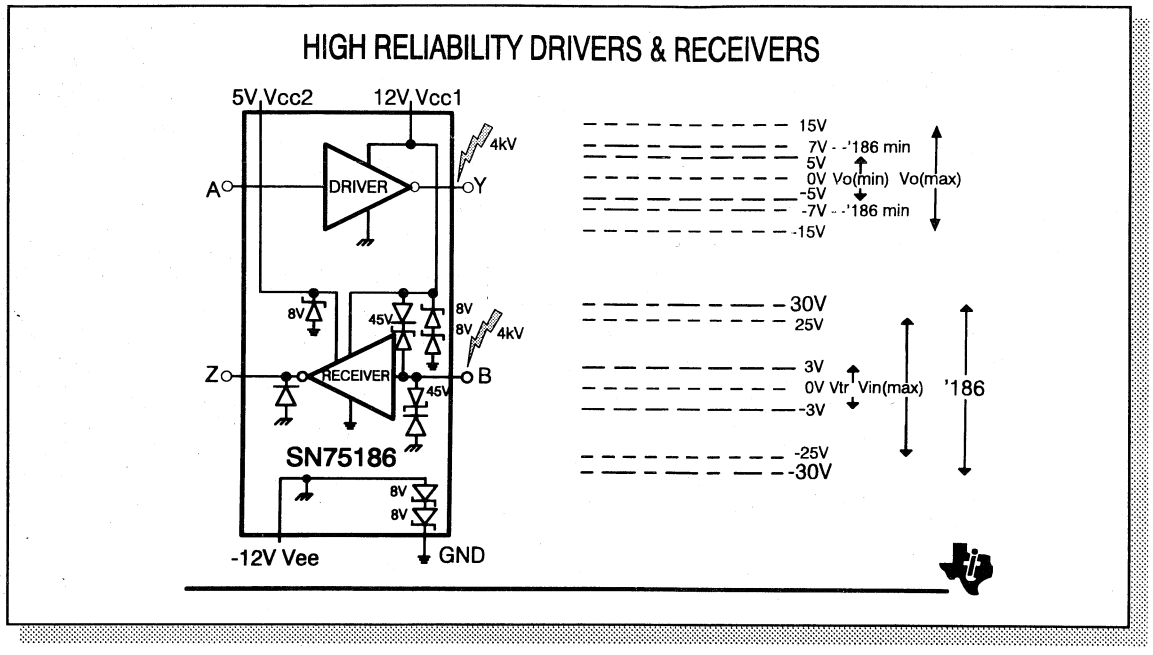


Figure 15 - High Reliability Drivers and Receivers

The EIA-232-D and the CCITT V.28 standards specify both the voltage ranges and the speed of the line's input and output signals. In most respects these are very similar, with the V.28 having more rigid timing requirements.

In meeting the EIA-232-D standards the driver must be able to drive the line with a voltage greater than 5V and less than 15V with a single receiver load of between 3kΩ and 7kΩ. Meeting these specifications is not normally a problem, but coupled with this the receiver should be capable of withstanding 25V on its inputs. The driver ideally should also be capable of withstanding these voltages. The **SN75186** device was designed bearing these specifications in mind. The maximum voltage at the driver's output or that can be applied onto the receiver's input is ±30V relative to ground, most other manufacturers who specify a 30V limit onto the receiver's input/ driver's output make it relative to the opposing rail.

Notes

In providing the required robustness there are two limits involved here;

a, power dissipated in the receiver's input resistance and,

b, the maximum voltage applicable to the output of the driver when it is driving the line.

Most other manufacturers tend to limit the latter range to just beyond the opposing rail and hence not fully meeting the specification. The SN75186 can easily go beyond the opposing rail. The wide range of voltages at the output of the driver and at the input of the receiver means that the protection circuitry of the device needs to take this swing into account.

In being designed to meet the requirements of both the EIA-232-D and the V.28 standards as well as maintaining good reliability, the SN75186 contains ESD protection which is guaranteed for up to 4kV. The receiver input, having a high input impedance, is more susceptible to charge induced spikes than other inputs/outputs and so contains two sets of 45V zener diodes polarised by two further diodes. This diode arrangement allows through the high range of input signals demanded by the standard while still providing a very robust protection from ESD. The input stage of the driver is also protected by a zener diode on its input, this is mainly to protect the device from ESD damage due to mishandling. A similar form of protection is applied to the supply voltages V_{EE}, V_{CC1} and V_{CC2} which can be quite frequently overlooked when considering ESD protection and precautions.

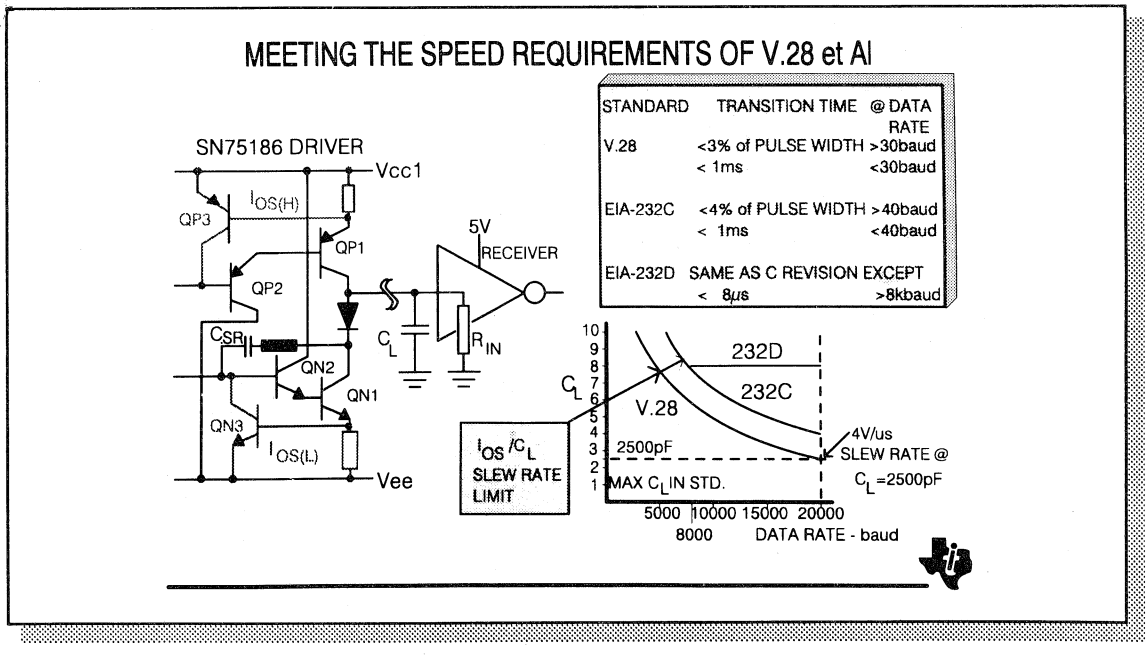


Figure 16 - Meeting the speed requirements of V.28

Both the EIA-232 C and D standards have similar voltage specifications to that of the V.28, their largest difference appears in their transition time specifications. The EIA-232 standards allow the transition time, t_T, to be 4% of the nominal element period or a maximum of 1ms whichever is less. V.28, on the other hand allows a maximum of 3% of the nominal element period. This timing difference means that the V.28 specification is harder to meet than the EIA-232 standards. This effect becomes more clear as the either the data rate or line capacitance increases.

At low data rates and low line capacitances all devices can meet both standards, this due to the driver not having to source a large amount of current to pass through the transition region. As the data rate or the line capacitance increases the driver has to supply more and more current to pass through the transition region quickly enough to meet the standards' specifications. A point will be reached where the short circuit current limit of the device is reached, resulting in the speed through the transition region depending on the ratio of line capacitance to device current limit. This limits what length of cable can be driven ($C_l \propto$ line length) and/or at what rate it can be driven.

T.I.'s **SN75186** was designed to meet all these standards, and so is capable of driving the 2500pF line while working at 20kbit/s, it is one of the few (if not the only) such driver and receiver pairs capable of doing this. Other devices do not have the output drive capability to be able to drive such heavy loads. In conjunction with this, the SN75186 contains internal slew-rate limiting, enabling it to meet the standards at light loads.

An approximate equation relating transition time of the device, the line capacitance, rate of change of output voltage and output current can be derived by assuming that the driver is in short circuit current limit. It will then behave as a current source charging up the line capacitance and driving the receiver's input resistance. This yields the following equation:-

$$t_T = R_i * C_l * \ln\left(\frac{|R_i * I_o| + |V_f|}{|R_i * I_o| - |V_i|}\right)$$

where;

- R_i is the minimum input impedance of the receiver = 3kΩ
- C_l is the load capacitance.
- I_o is the guaranteed minimum current that the driver can supply
- V_f is the final line voltage; in the transition region = +3V
- V_i is the initial line voltage; in the transition region = -3V

Turning this equation around with respect to, C_l, and cancelling for R_i,V_i and V_f we get :-

$$C_l = \tfrac{1}{3}\frac{t_T}{\ln\left(\frac{I_o + 1}{I_o - 1}\right)} \quad nF \ldots\ldots\ldots\ldots\ldots \quad \text{with } t_T \text{ in } \mu s,\ I_o \text{ in mA}$$

Notes

Using this equation and taking note that for the V.28 and EIA-232-D standards that t_T has maximum values of 3% and 4% of the nominal element period respectively the above curves are attained. The curve shows that the SN75186 is capable of driving 45m of cable at 20kbit/s and still meet the transition edge specifications of the EIA-232-D standard.

These equations are idealised but should give a worst case value, most of the SN75186 devices would yield far greater performances. Thus the device can be used to serve data links beyond the formal limits of EIA-232. For higher speed applications involving the SN75186 its noise protection filter may limit the data rate, but these rates would be outside the whole scope of the standard.

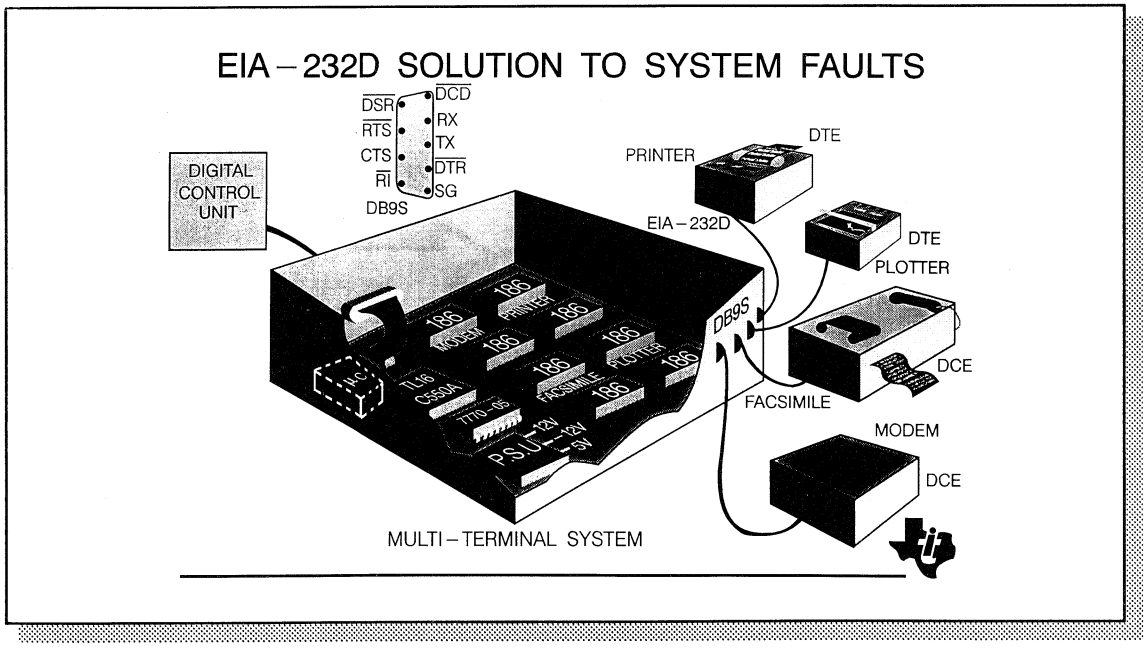


Figure 17 - A Solution to System Faults

In systems used to interface between multiple peripheral devices, such as shown in the figure, tracing faults can be very difficult and time consuming and can ultimately bring the whole system to a halt.

The **SN75186** is the ideal solution for tracing faults on the interface lines and the TL7770-05 is perfect for tracing power supply related faults.

Using all the features of the TL7770-05 enables both the logic supply and the interface supplies to be monitored and even provide over-voltage protection to the system. It can also be configured to provide a watchdog function on the controlling ACE. For further self monitoring the SN75186's Loopback mode provides the perfect solution to testing the line as well as providing the Robust input/output stages required for use in such conditions.

The EIA-232-D standard is ideal for sending information over short lengths at low data rates, and this is why its use has expanded to include the interface to printers and plotters. With the general increase in use and power of desktop machines the requirements of multi-cluster systems have also grown, thus giving the ability and ease of getting information displayed in a wide variety of ways. Unfortunately as versatility, grows the susceptibility to errors also increases. These errors can come from shorted lines due to crossed wires when devices are plugged into the system, they can also come from ESD damage. The SN75186 can be used to find out where faults on the line are and to a certain limit diagnose these faults.

For example, when put in loopback mode, the SN75186 used to interface to the printer can detect a fault on the printer line and feedback an error signal to the controlling µC alerting the user of the system. The SN75186 could then be driven to a state where the minimum amount of damage to the system and device could be done. For optimum protection the SN75186 could be used off separate supplies and could be switched off. The SN75186 can be used to detect faults for all the peripheral elements.

So ultimately the SN75186 provides the system with ability to meet the requirements of the EIA-232-D, EIA-232C and V.28 standards, as well as providing the system with a much higher level of fault protection/detection in an integrated circuit form. This saves on long term reliability and costs.

Notes

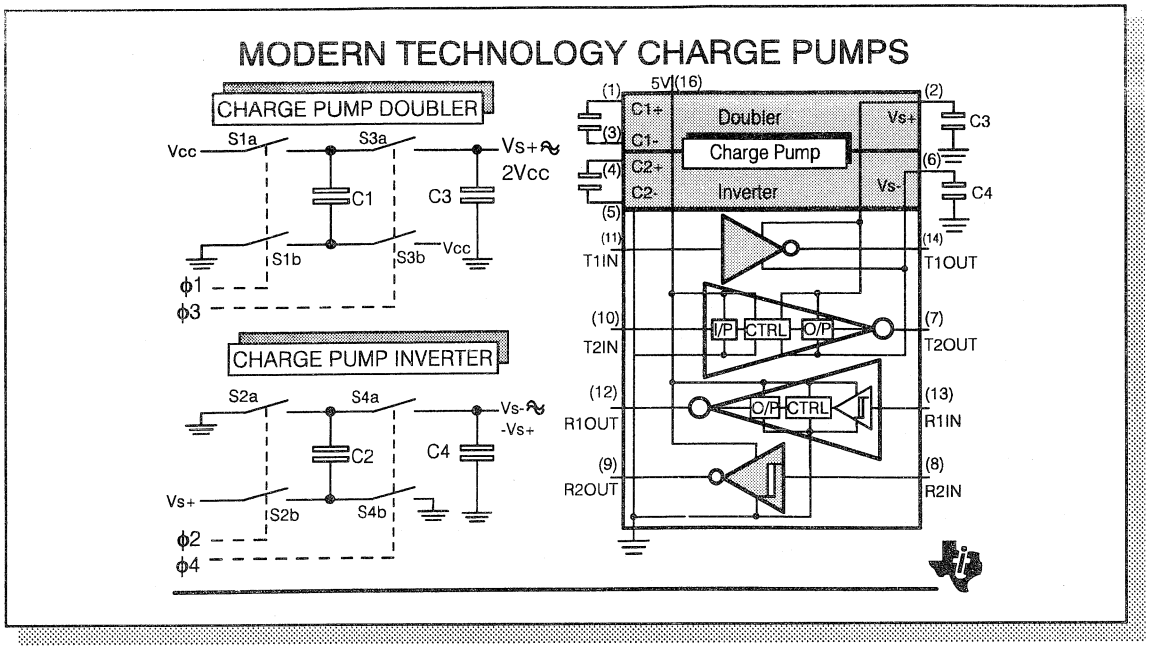


Figure 18 - Modern Technology Charge Pumps

One recurring problem that has often been problematic for EIA-232 users has been the necessity for dual supply rails; that is +12V and -12V. This is in addition to a 5V supply rail, meaning that a total of three regulators are required, the largest being the 5V. Linear regulators can only step down voltages, so it is not possible to convert the 5V supply to a 12V supply, nor can they invert the supply's polarity. The first regulators capable of performing such tasks are inductive switching regulators, but these can be noisy and require a lot of peripheral passive components. Another drawback, particularly for system integration is the large inductor and the power switch required. No one has yet been able to integrate inductors onto monolithic integrated circuits (except by the use of gyrators!).Therefore, until recently no cost effective solution for EIA-232 power supply generation has been available.

An alternative way, and the basis of modern technology charge pumps, is to make switching regulators using capacitors. In essence they operate by applying charge to a capacitor via an input voltage and then adding, subtracting or inverting the voltage on the positive or negative voltage terminals. This charge is then transferred into a holding reservoir capacitor which is then used to supply the output voltages. Furthermore such a scheme can be integrated into silicon. The network of capacitors shown in the figure both voltage doublers and inverters can be made.

Charge Pump Operation

Charge pump operation is best explained as a series of phases; There are 4 phases used which provide the clocking signals to control the distribution of charge. Phases 1 and 3 are used to provide voltage doubling and phases 2 and 4 provide voltage inversion.

Phases 1 and 3

During phase 1 the first pair of switches (S1a and S1b) close allowing capacitor C1 to charge up via Vcc. C3 supplies the load current. During phase 3 switches S1 open and switches S3 close thus transferring the charge stored in C1 on top of the supply voltage. This means that relative to ground the voltage on the top plate of C1 is now twice Vcc. The charge on C1 now charges up C3 in addition to supplying the load current. This process, assuming ideal switches, doubles the supply voltage.

The doubled voltage is now applied to a further bank of switches and capacitors to provide voltage inversion. This operation, phases 2 and 4 are similar in operation to phases 1 and 3.

Using this technique it is possible to convert the 5V digital supply to a positive 8.5V supply and a negative 8.5V supply.

This form of regulator, now known as a **Charge Pump** has not only been integrated onto silicon, but has also been coupled with EIA-232 drivers and receivers to make a EIA-232 line interface system capable of working from a single supply.

T.I. has two variants of such a device available; the **LT1080/1** and the **MAX232** both of which are becoming industry standard devices. Although working on similar principles they use different technologies, and the choice of technology can have a large effect on the overall performance of the system, just as it has in logic systems.

The original version of the MAX232 was fabricated in a CMOS process. This can cause reliability problems due to an inherent thyristor structure giving latch-up susceptibility.

In order to meet the relatively large currents and/or voltages required by data transmission circuits CMOS technologies need large geometries and large area output devices. The large geometries enable the devices to withstand higher voltages while the large area enables the device to pass larger currents. The larger the area of the device the larger the parasitic capacitance associated with the device. This means that with CMOS processes there will be a voltage, current , speed and cost compromise. The higher the current the harder it can be to provide the speed.

To overcome many of these problems TI fabricated its MAX232 product using the LinBiCMOS process. The advantages of the LinBiCMOS process have been discussed at length in earlier sections.

Notes

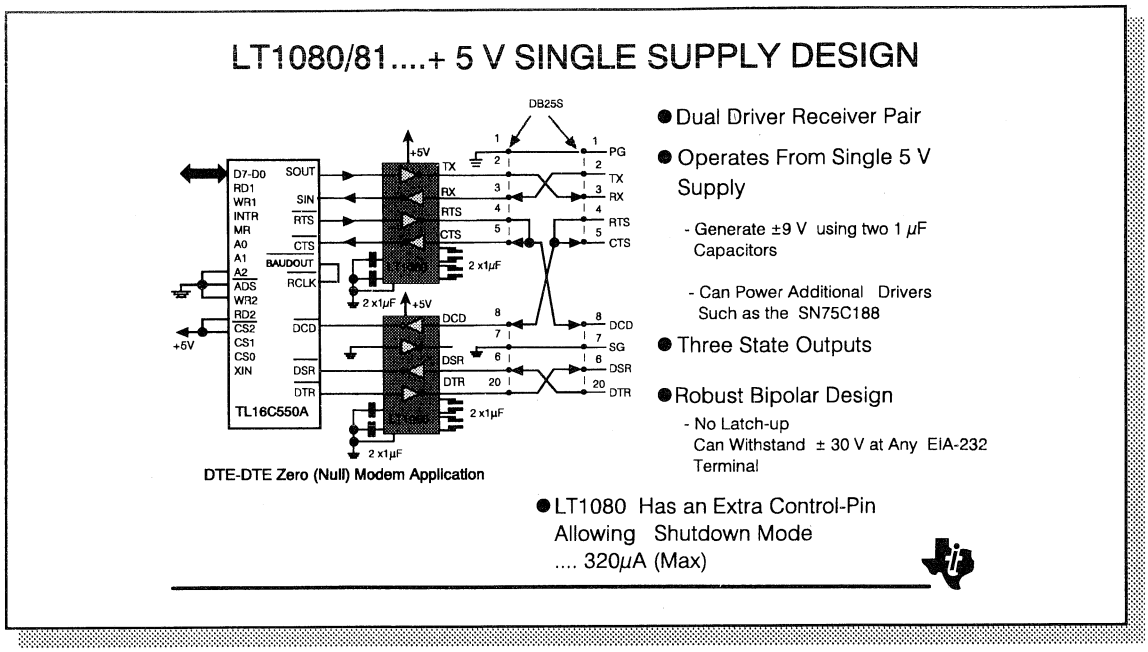


Figure 19 - LT1080/81...For Single 5V Supply Operation

In pure digital systems where no +/-12V supplies are available, a key requirement is for EIA-232 devices to operate from a single +5V supply. This can be achieved by EIA-232 devices with an internal charge-pump to step-up and invert a +5V supply voltage to +/-10V supplies to ensure that the minimum +/-5V voltage swing on the EIA-232 line can be achieved.

LT1080 and LT1081 are dual driver/receiver pairs featuring an internal charge-pump which facilitates single supply operation. Two 1µF capacitors are required for the charge pump operation and two additional 1µF capacitors are used for smoothing of the generated dual voltages. These devices are designed to avoid latch-up and provide a realistic balance between CMOS levels of power-dissipation and real-world requirements for ruggedness. The driver outputs are fully protected against overload and can be shorted to ± 30V.

The charge-pump provides enough current for driving low power external circuitry such as other EIA-232 drivers or op amps. However, they should be loaded with care, since excessive loading can cause the generated supply voltages to drop, causing the EIA-232 driver output voltages to fall below EIA-232 requirements.

The LT1080 features a shut-down mode that, in addition to a power reduction, puts both the driver and receiver outputs in high impedance states. This allows for several devices to share a receiver and driver line. Although the EIA-232-D makes no provisions for a transceiver configuration the LT1080 makes one possible.

In the application shown the LT1080 is a DTE to DTE communication link (also called a "zero or null modem" application.) All data and handshake lines are cross coupled. The ACE (TL16C550A) has 16 bytes receiver and transmitter FIFOs which reduces the number of interrupts to the microprocessor.

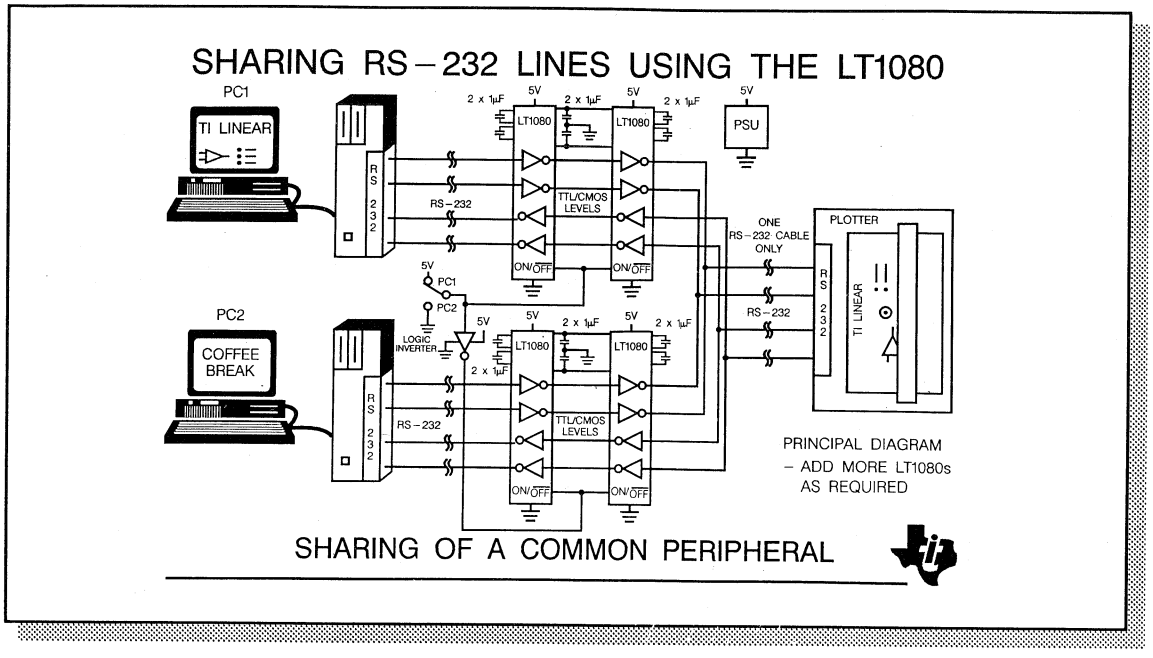


Figure 20 - Sharing EIA-232 Lines Using The LT1080

Tri-State Operation

Placing the LT1080 in **shutdown mode** by taking the ON/$\overline{\text{OFF}}$ pin **low** reduces the supply current into its V_{CC} pin to less than 100µA. In addition, enabling shutdown puts both the EIA-232 driver and receiver outputs in a high impedance state with leakage currents below 100µA and 10µA respectively. Control of the shutdown mode is simple since the ON/$\overline{\text{OFF}}$ pin is CMOS/TTL compatible, with a logic **high** fully enabling the device.

The virtual zero current consumption in shutdown mode can benefit power conscious systems in data off periods. However, this feature also allows drivers and receivers from different devices to share common EIA-232 lines, opening up new applications areas. Shifting between the two modes takes approximately 1ms.

Notes

Sharing of A Common EIA-232 Peripheral

Parallel connection of driver outputs and receiver inputs of two LT1080, and enabling /disabling them with an alternating control scheme allow two DTEs to share a common peripheral.

The example illustrated shows two PCs both having access to a common plotter through the same EIA-232 cable. If the plotter is not used frequently, even a simple manual switch at the PC side of the data communications cable is acceptable for shifting the plotter EIA-232 link from one PC to the other. This method is more reliable and convenient than fumbling with cables on the back of PCs to change the plotter host. When peripherals need more than two driver lines and two receiver lines just add more LT1080s.

Sharing EIA-232 lines in this fashion can be transferred to many other application areas, bearing in mind that such inter-connections are not covered by the EIA-232-D. Care should also be taken since excessive loading of a driver with more than one receiver's input impedance can cause the driver's output voltage swing to fall below EIA-232 requirements. In the application shown, where two PCs share a common peripheral, the additional output drive requirements are on the plotter side.

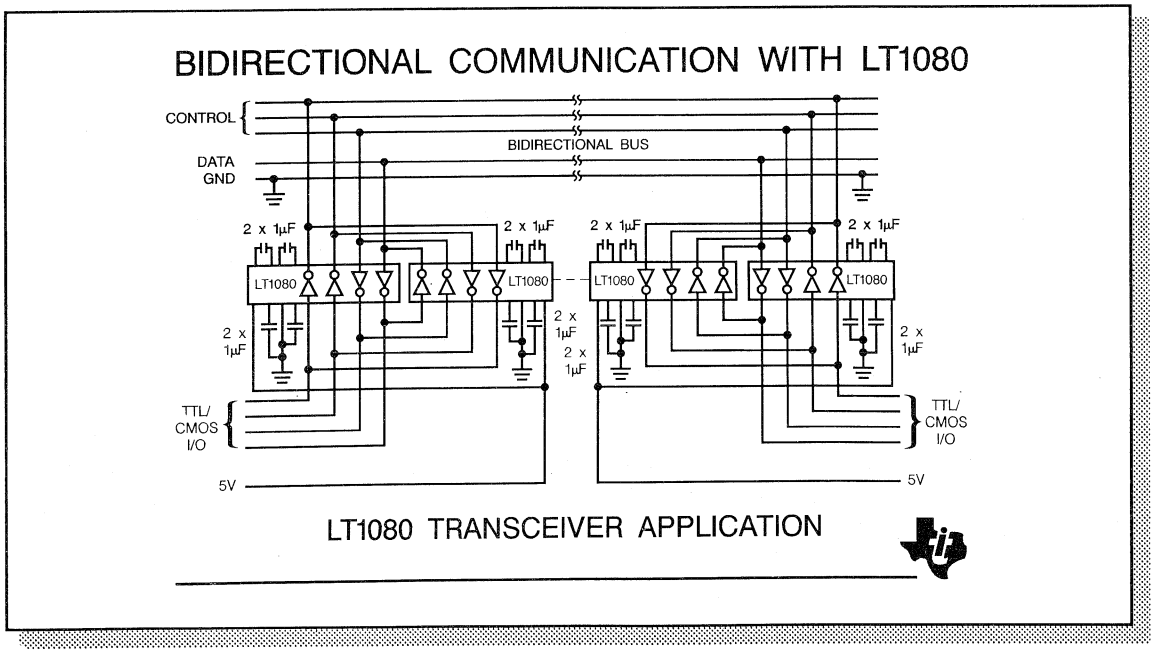


Figure 21 - Bidirectional Communication with LT1080

Connecting the driver outputs of one LT1080 to the receiver inputs of another, and vice versa, and using their power ON/ $\overline{\text{OFF}}$ function allows the LT1080 to operate as a true transceiver, enabling bidirectional communication.

Parallel connecting both driver outputs and inputs as well as receiver inputs and outputs of two LT1080 - and enabling/disabling them with an alternating control scheme allows true transceiver operation for bidirectional communication.

LT1080 Transceiver Application

The example illustrated shows two DTEs, each implemented by two LT1080s in transceiver mode, sharing four bidirectional lines. Three of the lines are used for handshaking while the is for data, but all are bidirectional. Theoretically, more than two stations can be connected to the communication line to form a low data rate mini-LAN, but each driver needs to be capable of driving all receiver inputs simultaneously. As EIA-232 devices are not designed for this purpose, care should be exercised to ensure that enough drive capability is available to pass through the receiver's input threshold region with an acceptable slew rate to reduce susceptibility to noise. In applications where the LT1080 drivers are driving two receiver inputs, worst case datasheet parameter designs mean that conformance to minimum EIA-232-D line level requirements can not be guaranteed. However in tests conducted on this application the communication worked perfectly.

Notes

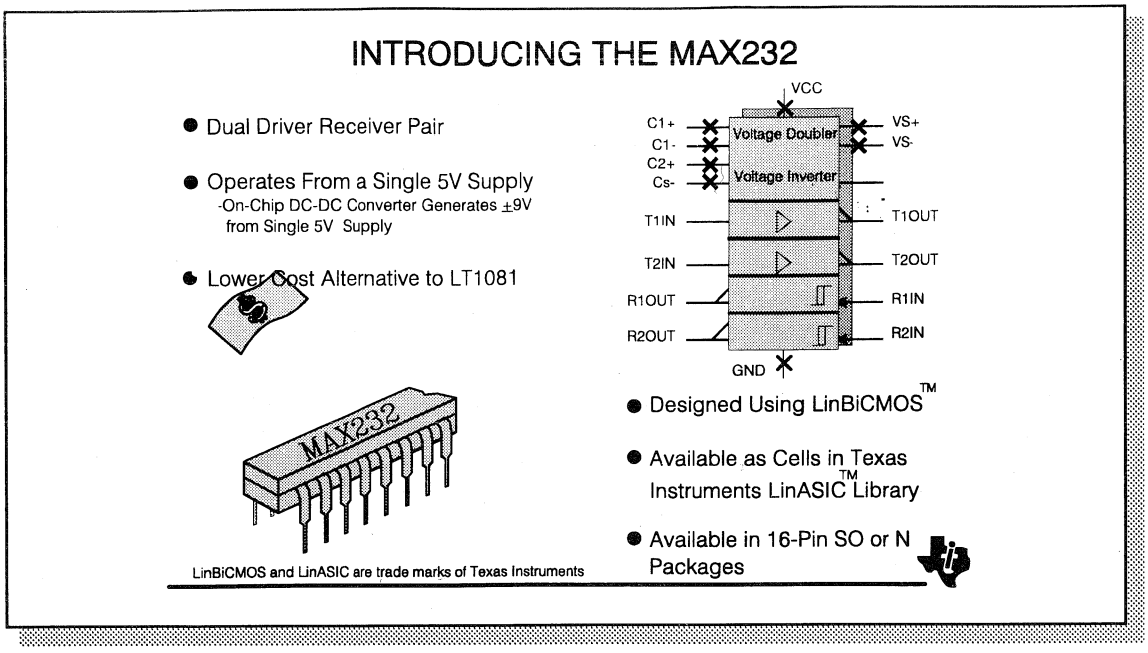


Figure 22 - MAX232

For more cost sensitive applications the MAX232 may be preferred. The MAX232 is functionally equivalent to both the LT1080 and the LT1081 and shares the same pin-out as the LT1081.

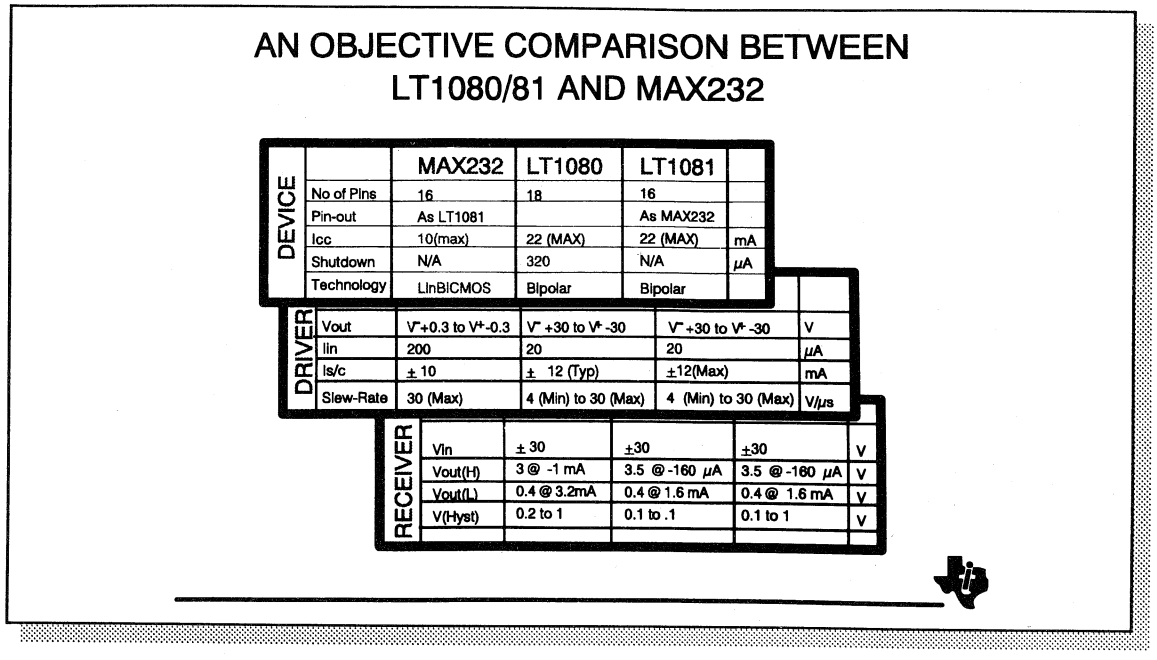
The MAX232, designed using Texas Instruments' LinBiCMOS™ process, is a dual driver/receiver that includes a capacitive voltage generator to supply EIA-232 voltage levels (Standard specifies a voltage between ±5 V to ±15V) from a single 5V logic supply.

Each receiver converts EIA-232 voltage level inputs to a 5V TTL/CMOS level. These receivers have a typical threshold of 1.3V and a typical hysteresis of 0.5V, and can accept ±30V inputs. Each driver converts TTL/CMOS input levels into EIA-232 levels.

LinASIC™ Cells

The driver, receiver and voltage generator functions are all available as cells in the Texas Instruments LinASIC™ cell library. This will allow future integration with more complex devices such as Texas instruments' range of ACEs.

LinASIC™ is a Trademark of Texas Instruments Incorporated.



		MAX232	LT1080	LT1081	
DEVICE	No of Pins	16	18	16	
	Pin-out	As LT1081		As MAX232	
	Icc	10(max)	22 (MAX)	22 (MAX)	mA
	Shutdown	N/A	320	N/A	µA
	Technology	LInBICMOS	Bipolar	Bipolar	
DRIVER	Vout	V⁻+0.3 to V⁺-0.3	V⁻ +30 to V⁺ -30	V⁻ +30 to V⁺ -30	V
	Iin	200	20	20	µA
	Is/c	± 10	± 12 (Typ)	±12(Max)	mA
	Slew-Rate	30 (Max)	4 (Min) to 30 (Max)	4 (Min) to 30 (Max)	V/µs
RECEIVER	Vin	± 30	±30	±30	V
	Vout(H)	3 @ -1 mA	3.5 @ -160 µA	3.5 @ -160 µA	V
	Vout(L)	0.4 @ 3.2mA	0.4 @ 1.6 mA	0.4 @ 1.6 mA	V
	V(Hyst)	0.2 to 1	0.1 to .1	0.1 to 1	V

Figure 23 - An Objective Comparison Between LT1080/81 & MAX232

The differences between the LT1080/81 and MAX232 have been some what eroded with the advent of Texas instruments' LinBiCMOS™ process. There are however still some differences which will be of importance for certain applications. These key differences are described below;

For EIA-232 purists (the EIA-232 standard does not specify 3-state conditions) MAX232 represents the best option for low power applications , with a driver and receiver quiescent current of just 10 mA (the line current needs to be added to give the total current drain).

If however the drivers/receivers are inactive for long periods, then a 3-state (shut-down) feature may be preferred. In 3-state mode the line is in effect disconnected, resulting in negligible line current .

Notes

The LT1080 contains such a feature, applying a logic low to the LT1080's ON/$\overline{OFF}$ pin places the receivers and drivers of the device into a high impedance state. A logic high will restore the device to normal operation.

The current consumed during shut-down can be calculated as follows;

$$2 \times \{I_{OZ\ (Driver)}\} + 2 \times \{I_{OZ(Receiver)}\} + I_{CC(Off)}$$

$$\{2 \times 100.10^{-6}\} + \{2 \times 10.10^{-6}\} + 100.10^{-6} = 320\ \mu A$$

The LT1080/81, as you would expect from a totally bipolar process, has a slightly wider output voltage range, making it more suitable for applications operating in electrically hostile environments. The voltage range is specified from V- +30V to V+ -30V, meaning that if the supply output voltages are ± 9 V, then external voltages of up to ± 21 V can be applied to the driver outputs without incurring device damage.

One final difference is in the receiver TTL/CMOS drive capability. The drive capability relative to a standard TTL gate requiring an I_{IH} of 40 µA and an I_{IL} of -1.6mA is shown below;

Parameter	MAX232		LT1080	
		Fan-out		Fan-out
$I_{(OH)}$	-1mA	25	-160 µA	4
$I_{(OL)}$	3.2mA	2	1.6mA	1

From the table above, for worst case design, the MAX232 has the greater current drive capability with a fan-out of 2. This would also imply that longer lines could be driven by the MAX232, but differences would be minimal.

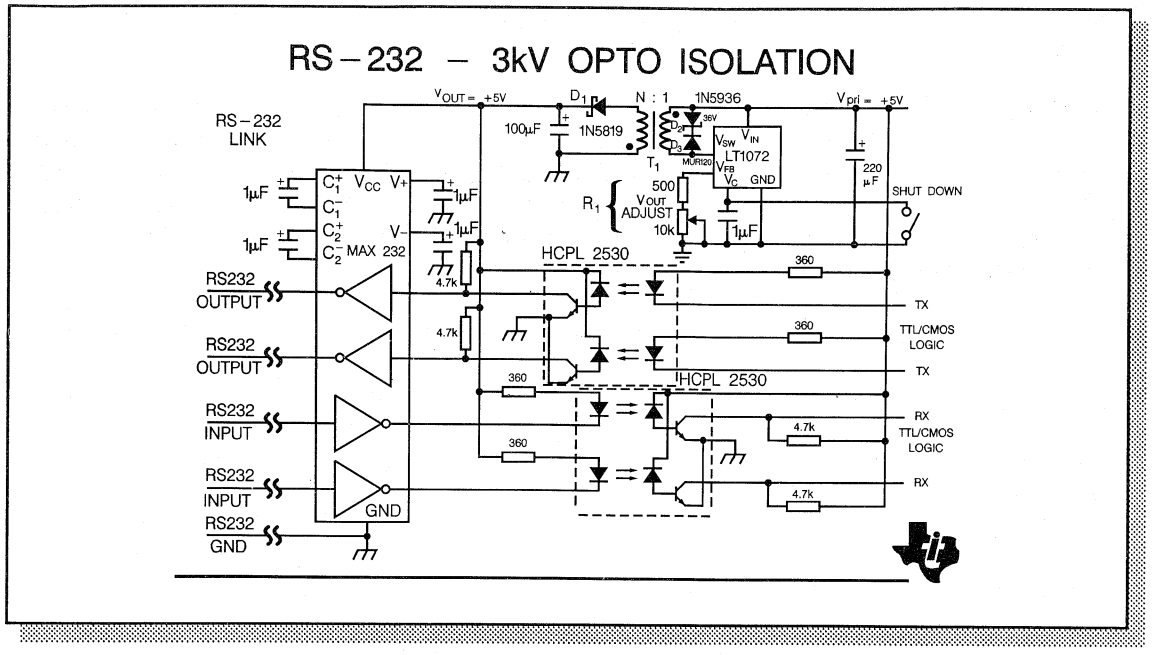


Figure 24 - EIA-232..... 3kV Opto Isolation

The Need for Galvanic Isolation

The capability to meet toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any EIA-232-D interface is galvanic isolation.

Such isolation in data communication systems is achieved without direct connection or wires between the EIA-232 interface devices and the DTE/DCE. Magnetic linkage from transformers provide the power for the system and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which can affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

Notes

To take a more practical view, two examples are mentioned, where problems are likely to occur without an isolated interface:

Firstly, when using an EIA-232 line to connect two pieces of equipment placed in different rooms or buildings, the ground potentials can differ by several volts. An indication of a possible problem is if a spark is seen at the connector housing, when joining these "grounds" with an EIA-232 cable. The spark itself may be harmless, but fluctuating levels of noise current should be expected when the cable is connected. With a high enough level, these noise currents may cause unreliable or faulty data transmission.

Secondly, in manufacturing environments where an EIA-232 link connects a data logger to a host computer and large motors are used, problems are also likely to happen. When a motor is started up, it can induce a momentary substantial difference in ground potentials at the data logger and the computer due to surge current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and at worst damage to the computer occur.

Simple Opto Isolated EIA-232 Design

The EIA-232, 3kV opto isolation application shown has two galvanic barriers; a transformer, T_1, providing magnetic transfer of power to the EIA-232 dual driver and receiver, MAX232, - and two dual opto couplers, HCPL2530, making an isolated data path available.

The circuit used is applicable to other Texas Instruments' EIA-232 drivers and receivers than the shown MAX232. However, in many industrial applications, a simple CTS, DTR handshaking scheme is adopted, which suits two drivers and two receivers. If more handshaking lines are required, the MAX232's built-in charge pump can also drive a SN75C1406, triple driver and receiver.

Choosing R_1 as a fixed 500Ω resistor in series with a 10kΩ potentiometer allows for some adjustment of the output voltage. As the voltage according to (1) is not linear with R_1, an adjusted value of R_1 = 1.4kΩ resulting in V_{FB} = 0.359V, was found to give a good variation around 5V. This resistor value is then used as basis to determine the transformer's turns ratio, N, from (2):

$$N = \frac{5V + 0.4V}{16V + 7k\Omega\left(\frac{0.359V}{1.4k\Omega}\right)} = 0.303 ;$$

Varying R_1 between 500Ω and 10,5kΩ results, according to (1) and (3), in a secondary output voltage, V_{out}, range of 5.7V to 4.5V.

Details of the transformer design is outside the scope of this data transmission section but is important for achieving the overall switching regulator performance and isolation voltage requirements. Please refer to the datasheet and available literature on switching regulator transformer design.

A snubber network consisting of a fast turn-on, high break-down diode, D_3 and a 36V zener diode D_2, limits the magnitude of the leakage inductance spike. Using a zener diode rather than a resistor in parallel with a capacitor improves efficiency because it minimises the duration of the inductance spike. A schotty diode, D_1, in the secondary reduces the voltage loss to the output and increases efficiency.

To save power in data off periods the LT1072 shutdown function can be activated by shorting V_C to ground. This switch function can be implemented by a MOSFET transistor controlled by digital circuitry or software. The power consumption for the complete application is reduced to less than 1.25mW in shutdown mode.

Opto coupling performed by two Texas Instruments' dual HCPL2530 allows fast data transfer only limited by the MAX232's capability, typically in excess of 64kbaud. For lower data rates, HCPL2730 is adequate. A 3kV isolation voltage is provided by these couplers.

An isolated +5V supply for the MAX232 is generated from the +5V logic supply by Texas Instruments' LT1072 switching regulator. The LT1072 has no electrical connection to the load; instead, the circuit derives its feedback from the transformer's flyback voltage. This technique is often referred to as an isolated flyback regulator. The switching regulator needs to deliver only modest current levels (100mA) allowing a physically small isolation transformer. Although a +5V logic supply is assumed, flexibility of the design allows easy adaptation to other regulated or unregulated input levels, from 4.5V to 15V, by changing the 360Ω resistors to provide approximately 10mA current through the LEDs.

In the isolated feedback mode, LT1072 does not use the feedback pin to sense output voltage; instead it senses and regulates the transformer primary voltage during the LT1072's switch off time. This voltage is related to the output voltage, V_{out} by:

$$V_{out} = N * V_{pri} - V_f ;$$

Where, N = turns ratio of transformer, V_f = forward voltage of rectifying output diode and V_{pri} = primary voltage during switch off.

The secondary voltage will be stable if V_{pri} is regulated. LT1072 switches from normal mode (feedback provided from a potential resistor divider across the regulated secondary output) to regulated primary mode when the current *out* of the feedback pin, V_{FB}, exceeds ≅10μA. An

Notes

internal clamp holds the voltage, V_{FB}, on this pin at approximately 400mV. The resistor from the V_{FB} pin to ground is used to put the LT1072 in isolated feedback mode. V_{pri} is regulated to 16V +7kΩ(V_{FB}/R_1), where the 16V is the LT1072's internal flyback mode reference voltage, V_{FB}/R_1 is equal to the current through R_1, and the 7kΩ is an internal resistor. V_{out} is therefore given by:

$$V_{out} = N\left[16V + 7k\Omega\left(\frac{V_{FB}}{R_1}\right)\right] - V_f ; \quad (1)$$

Re-arranging the equation gives the turn ratio:

$$N = \frac{V_{out} + V_f}{16V + 7k\Omega\left(\frac{V_{FB}}{R_1}\right)} ; \quad (2)$$

The feedback pin voltage, V_{FB} is about 0.4V for R_1 = 8.2kΩ, but the actual voltage depends on resistor value since the feedback pin has about 200Ω output impedance in this mode. From this information V_{FB} can be found to be given by:

$$V_{FB} = 0.41V\frac{R_1}{200 + R_1} ; \quad (3)$$

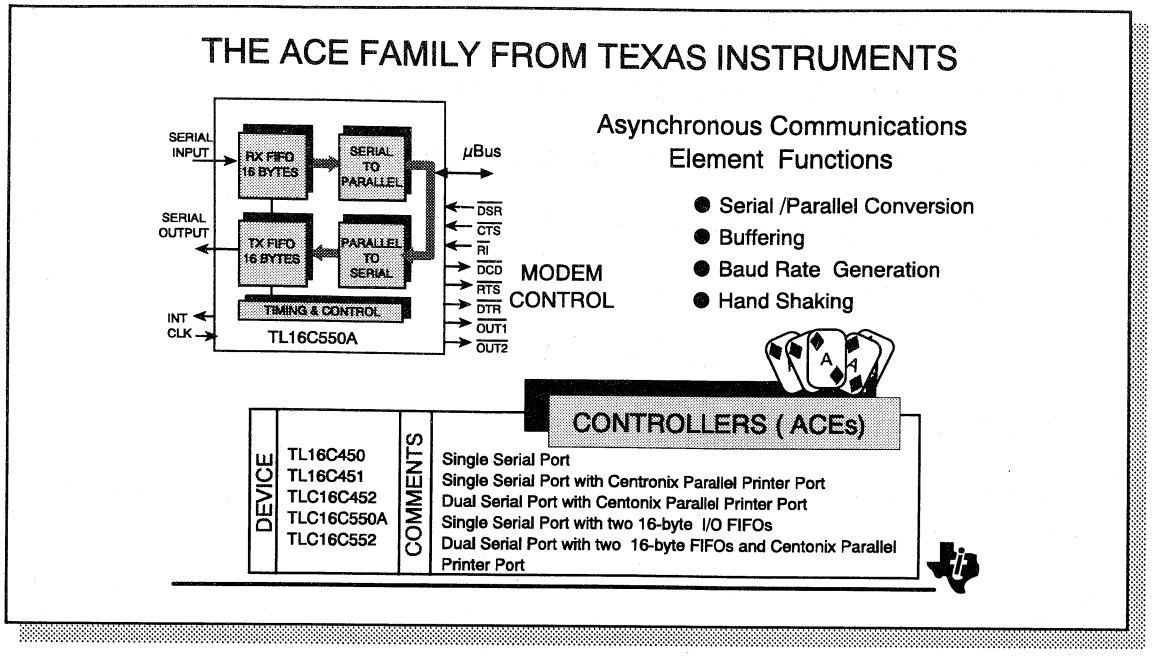


Figure 25 - The Texas Instruments ACE Family

Most EIA-232 systems use dedicated communication controllers. Termed ACE's (Asynchronous Communication Elements) or UARTs (Universal Asynchronous Receiver Transmitter) these devices are responsible for controlling the exchange of information over the EIA-232 interface.

The ACE

The ACE is a dedicated asynchronous communications controller designed to off load most of the communication activities from the CPU, thus freeing the CPU for other activities. It has the ability to add/delete start/stop bits and provide odd/even parity code generation and detection. Industry standard devices such as the *TL16C450* family contain many extra features as listed below;

Notes

- **Programmable baud rate generator**
- **Adds and deletes standard asynchronous communication bit**
- **Fully programmable serial interface characteristics**
- **Data communication diagnostic capability**
- **Modem control functions**
- **Simple interface to microprocessors**
- **Maximum data rate of 256kbits per second**

All devices are designed using Texas instruments' EPIC™ CMOS process and operate from a single 5 V supply.

The **TL16C450** is the most common choice for standard PC applications as well as many other asynchronous serial applications. The TL16C450, housed in a 40-pin package, contains all the necessary facilities for implementing a single asynchronous serial port. The CPU within the system can read and report on the status of the ACE at any point in the ACE 's operation. Reported status information includes; the type of transfer operation in progress, the status of the operation, and any error conditions encountered, parity, overrun etc.

The TL16C450 ACE includes a programmable, on-board, baud rate generator. This generator is capable of dividing a reference clock input by divisors from 1 to (2^{16} -1) and producing a 16 x clock for dividing the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the ACE is a complete modem control capability and a processor interrupt system that may be software tailored to the user's requirements to minimise the computing required to handle the communications link.

The **TL16C451** is similar to TL16C450 with the single serial port, but also contains a Centronix parallel printer port. The IBM© PC AT/XT sets the standard for this parallel printer interface which all "compatible" manufactures have to follow. TTL-level signals are presented on a 25 pin D-type socket. Apart from the choice of connector it is directly compatible with the "Centronix" standard printer interface.

The **TL16C452** has two serial ports plus a parallel Centronix printer port. Using this ACE together with two SN75C185s provides a simple 3 chip complete solution for the two EIA-232 ports plus a printer port which is common on basic PC configurations.

The FIFO (First In First Out)

The CPU can send data at much faster rates than a normal ACE can handle, this is particularly true for today's multitasking applications which demand high performance microprocessors. This can be expensive in CPU overheads as the CPU will be tied to the

speed of the serial interface, ie data will be transferred over the interface through the ACE and onto the CPU bus. This is true also when the data is exchanged from the CPU to interface via the ACE.

Devices like the **TL16C550A** and **TL16C552** alleviate this problem by including buffer registers, FIFOs in series with the ACE's transmitter and receiver. These are quick access registers which hold data until the CPU can be freed. The CPU can then execute a block read or write.

The ACE is, in effect, isolated from the slow communications channel.

The TL16C550A is similar to the TL16C450, but two 16 bytes FIFOs are included to buffer the transceiver and receiver data stream, further reducing the number of interrupts from the microprocessor.

Forward Looking Performance With Backward Compatibility

By allowing two modes of operation the TL16C550A allows users to maintain software compatibility with earlier industry standard ACEs such as the TL16C450. In addition to TL16C450 mode the TL16C550A can operate in FIFO mode. In FIFO mode, two 16-byte FIFOs (First In First Out) are enabled, to relieve the CPU of excessive software overheads. The independent receive and transmit FIFOs act as buffers, vastly reducing the number of interrupts required. Furthermore two dedicated pins serve as handshaking lines to a DMA (Direct Memory Access) controller, thus allowing the FIFOs to load and unload data without direct intervention from the CPU.

The flagship of the range is the TL16C552, which is similar to the TL16C452 in structure but with the added advantage of input/output FIFOs as in the TL16CC550A .

The device serves two serial input/output interfaces simultaneously in either microcomputer or microprocessor based systems. In addition to its dual asynchronous serial communication capabilities, the TL16C552 provides a fully bidirectional parallel data port that fully supports the parallel Centronix type printer. The parallel port and the two serial ports provide IBM PC/AT compatible computers with a single low-power device to serve the three port system. Like the TL16C550A, the TL16C552 contains 16-byte receive and transmit FIFOs which act as buffers to reduce the number of interrupts on the CPU. Also in common with the TL16C550A the device contains two pins for each ACE which serve as handshaking lines for DMA control.

Notes

The TL16C552 is housed in a 68-pin plastic leaded chip carrier, PLCC.

Integration of FIFO and DMA signalling circuitry onto a single chip makes the TL16C550A and TL16C552 one of the most efficient solutions for higher performance multitasking systems.

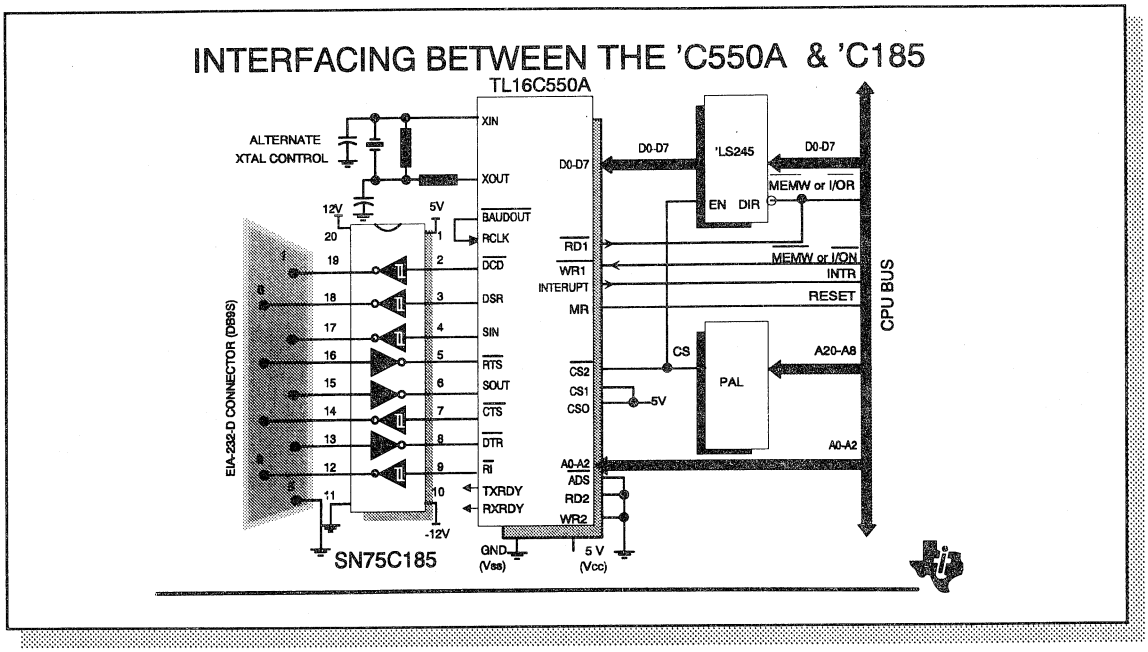


Figure 26 - Interfacing Between TL16C550A and SN75C185

The circuit shown demonstrates the simplicity, in hardware terms, in implementing an asynchronous serial interface when the SN75C185 driver/receiver and the communications controller TL16550A.

When interfacing between the TL16C550A ACE and the Intel CPU bus, minimal glue logic is required. Namely a 'LS245 Octal bus transceiver, to provide drive current to an 'off-card' CPU, and a PAL to decode address lines and generate a chip select signal.

While an exhaustive description of this interface is beyond the scope of this section, a discussion of key interface lines is interesting and can be useful.

Xin/Xout: External clock. Connects the ACE to the main timing reference (clock or crystal).

$\overline{\text{baudout}}$, RCLK: The transmitter reference clock is available externally via the $\overline{\text{baudout}}$ pin. In this application baudout is fed into the receiver clock to provide a timing reference for the receiver circuitry. Clock rate is established by the reference oscillator clock frequency (xin) and divided by a driver specified by the baud generator divisor latches.

$\overline{\text{TXRDY}}$: Transmitter Ready Output. This pin is used during DMA signalling.

$\overline{\text{RXRDY}}$: Receiver Ready Output. This pin is also used during DMA signalling.

D0 to D7: Databus. Eight 3-state data lines provide the bidirectional path for data, control and status information between the ACE and CPU bus.

$\overline{\text{RD1}}$, RD2: Read inputs. When either input is active (high or low respectively) during ACE selection, the CPU is allowed to read status information from and selected ACE register. Since only one of these inputs is required for the transfer of data during and read operation, RD2 is tied to its inactive state, i.e.: low.

$\overline{\text{DCD}}$, $\overline{\text{DSR}}$, SIN, $\overline{\text{RTS}}$, SOUT, $\overline{\text{CTS}}$, $\overline{\text{DTR}}$, $\overline{\text{RI}}$:

These signals are the EIA-232 Compatible modem control lines. Devices such as the SN75C185 are employed to convert the TTL/CMOS level signals from the ACE to EIA-232 compatible bipolar voltages of between +/-5V to +/-15V. The signal can then be transmitted over distances of up to 15 metres.

The advantages of the SN75C185 can be clearly seen by the simplicity of the interface connections. For example; driving/receiving combinations precisely match the interface requirement plus the pin-out is aligned directly to the DB9S connector.

$\overline{\text{WR1}}$, WR2: Write inputs. A logic applied to $\overline{\text{WRI}}$, during ACE selection allows the CPU to write either Control words or data into a selected ACE registers. WR2 is tied in active, i.e: logic low.

INTERRUPT Interrupt. When active (high) the interrupt pin informs the CPU that the ACE has an interrupt to be serviced. This interrupt could occur for one of four reasons;

i) **Receiver error**

ii) **Received data available or timeout (FIFO mode only)**

ii) **Transmitter holding register empty**

iv **Enabler modem status interrupt**

Notes

The interrupt is reset (de-activated) either when the interrupt has been serviced or by a master reset (MR).

MR: Master reset. When active (high) MR clears most ACE registers and sets the states of various outputs (i.e.: interrupt).

CS0, CS1, $\overline{\text{CS2}}$: Chip Select. An active low on the $\overline{\text{CS2}}$ pin selects the ACE. CS0 and CS1 must be tied active (high) to ensure proper functioning of the $\overline{\text{CS2}}$ chip select. A logic high on $\overline{\text{CS2}}$ will de-select the ACE.

A0 TO A2: Register Select. These three inputs are used during read or write operations to select the appropriate ACE registers. For example: providing the correct write/read operation had taken place a logic 0 at A2, A1 and A0 would cause the receiver buffer (read) or the transmitter buffer to write.

$\overline{\text{ADS}}$: Address strobe. An active low on $\overline{\text{ADS}}$, the register select signals (A0 TO A2) and chip select signal ($\overline{\text{CS2}}$) drive the internal logic directly.

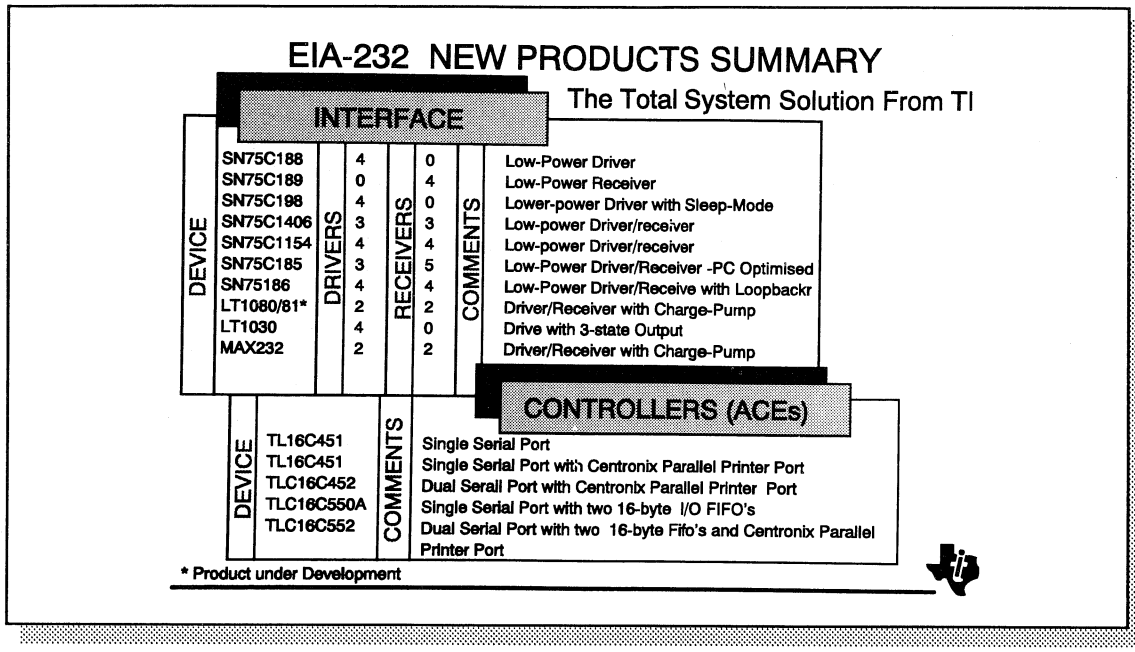


Figure 27 - EIA-232 New Product Summary

Texas Instruments is continually developing new products in support of the EIA-232 standard. As can be seen from the products discussed, particular emphasis has been placed on devices offering high levels of system integration, optimisation and robustness of design. All designs have been made with today's low-power requirements in mind. Detailed discussion of all key parameters is beyond the scope of this text, so for more detailed information and an overview of Texas instruments' complete range of devices the reader's attention is drawn to the 1991 Interface Circuits Data Book. The following table shows the current range of devices for the EIA-232 standard.

Notes

DEVICE FUNCTION	DEVICES PER PACKAGE	DEVICE TYPE
Line Drivers	2	SN75150
		UA9636AC
	4	LT1030
		SN55188
		SN65C188[1]
		SN65C198[1]
		SN75188
		SN75C188[1]
		SN75C198[1]
Line Receivers	4	SN75154
		SN55189
		SN55189A
		SN65C189[1]
		SN65C189A[1]
		SN75189
		SN75189A
		SN75C189[1]
		SN75C189A[1]
Line Driver/Receiver	1/1	SN75155
	2/2	*MAX232*
		LT1080[2]
		LT10801[2]
	3/3	SN65C1406[1]
		SN75C1406[1]
	4/4	SN75186[1]
		SN65C1154[1]
		SN75C1154[1]
	3/5	SN65C185[1]
		SN75C185[1]

Notes: 1. New product release
2. Product under development

Of particular note is not only the range of products on offer but that both line driving/receiving functions and controller elements are supported - ***a total system solution.***

Future developments will see an ever increasing use of the LinBiCMOS™ process, which by combining the benefits of both bipolar and CMOS will allow line driving/receiving functions to be integrated along with the high density controller functions.

Differential Data Transmission Standards

Specifications and Transmission Line Practicalities

Introduction

This section focuses on two of industries most widely used balanced transmission line standards, the EIA RS-422 and the EIA RS-485. After reviewing key aspects of these standards, the reader will be introduced to the practicalities of implementing a differential transmission scheme. Finally, several new additions to Texas Instruments EIA product range will be discussed and where appropriate, their application.

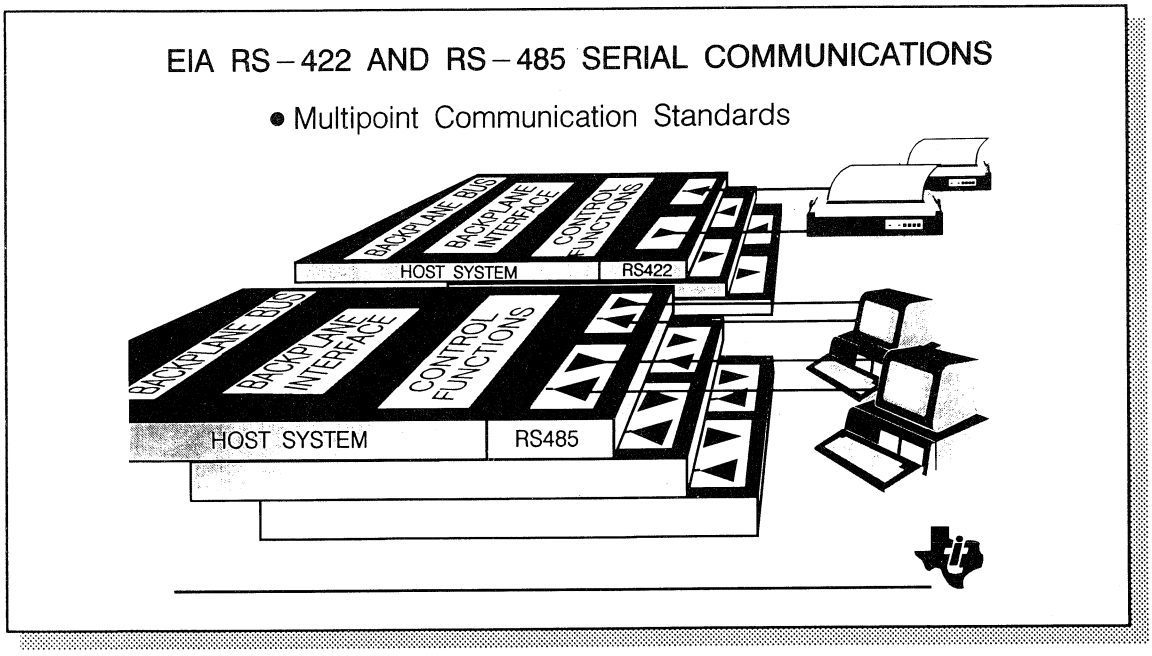


Figure 01 - EIA RS-422 and RS-485 Serial Communications

The Need for Balanced Transmission Line Standards

High speed data transmission between computer system components and peripherals over long distances, under high noise conditions, usually proves to be very difficult if not impossible with single-ended drivers and receivers. Recommended EIA standards for balanced digital voltage interfacing provide the design engineer with a universal solution for long line system requirements.

RS-422 and **RS-485** are balanced (differential) digital transmission line interfaces developed to incorporate and improve upon the advantages of the current-loop interface and improve on the EIA-232 limitations. The advantages are;

- **Data rate - to l0M baud and beyond**
- **Longer line length - up to 1200 metres**
- **Differential transmission - less noise sensitive**

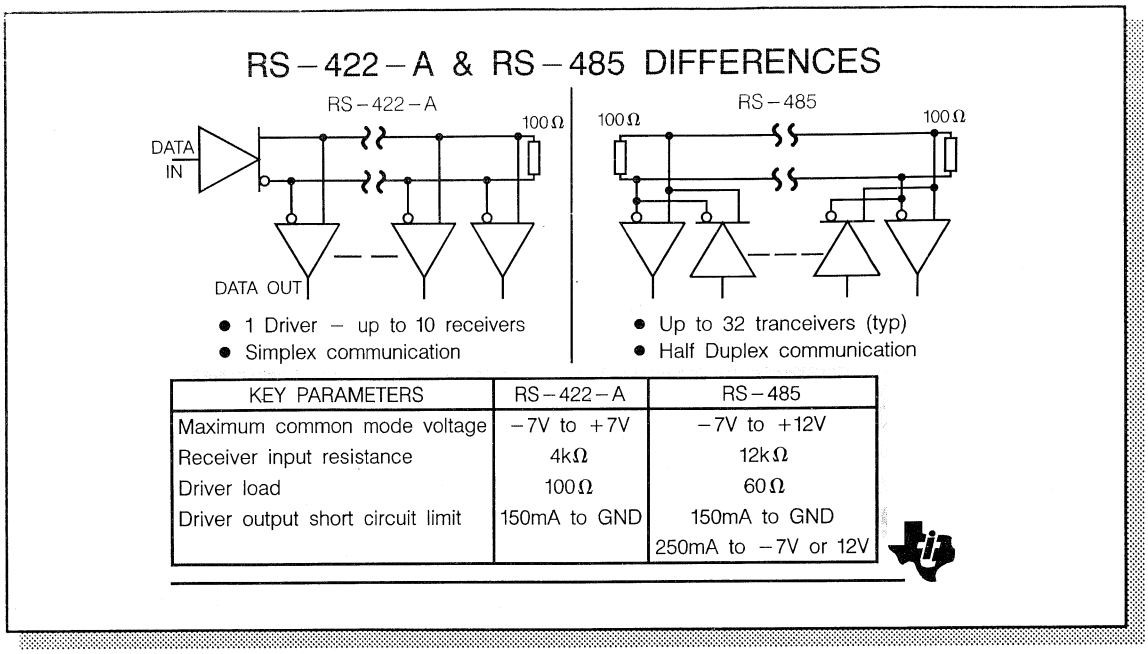
Application Areas

RS-422 offers a reliable multipoint one way communication. A typical application area is its use in transmitting data from a central computer to multiple remote monitors, printers or stations, such as airport arrival and departure monitors.

RS-485 is an upgraded version of RS-422 extending the number of peripherals and terminals that a computer can interface to, particularly where longer line length or increased data rates are called for. Additionally, RS-485 allows for bidirectional multipoint party line communication and can effectively be used for "mini-LAN" applications, such as data transmission between a central computer and remote intelligent stations. For example, between point of sales terminals and a central computer for automatic stock debiting.

As a result of its versatility an increasing number of standard's committees are embracing the RS-485 as the electrical specification of their standard. Examples include the ANSI (American Nationals Standards Insitute) Small Computer Systems Interface (SCSI).

Notes



KEY PARAMETERS	RS – 422 – A	RS – 485
Maximum common mode voltage	–7V to +7V	–7V to +12V
Receiver input resistance	4kΩ	12kΩ
Driver load	100Ω	60Ω
Driver output short circuit limit	150mA to GND	150mA to GND 250mA to –7V or 12V

Figure 02 - EIA RS-422-A and EIA RS-485 Differences

EIA RS-422-A

The balanced transmission line standard EIA RS-422 was developed in 1975 to interface a host computer's data, timing or control lines to its peripherals. The standard was revised (RS-422-A) in December 1978 bringing it in line with its present specifications.

A RS-422 line allows for only one way communication (simplex mode) but by using a differential twisted pair transmission media (not specified in std.) and a RS-422 receiver with its minimum 7V common mode voltage capability makes it less susceptible to noise picked up in hostile environments, via the long cables allowed by the standard. Each driver can drive up to 10 receivers. The specification in the standard places no restrictions on minimum or maximum operating data rates but rather on the relationship of transition speed to a unit interval. However, data rates up to 10M baud are supported and a line length up to 1200 metres is given as guide-line, but not at the maximum data rate.

When operating at low data rates (below 200k baud), or at any speed where the ratio of the driver's output rise time to the one-way propagation delay time of the cable exceeds ten, the cable will not act as a true transmission line and therefore termination is not absolutely necessary. Under all other conditions, the cable loading can no longer be considered as a lumped parameter but must be considered as a transmission line.

The characteristic impedance of twisted pair cable is a function of frequency and cable type, however typical twisted pair cable impedances lie in the range of 100Ω to 120Ω. A

termination resistor with an impedance similar to the cable's characteristic impedance should only be connected at the furthest end of the cable.

EIA RS-485

The Increased use of balanced data transmission lines in distributing data to several system components and peripherals over relatively long lines brought about the need for multiple driver/receiver combinations on a single twisted pair line. Hence, an upgraded version of EIA RS-422-A , named EIA RS-485, was introduced in 1983.

RS-485 takes into account RS-422 requirements for balanced-line data transmission plus additional features allowing for multiple drivers and receivers. The guide-lines for data transmission speed, cable lengths and media are the same as for RS-422.

The Differences

The differences between the RS-485 standard and the RS-422 standard lie primarily in the features that allow reliable multipoint communications.

Driver features

1. One driver can drive as many as 32 unit loads (one unit load is typically one passive driver and one receiver).

2. The driver output, off-state, leakage current shall be 100μA or less with any line voltage from -7V to +12V.

3. The driver shall be capable of providing a differential output voltage of 1.5V to 5V with common-mode line voltages from -7V to 12V.

4. Drivers must have self protection against contention (multiple drivers contending for the transmission line at the same time).

Receiver features

1. High receiver input resistance, 12kΩ minimum.

2. A receiver input common-mode range of -7V to 12V.

3. Differential input sensitivity of ±200mV over a common-mode range of -7V to 12V.

Notes

Line Drivers, Receivers and Transceivers for RS-422 and RS-485

Texas Instruments has a wide range of devices supporting these standards as specified in the following tables:

APPLICATION	DEVICE FUNCTION	DEVICES PER PACKAGE	DEVICE TYPE
EIA Standard RS-422-A	Drivers	2	SN75158
			SN75159
			SN75ALS191[1]
			μA9638C
		4	AM26LS31C
			AM26C31[2]
			MC3487
			SN75151
			SN75153
			SN75ALS192[1]
			SN75ALS194[1]
	Receivers	2	SN75146
			SN75157
			μA9637A
			μA9639C
		4	AM26LS32A
			AM26C32[2]
			MC4386
			SN75ALS193[1]
			SN75ALS195[1]

APPLICATION	DEVICE FUNCTION	DEVICES PER PACKAGE	DEVICE TYPE
EIA Standard RS-485 and EIA Standard RS-422-A	Drivers	4	SN75172
			SN75174
	Receivers	4	SN55173
			SN75173
			SN75175
	Transceivers	1	SN65LBC176[2]
			SN75LBC176[2]
			SN65176B
			SN75176A[1]
			SN75176B
			SN65ALS176[1]
			SN75ALS176[1]
			SN75ALS176A[1]
			SN75ALS176B[1]
			SN75177B
			SN75178B
			SN95176B
			TL3695
		3	SN75ALS170
			SN75ALS171
	Drivers / Receivers	1 / 1	SN75179B
			SN65ALS180[1]
			SN75ALS180[1]
		2 / 2	SN751177[1]
			SN751178[1]

NOTES: 1. New product release
2. Product under development

Detailed Description of Key RS-485 Specifications

The following text describes in some detail the key specifications embraced by the RS-485 standard.

Notes

Generator (Driver Characteristics)

The open circuit test (left in figure). Used to define the differential and single-ended voltage range for the logic states as follows:

For either logic or binary state, the magnitude of the differential voltage, V_O measured between the two driver output terminals shall be not less than 1.5V and not more than 6V; and the magnitude of V_{oa} and V_{ob} measured independently between each generator output terminal and generator circuit ground shall be not more than 6V.

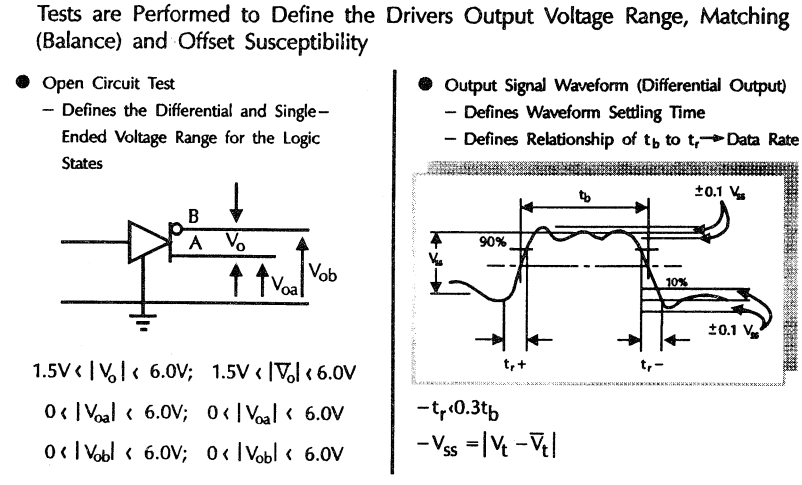


Figure 2a- Generator (Driver Characteristics)

The output signal waveform - differential output (right in figure). This defines both the waveform settling time and the relationship between the waveform unit interval (t_b) and the waveform rise time (t_r). It is this relationship which sets the limit on the data rate achievable using the RS-485 standard. (Note, the same rule applies for the RS-422 specification but with a relaxed ratio, see previous section). The differential output voltage measured across the test load, 54Ω in parallel with 50pF, should have a monotonic transition between the binary states. Thereafter, the signal voltage shall not vary by more than 10% from the steady state value of V_{ss} (the differential voltage between the two states of the generator output), until the next binary transition occurs. The instantaneous magnitude, V_t and $\overline{V_t}$ of either binary state shall not exceed V_{ss} or 5V.

RS-485 defines the maximum data rate of a device in terms of the transition time, t_r relative to one unit interval, t_b. If the transition time for a device is known then the maximum operating data rate, fb for RS-485 conditions can be calculated as follows:

$$t_r = 0.3\ t_b \quad \text{or} \quad t_b = t_r/0.3;$$

For example, the SN75ALS176 has a specified maximum transition rise time (t_r) of 8ns. At worst case the maximum data rate would be:

$$f_b = 0.3/(8ns) = \underline{37M \text{ baud.}}$$

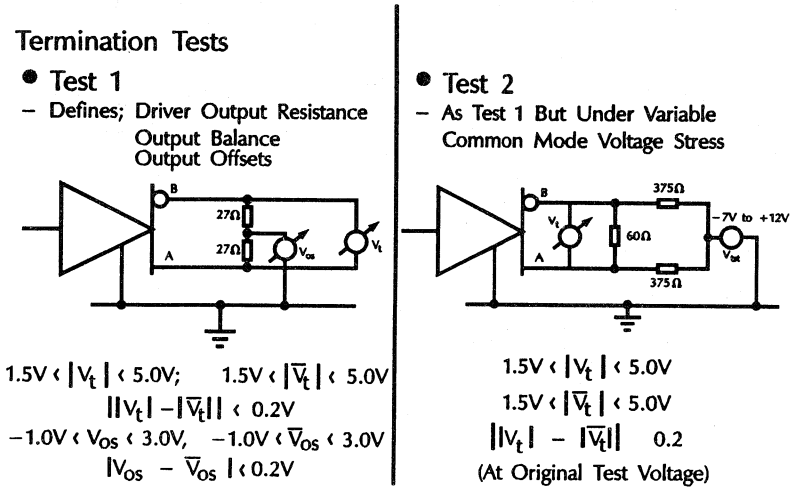


Figure 2b- Generator Tests Continued

There are two termination tests carried out; Test one defines the output resistance, balance and offsets of the driver. With the test load as shown, the magnitude of the differential voltages, V_t and the offset voltages, V_{OS} should be as specified. The balance, difference between the magnitudes of the differential outputs, of the driver should be within 200mV. Where the offset, or common-mode output, voltage of the driver should not be less than -1V and not more than 3V.

Test two is used to measure the magnitude of the differential voltages, Vt, under worst case common-mode signal (-7V to 12V) conditions. The circuit is loaded as shown on the righ hand side of the figure and should yield the results as stated.

Notes

Receiver Characteristics

The two main tests carried out on the receiver are the sensitivity test and the balance measurement used to give an indication of the receiver's ability to reject common mode signals.

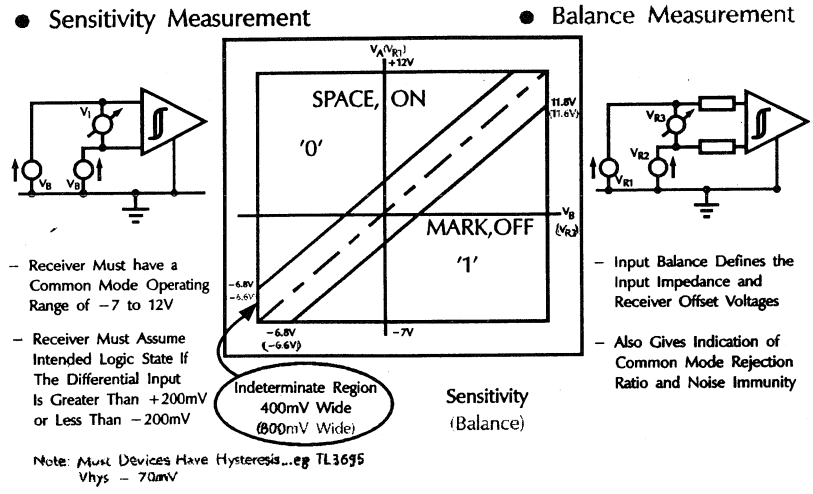


Figure 2c- Receiver Characteristics

Sensitivity and Balance Measurements

Sensitivity measurements. The maximum range of input voltages appearing at the receiver input terminals measured with respect to receiver common shall be between -7V and 12V. For any combination of receiver input voltages within the allowed range, the receiver shall assume the intended binary state with an applied differential input voltage of +/-200mV or more. To avoid faults from noise on slow rising/falling signals, receivers usually have hysteresis incorporated in to their input stages, E.g. TL3695 Vhys = 70mV.

Input balance measurements. This defines the input impedance and receiver offset voltage and gives an indication of how well a device rejects common-mode signals. With a test configuration as shown, a differential signal of +/-400mV is applied through two equal valued (1500 Ohm /(number of unit loads) series resistors. With this signal applied, the receiver output shall remain in the intended binary state throughout the -7V to 12V common-mode range.

Fault Conditions

The RS-485 standard has been designed with the realities of long distance and high data rate communication in mind. Therefore the standard takes great care in ensuring that adequate fault protection and robustness is built into devices claiming RS-485 conformance. Detailed in the following figure are just some of the tests used to ensure device robustness.

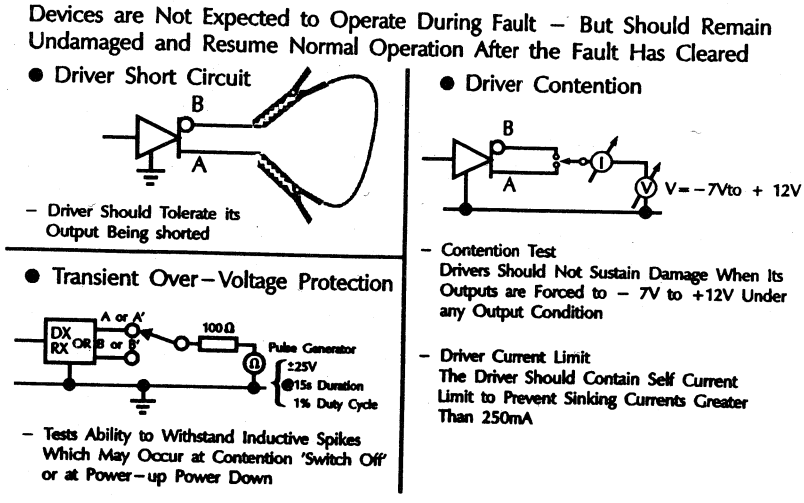


Figure 2d - Fault Conditions

However, it should be noted that even with the precautions taken by the RS-485 standard some applications demand even greater levels of fault protection and tolerance.Excessive and damaging voltage (more than +/-25V) stress on the receiver inputs can be clamped with appropriate circuitry - while excess common-mode voltage exceeding the maximum specified range (-7V to 12V) by the standard, can usually be avoided by effective grounding techniques and choice of shielded twisted pair cables as transmission media.

Notes

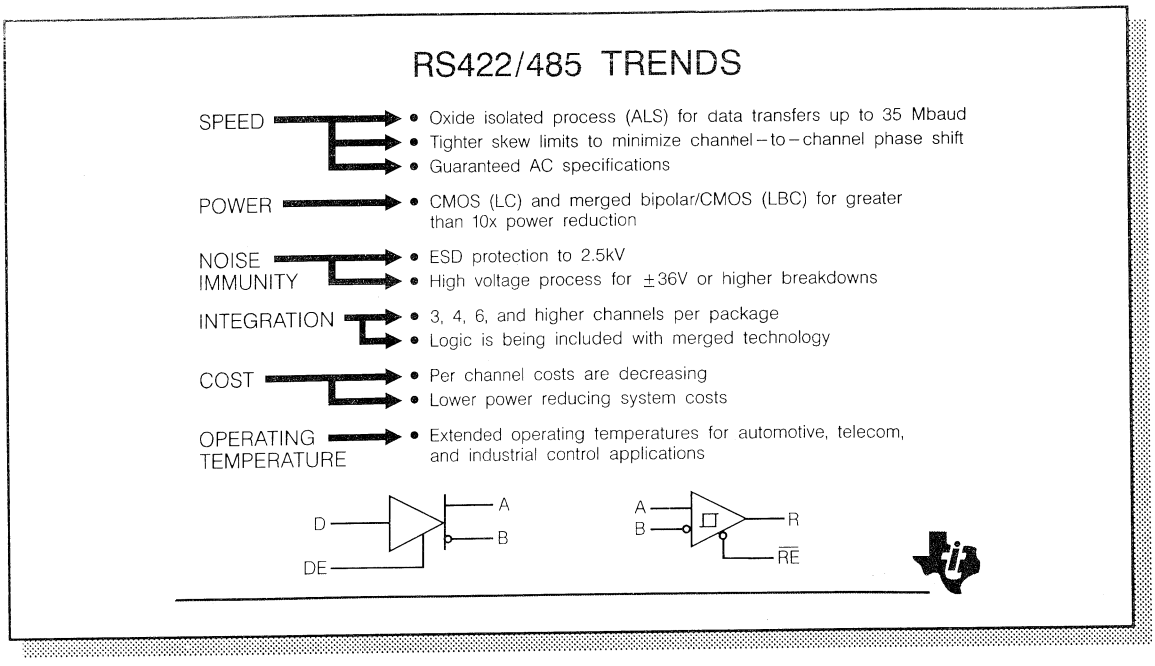


Figure 03 EIA RS-485 /422 Product /Application Trends

Many propriety systems designers are beginning to recognise the inherent advantages of a balanced, differential, transmission scheme over the single ended interface. Such advantages are higher noise immunity, lower noise emissions and improved signal quality. These facts are also not lost on independent standards committees which are starting to embrace RS-485 as the electrical part of their overall specification. Furthermore those systems not following the RS-485 specification verbatum are recognising the virtues of Texas Instruments' range of differential driver/receivers, particularly the high speed/low power ALS options.

Representatives of those standards bodies employing a differential transmission scheme can be found in most industries, some examples are listed below;

i) **Computer;** The ANSI-X3T9.2-1986 Small Computer Systems Interface (SCSI)
ii) **Computer;** ANSI X.3129-1986 Intelligent Peripheral Interface (IPI)
iii) **Automotive multiplex Wiring;** CAN, VAN and SAE J1850
iv) **Telecommunications;**
v) **Factory Automation;** P-Net (A derivative of Field bus)

Each one of these application areas makes its own demands on the processing technology used. Examples of these demands are guaranteed AC specifications and increased data rate capability. In particular, tighter skew specifications are needed for both telecommunication and computer applications, however the interpretation of skew can differ. For example, telecommunication applications are more concerned with device skew, that is the difference between the positive and negative edges of the differential output voltage. A low skew value in this case would represent a lower likelihood of noise radiation. For the

computer application, SCSI, a low bus skew is required. In a SCSI there can be as many 18 differential lines, obviously for timing purposes it is desirable to have low skew between each channel. For these types of applications a high speed bipolar process like the advanced low power scchottky would be required.

A key requirement across most application areas is low power consumption, particularly with the emergence of battery backed or operated equipments. This requires a low power technology, for example CMOS. However although fine for controller applications, CMOS is not generally suitable for line drive/ receive functions, here a more robust technology is needed, for example, a bipolar or merged technology like Texas Instruments' LinBiCMOS (combination of analogue bipolar and analogue CMOS).

Due to the increasing use of differential systems, particularly in electrically hostile environments, increased common mode voltage ranges and low susceptibility to ESD (Electro-Static Discharge) damage is required. Furthermore, extended temperature ranges are required particularly in automotive applications where the line drive/receive functions may be located under the car bonnet (hood). All new devices in Texas Instruments' range of line drivers and receivers contain temperature range options for both commercial, 0° C to 70°C and industrial, -40°C to 85°C. Some devices like the SN65076 have been designed especially for automotive applications by offering a -40°C to 105°C temperature range.

One final demand made by all types of equipment is for increased integration. Designers are requiring increased functionality from semiconductor chips and, perhaps an even more importantly require that these chips be less expensive than the solution(s) they replace.

Notes

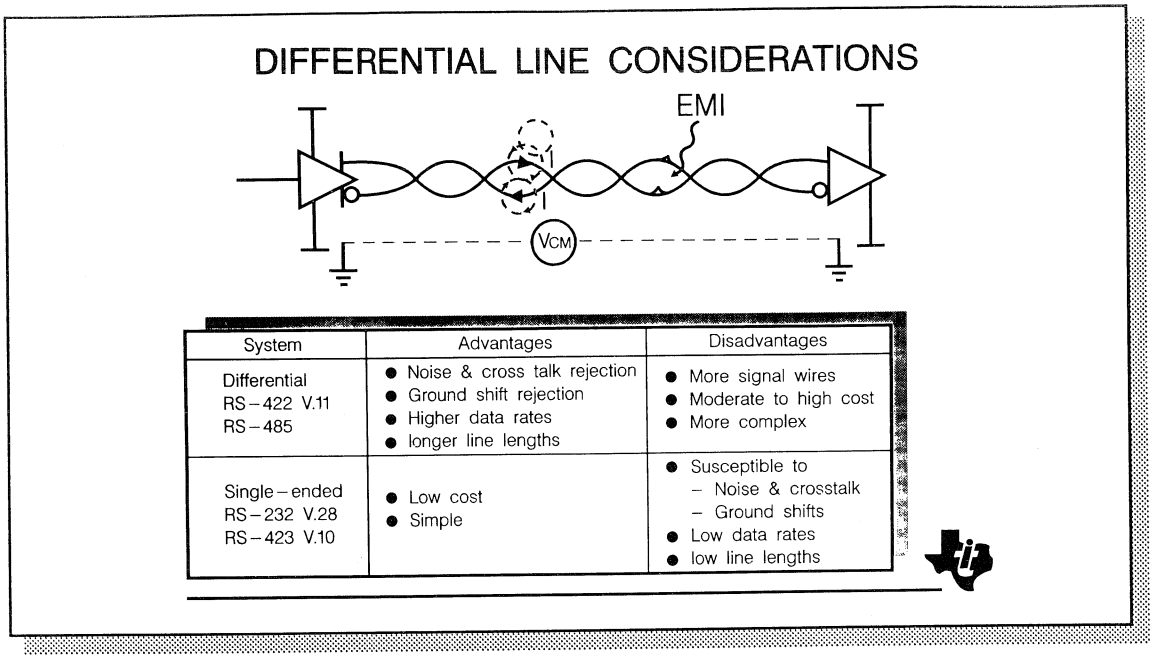


Figure 04 - Differential Line Considerations

A differential communication system requires the use of two 'signal carrying' wires between driver and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the *difference* in voltage between the two wires. The absolute value of the d.c common mode voltage of the two wires is not important. In practice, drivers and receivers have a finite common mode voltage range within which they can operate.

The use of a differential communications interface allows data transmission at high rates and over long distances to be accomplished. This is because effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode voltage level of the signals. The differential output voltage to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost, but provides superior performance when data is to be transmitted at high rates over a long distance.

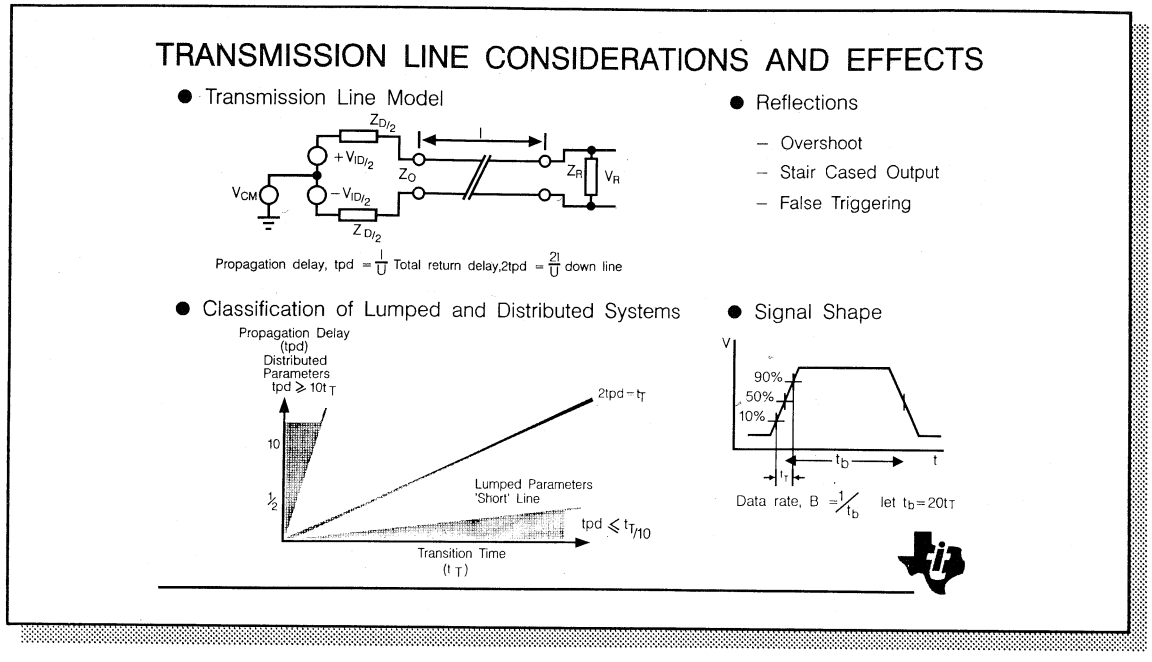


Figure 05 - Transmission Line Considerations and Effects

Before design of a digital data link can take place application constraints and an understanding of the signal's characteristics must be understood. More specifically, a method of identifying the class of data link, and any special design techniques required must be made.

A digital data link can be classed in two modes;

i) A transmission line (distributed parameter model)
ii) Short wire (lumped parameter model).

A distributed parameter model considers the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections making up the line. The result is that a transmission line is said

Notes

to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a wavefront at any point as it travels along the line.

The transmission line will always consist of two conductors, with the current flowing in opposite directions in each of the conductors. In the single ended case, one of these conductors is the ground wire.

The speed that a pulse travels at along a transmission line approaches that of the speed of light. The type of cable used will provide the limit to the actual speed.

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings. If the signal starts to change at the driver's output at one end of the line, the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the driver terminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system. A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the rise time , t_T, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from driver to receiver and back to driver, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, t_{pd}, to occur during the transition edge time.

When the cable is operating like a transmission line, extra loads in the form of drivers and receivers can be added, providing that they do not cause too great a shunting effect on the line. These extra loads, if evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. The extra devices will decrease the line impedance and reduce the speed of the signal along the line.

In the case of the lumped parameter model, the line tends to represent a pure fixed load to the driver device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of a driver device that can supply a finite amount of current to the line.

Line Termination

It is generally good design practice to terminate the ends of lines which are classified as transmission lines. Here the golden rule is to match the impedance from the source of the driver to the characteristic impedance of the cable, and from the cable to the characteristic impedance of the receiver. If there is an impedance discontinuity at any junction, then the signal will be reflected from the mismatch. This will lead to signal distortion which in turn leads to either a falsely triggered receiver or excessive propagation delay. Calculation of a suitable value for this termination value will be dealt with later in this section whilst a more detailed discussion can be found in the glossary section.

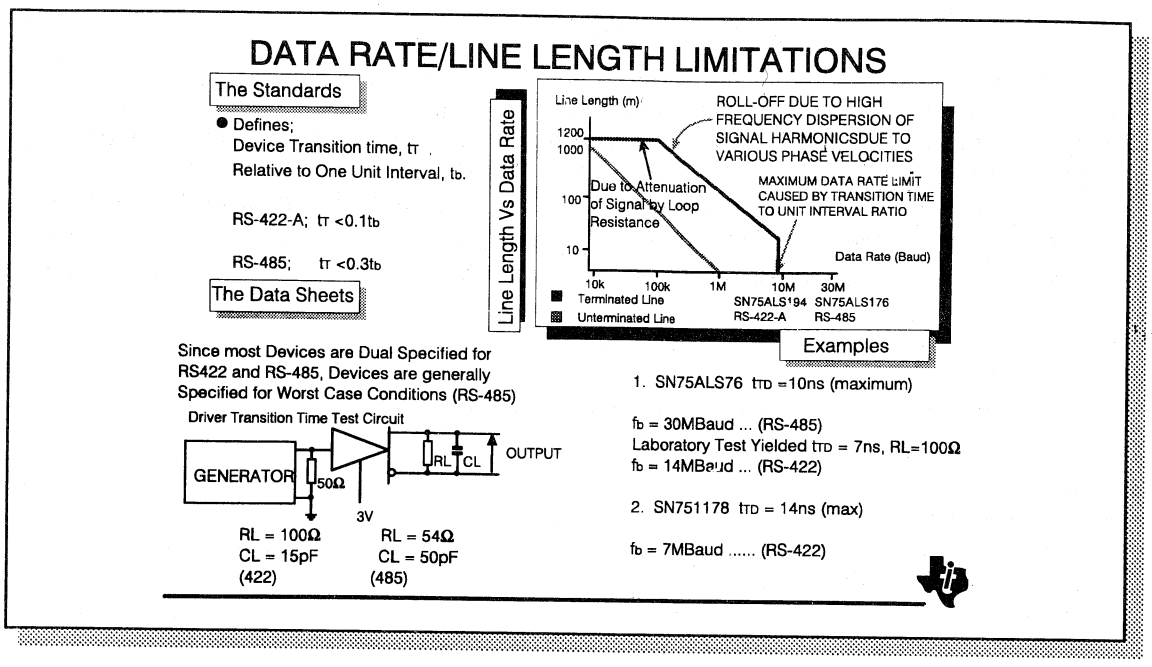


Figure 06 - Line Length and Data Rate Limitation

Most application areas will demand some kind of compromise between the line length used and the data rate required, particularly if distortion in its many guises is to be avoided. A first, all important, step in understanding what compromises are necessary is to recognise the various forms of distortion and why they occur.

No transmission line is perfect, even by sending current down the line some voltage drop will occur due to the resistive nature of the line, this in its most simplistic form is distortion. This is compounded when longer line lengths are used where the attenuation from source to destination can cause quite severe distortion. This places a limit on the line length even at low data rates as shown in the top right hand corner of the figure.

A typical cable of 24 SWG can have a series resistance of 80 Ω per km, and so the line length will be limited to the order of 1200m (series resistance equals the line's characteristic impedance).

Notes

The Standards

Another limitation of system performance are the speed limitations of the line driving elements themselves. No device, no matter what technology used, will have zero propagation delays and transition times. The trick is to ensure that any delay introduced by these devices is insignificant in comparison to the line propagation delay. To ensure the device does not introduce distortion, ie to maintain signal shape, it is good design practice to set a ratio between the unit interval, t_b, and the transition rise time, t_T .This limitation is often specified in the standard being used. For RS-422-A the ratio of t_T to t_b is 1: 10, and for RS-485 1:3.3.

The Data Sheets

Many devices within Texas Instruments' range are specified for both RS-422 and RS-485 operation. The differing specifications of relating t_T to t_b between the standards makes an understanding of data rate capability for RS-422 operation difficult to ascertain, since these devices are tested to the worst case conditions of the RS-485 specification. That is, the driver output is driven into a resistive load of 54Ω in parallel with a capacitive load of 50pF.

An example of such a device is the SN75ALS176 which can be used for both RS-422 or RS-485.

Examples

1. **SN75ALS176B** has a differential-output transition time t_T of 10ns(Max).

Therefore; $t_b = 3.33 \times 10x10^{-9} = 33.3ns$ giving a minimum theoretical frequency of **30Mbaud.**

As the data sheet specifies a minimum t_T = 5ns the maximum theoretical data rate could be as high as 60 Mbaud.

Using the RS-422 data rate test for this devices does not give a clear picture as the standard requires a lighter load to be applied. However, laboratory test using the RS-422 load gives a t_T for the ALS176 of 7ns (RS-485 load = 14ns) indicating a RS-422 data rate of 14Mbaud.

2. **SN75ALS194** has a differential-output transition time t_T = 14ns(Max). Since this device is specified solely for RS-422 we can clearly calculate the minimum theoretical data rate.

Therefore; $t_b = 10 \times 14x10^{-9} = 10 \times 14x10^{-9}$ giving a minimum theoretical frequency of **7Mbaud.**

Again a more aggressive data rate could be achieved if the typical specified value for t_T = 8ns was used. Giving a typical frequency of 12.5 Mbaud.

Other Effects

Other effects acting upon the transmission line are due to phase distortion introduced on the driver's transition edges. The high speed edges, necessary for high speed systems, have a high frequency harmonic content. The inductive and capacitive (and resistive) nature of the line introduces delay and distortion into these harmonics. This in turn reduces the clarity of the signal being sent down the line, thus increasing the probability of error.

This effect is normally measured using eye patterns which measure the jitter and distortion in the signal being sent down the line. It is this effect that causes the predominant reduction in data rate as the line length increases. Another limitation can be caused by incorrect termination of the line, causing reflections. These reflections can cause errors due to loss of timing information.

In conclusion, distortion and thus data integrity is a function of signal rise time and line attenuation. Signal rise time and attenuation are often quoted in manufactures data, and can be used to determine the line distortion.

A Discussion of Skew

When driving the line at high speeds the effects of the driver and receiver on the system become more apparent. The size of the delays relative to the unit interval will increase, meaning that asymmetries in the edges can cause extra distortion on the output to the line.

Using differential line systems, the delays through the driver and receiver have different meanings. This is because the driver is really a single ended input to differential output converter, while the receiver is a differential input to single ended converter.

When discussing propagation delays through the driver, two possibilities arise; the propagation delay from the input to one output and the other output (single ended) and also the propagation delay from the input to the differential output (differential).

The single ended propagation delay is normally measured between the input going through 1.5V and the output going through 1.5V, while the differential propagation delay is measured from the input going through 1.5V and the differential output going through its mid-voltage, (in a balanced line 0V across the line).

Notes

These propagation delays effectively displace the signal on the line in time, but do not ideally distort it, however, differences in the delays from output A going high and output B going low to output A going low and output B going high does cause distortion. The differences between these are termed as the skew in the output. For a single ended measurement it is termed the ***Propagation Skew***, while for the differential measurement it is termed ***Differential Skew***.

The main effects of propagation skew are that the differential transition edges can be stretched out and that they can become flat around the threshold region of the receiver, i.e. at the common mode voltage of the line. This gives the system a lower noise immunity and can increase the radiated RFI and sensitivity.

The main effect of the differential skew is the asymmetry caused by different differential propagation delays causing one state to be longer than the other state.

The propagation skew is specified on the older differential line drivers, while differential skew is specified on the more modern devices such as Texas Instuments' SN75ALS176.

The receivers are tested on the propagation skew. With one input tied at a reference voltage and the other toggled, giving a single ended propagation delay. The skew in this delay will also cause extra distortion to the signal, especially its timing information, as the periods can be further distorted.

Practical Considerations

Having reviewed some of the key issues involved in implementing a high speed differential data link, practical ways in which to overcome some of the problems encountered are now discussed.

The first areas of concern are how to make connections to the line, how and where the line should be terminated and into what value?.

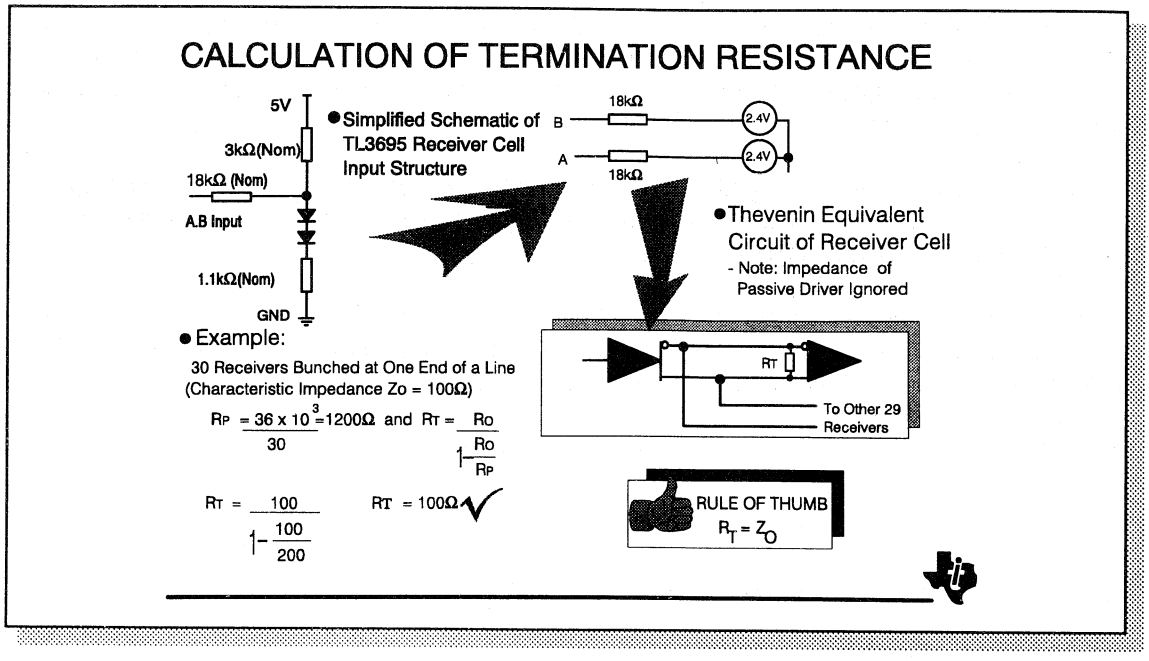


Figure 07 - Calculation of Termination Resistance

For better performance, the transmission line needs to be terminated by a resistor of a value close to its characteristic impedance. One question that immediately arises is the value of terminating resistance required if the line is loaded by other receivers. More specifically, does the receiver's input impedance have any effect?, especially when many receivers may grouped together at the far end of the line. The following text sets out to prove that for the majority of applications the loading effect of receiver stations can be ignored and as a rule of thumb (working approximation) the value of R_T should equal the characteristic impedance of the line.

In fact, the characteristic impedance varies very little with respect to the physical dimension of the cable. For example a wire over-ground transmission line with a wire diameter equal to the diameter of an electron and a height above the ground plane of 500,000Tm (50 light years) has a characteristic impedance, Z_O, of 3000Ω.

Notes

Each input of the receivers has a nominal input impedance of 18kΩ feeding into a diode-transistor- resistor biasing network, this is equivalent to an 18kΩ input resistor tied to a common mode voltage source of 2.4V. -It is this configuration which provides the large common range of the receiver required for RS-485 systems!.

Due to the fact that the each input is biassed to 2.4V, the normal common-mode voltage of balanced RS-485 systems, the 18kΩ resistors on the inputs can be taken as being in series across the input of each individual receiver.

If thirty such receivers are placed close together at the end of the line, they will tend to react as thirty 36kΩ resistors in parallel with the termination resistor. This overall effective resistance will need to be close to the characteristic impedance of the line.

The effective parallel receiver resistance, R_P, will therefore be equivalent to;

$$R_p = 36 \times 10^3 / 30 = 1200\Omega .$$

While the termination resistor, R_T, used will be equal to;

$$R_T = R_O / [1 - R_O/R_P] .$$

Thus for a line with a characteristic impedance of 100Ω, the termination resistor R_T should be:

$$R_T = 100/[1 - 100/1200] = 110\Omega$$

Since this calculated value is within 10% of the line characteristic impedance the value chosen for the line termination resistor, R_T, will normally be equal to the characteristic impedance, Z_O.

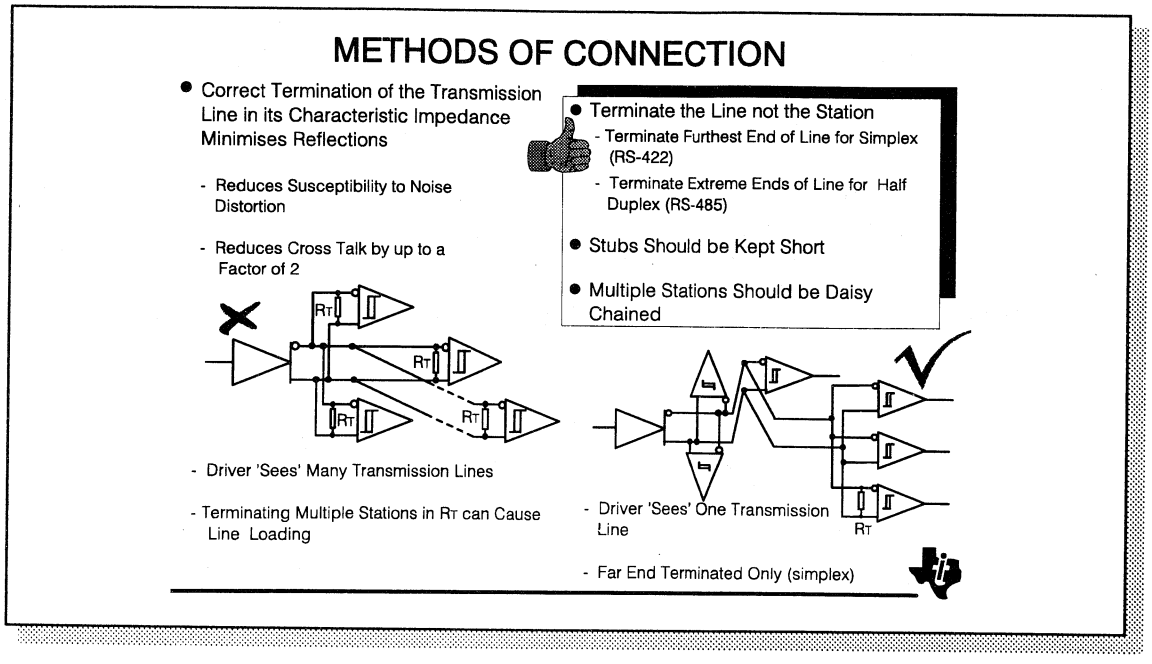


Figure 08 - Methods of Connection

Methods of Connection

The way in which stations are connected to the line needs careful consideration. Furthermore methods of line termination and device positioning must be considered. There are two basic methods of connection;

i) The star connection
ii) The daisy chain connection

Considering the star connection, the transition edge from the driver will be loaded by a group of separate transmission lines, rather than one. Each transmission line boundary will cause a change in impedance resulting in reflections.

Notes

Another situation to avoid is the termination of multiple stations, since this could excessively load the driver. Termination at the extreme ends for RS-485 (half duplex) and far end only for RS-422 is recommended. Normally stubs (taps of the main line) should be kept as short as possible so not to appear as transmission lines themselves.

The recommended method is to use the daisy chain, a configuration where the transmission line continues from one receiver to the next and only the last receiver on the chain is terminated. This means that the transmission line and hence the driver will see one continuous transmission line with only one termination resistor. Each tap-off will in effect be a stub, but in this case they will not be all grouped together and will be kept very short to reduce their effect.

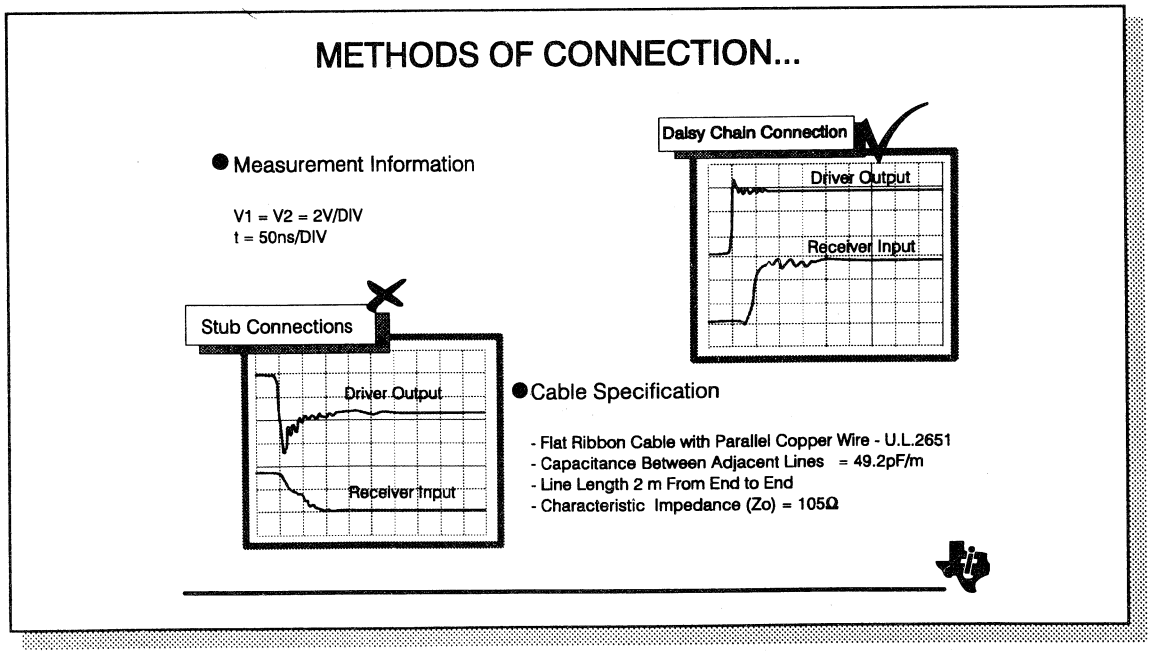


Figure 09 - Methods Of Connection...

Comparing the Quality

The figure shown, further confirms the need tor keep stub lengths short and the use of correct termination techniques by comparing the effect on signal quality for the daisy chain and star method of connection.

In both instances exactly the same application scenario was used as was the same cable specification. The cable used was a flat ribbon cable with parallel copper wire conforming to U.L. specification 2651. Connections were made as shown in the previous figure and the total cable length from source to destination was 2 m.

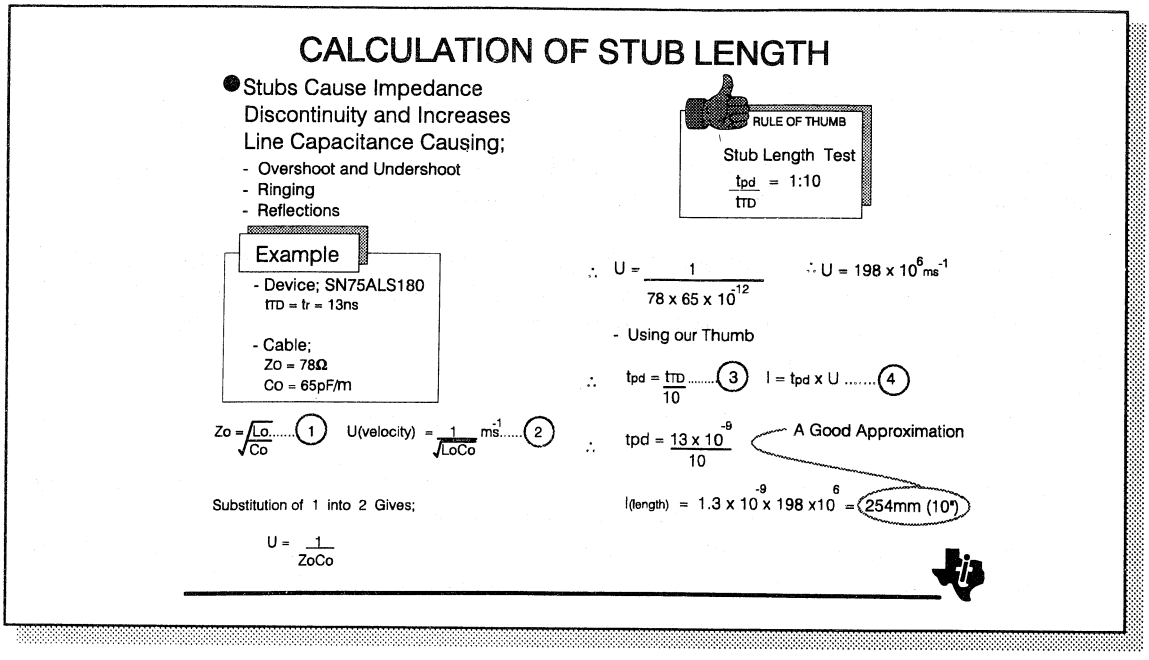


Figure 10 - Calculation of Stub Length

In the earlier section a rule of thumb was developed which stated that if signal distortion is to be avoided, all connections to the main line must be kept as short as possible. Distortion in this context could be both amplitude and phase distortion - leading to reflections amongst other undesirable factors.

These connections are usually termed stubs. A stub is a connection to the transmission line from either a driver or a receiver . However, even when short in comparison to the length of the main transmission line it too could exhibit transmission line effects. Any connection to the line will cause an impedance discontinuity, leading to reflection at the stub/transmission line boundary.

To minimise these effects the stub should be kept as short as possible, so that the stub is seen as a lumped (non transmission line) rather than a distributed (transmission line) load to the line.

Notes

How Short is Short ?

It has been described earlier that a pair of cables will act as a transmission line if the round trip propagation delay, t_{pd} ,is more than 5 times the transition times of the driver, t_T. The converse is true if the line is not to operate as a transmission line but as a lumped parameter model. This forms the basis of the stub length calculation given below.

The figure shows a calculation for determining the maximum length of the stub. The rule of thumb that the transition time of the pulse sent down the line should take ten times the time taken for the pulse to propagate to the end of the stub. Rsulting in any reflections being incorporated into the transition edge.

From this basis, the length of a stub can be calculated using the cable and driver parameters.

The pulse speed down the line, U, equals the reciprocal of the product of the line impedance and line capacitance, both of which are normally specified for the cables used.
The propagation delay down the stub should be at the most one tenth of the transition time of the pulse. These facts can be brought together to give the length of the stub, l_S , as;

$$l_S = t_{TD}/ (10)$$

Using the SN75ALS180 and its transition time of 13ns, a cable with a characteristic impedance of 78Ω and line capacitance of 65pF, gives a maximum stub length of 254 mm or ten inches.

The main effect in this case will be a slight increase in the capacitance loading of the line.

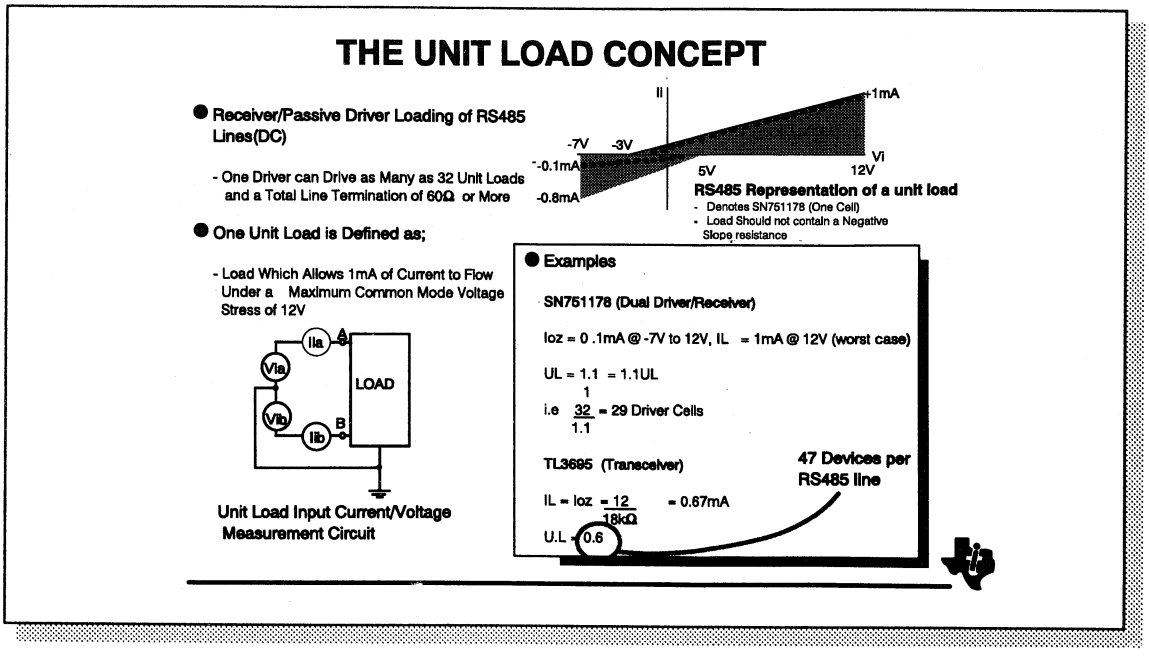


Figure 11 - The Unit Load Concept

Line Loading Considerations

One final consideration needed to implement a digital data link is the number of driver/ receiver elements that can be connected to the line. This is now discussed;

The Unit Load Concept (RS-485)

The maximum number of drivers and receivers that can be placed on a single communication bus depends upon their loading characteristics relative to the definition of a unit load (U.L). RS-485 recommends a maximum of 32 unit loads per line.

One U.L (at worst case) is defined as a load that allows 1 mA of current under a maximum common-mode voltage stress of 12 V . The loads may consist of drivers and/or receivers but

Notes

does not include the termination resistors, which may present additional loads as low as 60Ω total.

The first example shows a unit load calculation for the dual SN751178 driver/receiver which offers a unit load value of 1.1 U.L - meaning 29 such devices could be connected on one line. In the second example the TL3695 transceiver is used. Since this device is internally connected as a transceiver, ie driver output and receiver input connected to the same bus, it is difficult to obtain separate driver leakage and receiver input currents. For this calculation reference is made to the receiver input resistance, 18kΩ, giving a transceiver current of 0.6mA. This can be taken to represent 0.6 U.L. which will allow upto 47 devices to be connected to the line.

Obviously it may be possible to connect more devices than the RS-485 recommendation, but this is at the designers risk.

The graph in the top right corner of the figure is used to define the boundaries of the unit load, and works by superimposing the voltage and current characteristics of the load upon a reference trace. A line from - 3 V is drawn at a tangent to intercept receiver input current at the 12 V point. Similarly, a line is drawn from -7 to intercept the driver leakage current at the 5 V point. The currents indicated at - 7 V and -12 V are then compared to the currents specified by the standard. The larger of the two voltage to current ratios forms the unit load value.

The electrical characteristics should not show any negative resistance otherwise instability and spurious oscillations could occur.

Total Load Characteristic Limits (RS-422)

In RS-422 the d.c load characteristics is specified much more simply;

The total load including multiple receivers, fail safe circuitry, and cable termination shall have a resistance greater than 90Ω between its input points (A and B), ie across the line, or when the cable is left un-terminated the resistance shall be greater than 400Ω, and shall not require a differential input voltage of more than 200mV for all receivers to assume the intended binary state.

With a basic understanding of transmission line practicalities, a brief discussion of the range of Texas Instruments products available and their application can begin.

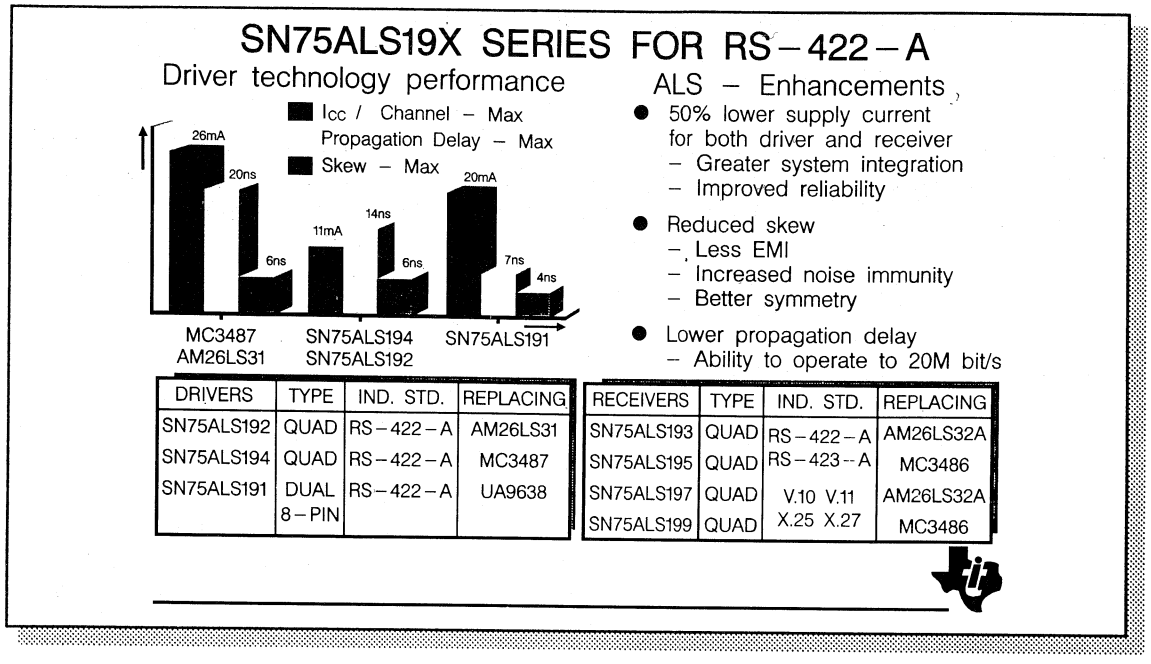


Figure 12 - SN75ALS19x Series For RS-422

The well proven SN75ALS19x series of drivers and receivers for RS-422-A represents some of the best speed versus power consumption alternatives in the industry today for reliable balanced line transmission over short as well as long distances. The series has found wide use in telecommunication as well as in computer applications.

ALS Technology Advantages

All ALS products employ Advanced Low-Power Schottky or Impact™ processes. These have been derived from the digital processes and trimmed for linear applications requiring wide common mode voltage operation, tough protection and accurate receiver input threshold

Notes

voltages. ALS technology provides combined improvements in die design, tooling production, and wafer fabrication, which in turn, provide lower power consumption and permit much higher data throughput than other designs - in short; speed without the usual power penalties. Standby current is typically reduced by 50% although switching speed has gone up by more than 30% compared with previous LS (Low Power Schottky) parts.

50% Lower Supply Current

The significant reduction in power consumption allows for a higher board packaging density and hence greater system integration without increasing temperature due to power dissipation. In addition, a lower operational temperature improves system reliability.

Lower power consumption also permits devices to operate in an extended temperature range (-55°C to +125°C) with fewer constraints.

30% Improvement in Data Throughput

Lower propagation delays and reduced skew, combined with lower standby power consumption, allows these devices to operate in excess of 20Mbaud. For example; a SN75ALS192 quad driver is capable of transmitting data at 20Mbaud (50% duty cycle) while only dissipating the same power as an AM26LS31A in standby mode. The maximum achievable data rate is usually determined by maximum power dissipation at the maximum operating temperature. Reference should be made to the datasheet's Dissipation Rating Table.

Reduced Skew

Skew for a data transmission driver or receiver is related to the difference in propagation delays from input to output. With different high and low going propagation delays for a device, asymmetry in its output signal occurs, which ultimately reduces the maximum data rate.

When switching the output of the differential driver from one state to the other state, differences in propagation delays from the input to the inverting and non-inverting outputs can cause the differential output voltage to flatten out as it passes through the receiver's threshold region. Clearly, this makes the received signal more vulnerable to noise.

The SN75ALS19x series has been designed with minimum skew to improve symmetry, increase noise immunity and radiate less EMI (Electromagnetic Interference) caused by non-common mode currents in the transmission cable. The high-speed dual driver, SN75ALS191 in an 8-pin package features a typical differential skew of 1.5ns (4ns maximum).

Products

A wide range of SN75ALS19x products are available as improved pin for pin replacements for industry standard devices.

The main difference between the quadruple drivers, SN75ALS192 and SN75ALS194, is related to their enabling configuration. SN75ALS192 has a common pin enabling all four drivers, whereas independent enabling schemes are possible for each pair of drivers in the SN75ALS194. Similarly, different enabling schemes distinguishes the quadruple receivers, SN75ALS193 and ALS195. The SN75ALS192 and SN75ALS193 form complementary devices as do the SN75ALS194 and SN75ALS195 devices. Using complementary drivers and receivers together should provide optimum performance.

The quadruple receivers, SN75ALS197 and ALS199 have relaxed input sensitivity specifications of ±300mV, compared to ±200mV for SN75ALS193 and ALS195. However, they are available in low cost D (surface mount) or N (DIL) packages and meets CCITT Recommendations V.10, V.11, X.26 and X.27.

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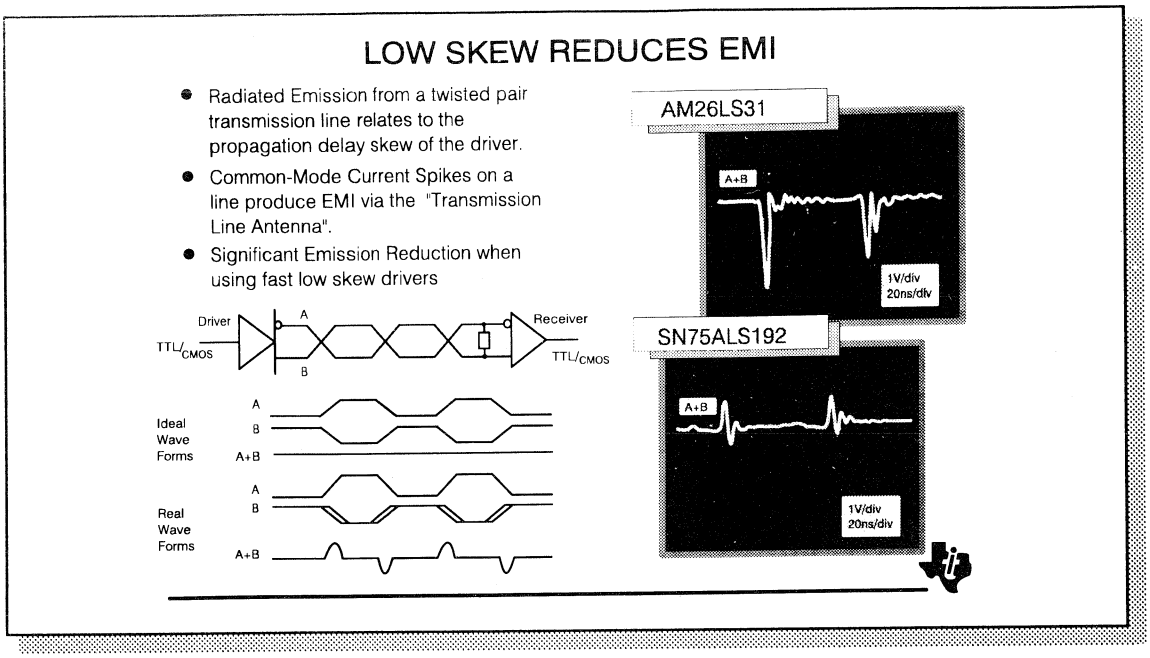

Figure 13 - Low Skew Reduces EMI

EMI Related to Differential Transmission Lines

Radiated emissions from electronic systems is having more attention paid to it, as mutual disturbances between electronic equipment increase and the subsequent need for EMC regulations becomes more apparant. This is compounded by the increased use of high clock rates and high currents which generate high frequency EMI. Applications placed on printed circuit boards are normally enclosed in a confined space making the problem easier to solve, but when transmitting data signals to the outside world through cables, increasing the total radiated emission by the system is difficult to avoid.

In large computer systems, Inter-unit cables within the system have been found to be responsible for much of the radiated emission. Further studies have revealed that the noise itself is a function of common mode current spikes, brought about by the skew between the outputs of clocked differential drivers. Significant improvements in system-wide emissions were seen in practice after replacing high skew driver devices with others those which had less skew.

The effect seen is not only related to large computer systems but is scaleable to all systems using differential transmission lines. Differential drivers and receiver are designed to operate under conditions with high common mode signals. Low frequency common mode signals usually cause no problems, but high frequency common mode spikes cause EMI and in systems with inter-unit cabling an antenna is readily available increasing the radiated emission. Clearly, twisted pair cables used to interconnect boards within the same cabinet, or

to establish data transmission between various equipment, using for example the popular standards RS-422-A or RS-485, are likely to radiate EMI if the driver's complementary outputs are not exactly symmetrical. This is true for the single differential line in an industrial system as well as for the many parallel differential lines used in a SCSI interface cable.

Low Skew Devices Reduce EMI

Ideally, a differential driver should not generate common mode signals due to the nature of the differential output and the twisted cable cancelling the common-mode currents but in practice, small differences between the complementary outputs occur which produce fast common mode pulses on the line.

The skew specification, specified as the propagation delay difference from the input of the differential driver to the driver's respective inverting and non-inverting outputs is a good measure for how much or how little radiation that can be expected from high frequency common mode signals during switching. However, a low skew specification on its own does not guarantee negligible common mode signals as the signals can still be unsymmetrical due to different rising and falling waveforms. In such cases Significant current spikes can be measured on the line.

Use Fast Devices Even in Low Data Rate System

Even in systems where low data rates are used, EMI can still cause problems with EMC regulations. These problems are best solved by employing high speed devices usually having a significant lower skew than slower drivers.

Consequently, previous low power schottky (LS) designs like, AM26LS31 or SN75176 will in general radiate more emissions than newer Advanced Low Power designs like SN75ALS192 and SN75ALS176 or even the new BiCMOS designs like AM26C31 and SN75LBC176. A measurement was made to demonstrate this effect comparing AM26LS31 with SN75ALS192. Evidently, the negligible common mode signals resulting from switching the SN75ALS192 are significantly smaller than the clearly visible common mode current spikes produced by the AM26LS31.

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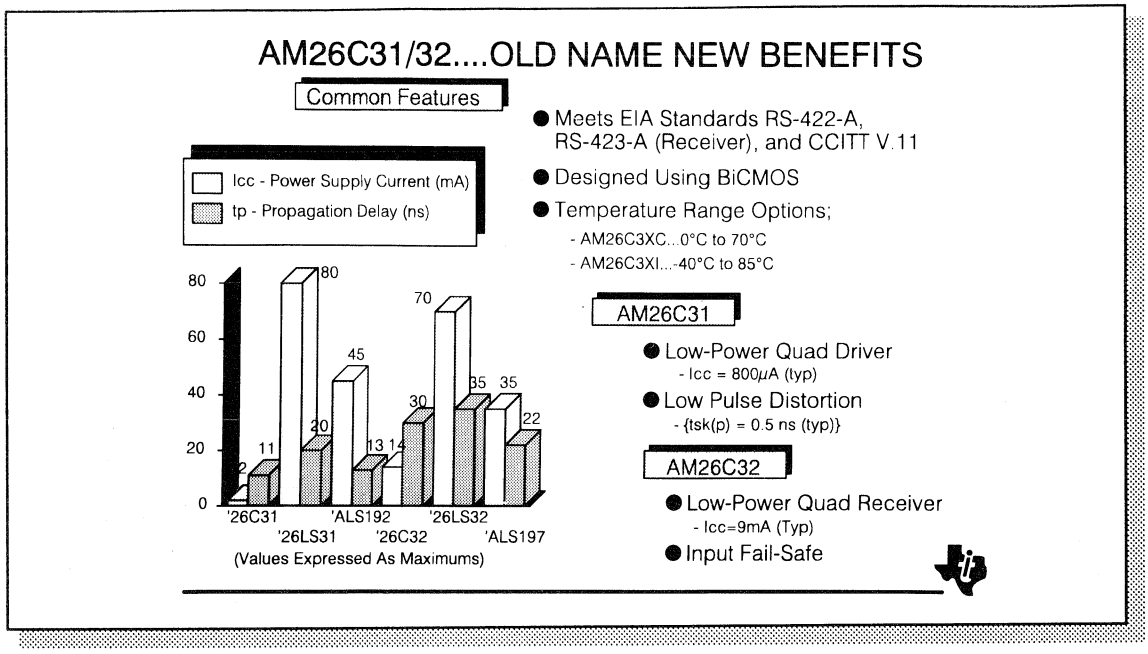


Figure 14 - AM26C31/32....Old Name New Benefits

Improvements in Power Consumption and Speed

Industry has long been aware of the advantages gained from using the quadruple driver AM26LS31 and the accompanying quadruple receiver AM26LS32 for RS-422 type applications . However the old low power schottkey (LS) process is no longer capable of keeping pace with todays demands for high speed and low power. The AM26C31 are AM26C32 are modern upgrades, fabricated using a low power BiCMOS process.

These devices find applications where high speed and low skew are crucial, for example in disk drive and Telecommunication applications. One particular application which would benefit from the low power consumption will be the Central Office Exchange, where due to the shear number of devices used, power consumption becomes a critical issue - especially when the rest of the system is implemented in low power CMOS.

The figure shows some key benefits of these new designs and compares the power consumption and propagation delay against industry standard devices. It can easily be seen that the BiCMOS devices not only exhibit a dramatic reduction in power consumption, from 80 mA to 2 mA, but there is also an improvement in ac performance. The AM26C31 driver has a lower propagation delay than any of the devices shown in the graph.

Description

Both the AM26C31 and AM26C32 have been manufactured using a BiCMOS technology which is a combination of bipolar and CMOS transistors. This process provides the high

voltage/current drive of bipolar with the low quiescent power consumption of CMOS. The graphs in the figure show that the power consumption of the AM26C32 receiver is reduced to approximately one-fith of the standard LS part.

The AM26C31 is a quadruple complementary-output line driver designed to satisfy the requirements of EIA RS-422-A and CCITT recommendation V.11. The three-state outputs have a high-current drive capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high impedance state in the power-off condition. The enable function is common to all four drivers and offers the choice of active-high or active-low enable input.

The AM26C32 is a quadruple line receiver for balanced and unbalanced digital data transmission. Conformance to the EIA standards RS-422-A and RS-423-A and CCITT recommendation V.11 is guaranteed. The enable function is common to all receivers and offers a choice of either active-high or active-low inputs. Three-state outputs permit connection to a digital data bus. Fail safe circuitry design on the receiver input side ensures that the outputs will remain in a high state even if the inputs are left open. This reduces the chances of incorrect data interpretation.

Notes

Protecting Against Data Corruption

One noted feature offered by the AM26C32 receiver was an built-in fail safe feature. This feature is also a requirement in many RS-485 applications, however its usefulness needs to be considered and understood at an application level.

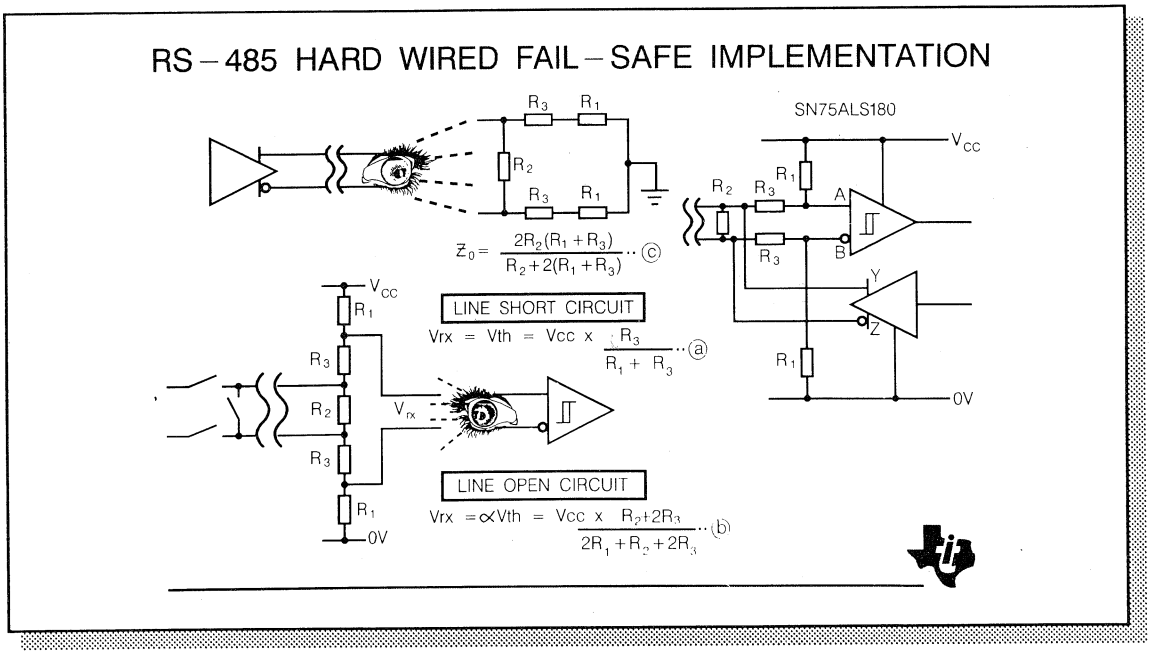


Figure 15 - RS-485 Hard Wired Fail safe

The need For Fail safe Protection

In any party line interface system, with multiple driver/receivers, there will be long periods of time when the driving devices are in-active. This state known as line idle occurs when the drivers place their outputs into a high impedance state. During line idle, the voltage along the line is left floating, i.e. indeterminate - neither logic high or logic low. As a result the receiver could be falsely triggered into either a logic high or a low logic state, depending upon the presence of noise and the polarity of the floating lines. This is obviously undesirable as the circuitry following the receiver could interpret this as valid information. The receiver should be able to detect such a situation and place its outputs into a known, and pre-determined state. The name given to methods which ensure this condition is called **fail safe**. An Additional feature which a fail safe should provide is to protect the receiver from shorted line conditions which can again cause erroneous processing of data and/or receiver damage.

There are several ways implement a fail safe, including a hard-wired fail safe using line bias resistors or protocols. Protocols, although complicated to implement, are the preferred method and are discussed in more detail following this section. However since most system designers, hardware designers in this case, prefer to implement such functions in hardware a hard-wired fail safe is often implemented.

A hard wired fail safe should provide a defined voltage across the receiver's input whether or not the line is shorted to either supply rail or is left open circuited. The fail safe should also be incorporated into the line termination network when at the extremes of the line.

Internal Fail safe

Manufacturers have gone part way to facilitating fail safe design by including some form of open line fail safe circuitry within the integrated circuits. Unfortunately, due to power consumption constraints, the extra circuitry has proved little use. The extra circuitry is quite often just a large pull-up resistor on the non-inverting receiver input, and a large pull-down resistor on the inverting input of the receiver. These resistors are normally in the range of 100kΩ, and so when used in conjunction with line termination resistors to form a potential divider, only a few milli volts are generated. As a result this voltage (receiver threshold voltage) is insufficient to switch the receiver. In effect, to use these internal resistors no line termination resistors can be used, which reduces the allowed reliable data rate enormously.

External Fail safe-Open Line Conditions

A more reliable way of offering open line fail safe is to use external pull-up and pull-down resistors. There two basic ways of doing this; one way is to polarise the line with the pull-up/pull-down resistors and use these resistors to match the line impedance. Another way is to use larger polarising resistors while using an extra resistor to terminate the line. The first idea has one advantage in that it provides a low impedance path to an a.c. ground, so that any currents induced on to the line have a low impedance path to ground. However a problem is encountered with this method because the driver output now has to drive very much lower impedances. If the driver output current capability is poor the device could easily go into output short circuit current limit. The second way, although requiring an extra resistor will not load the driver's output to such an excess.

Notes

Placing external pull-up and pull-down resistors R_1 on the non-inverting and inverting inputs of the receiver will produce open circuit fail safe. Terminating the transmission line with its characteristic impedance,Z_O , produces a potential divider between $2R_1$ and Z_O. The voltage formed across the line, V_{OC}, equals

$$V_{OC} = V_{CC} * \frac{Z_O}{2R_1 + Z_O}$$

Devices meeting the RS-485 receiver threshold voltage specifications require V_{OC} to be greater than 200mV . From this the relationship of R_1 to Z_O can be derived:-

$$R_1 = Z_O * \frac{1}{2} * \frac{V_{CC} - V_{OC}}{V_{OC}}$$

With V_{CC} = 5V, V_{OC} = 200mV and Z_O = 100Ω, yields R_1 = 1.2kΩ.
Biassing the receiver in this way will only provide open line fail safe, it will not provide shorted line fail safe. However, when using transceivers it is not possible to provide shorted line fail safe configurations, this ia result of the driver and receiver sharing the same i.c. pins. Hence for devices like the SN75ALS176 this open line configuration the optimum fail safe available.

External Fail safe-Shorted Line Conditions

To implement protection from the shorted line condition, further resistors are required. When the line is shorted the transmission line's impedance goes to zero and the termination resistors will also be shorted. Putting extra resistors in series with the input to the receiver can provide shorted line fail safe protection.

The extra resistors, R_3 in the figure, can only be added when using devices with separate driver outputs and receiver inputs. So internally wired transceivers cannot be used to offer shorted line fail safe. If this form of protection is required then a device such as the SN75ALS180, with its separate driver outputs and receiver inputs, should be used. If a transceiver type device was used then the extra resistors R_3 would cause extra attenuation of the output signal. The ALS180 will have its driver outputs fed directly to the line, bypassing resistors R_3.

Calculating the Resistor Values

If the line became shorted then R_2 would be removed leaving a voltage across the receiver inputs of:-

$$V_{rx} = V_{CC} \times R_3/(R_1 + R_3) \qquad \textbf{(a).}$$

For RS-485 and 422A applications the standard specifies V_{rx} to be greater than 200mV. So $V_{rx} = V_{th}$ = 200mV. Using this figure, along with the minimum permissible supply voltage for the devices gives a relationship between R_1 and R_3.

When the line goes into a high impedance state the receiver will see the two R_3 in series with R_2 plus the two R_1's pulling up and down on either input. The receiver input voltage will now be:

$$V_{rx} = V_{cc} \times (R_2 + 2R_3)/(2R_1 + R_2 + 2R_3) \quad \textbf{(b).}$$

Relating this new V_{rx} to the minimum specified in the standard, V_{th}, gives:

$$R_1 = \tfrac{1}{2}R_2 \times \left[\{(V_{cc} - \alpha V_{th})(V_{cc} - V_{th})\}/\{(\alpha - 1)\, V_{th}\, V_{cc}\}\right]$$

$$R_3 = R_2 \times (V_{cc} - V_{th})/V_{th}$$

The transmission line will see an effective line termination resistance of R_2 in parallel with twice the sum of R_1 and R_3. This should match the transmission line's characteristic impedance, Z_o, therefore

$$Z_o = 2R_2 \times \frac{R_1 + R_3}{2R_1 + R_2 + 2R_3} \quad \textbf{(c)}$$

Combining equations **(a), (b)** and **(c)** yields the following equations for R_1, R_2 and R_3:-

$$R_1 = \tfrac{1}{2}Z_o \times \frac{(V_{cc} - V_{th})^2}{(\alpha - 1)\, V_{th}\, V_{cc}}$$

$$R_2 = Z_o \times \frac{V_{cc} - V_{th}}{V_{cc} - \alpha V_{th}}$$

$$R_3 = \tfrac{1}{2}Z_o \times \frac{V_{cc} - V_{th}}{\alpha - 1\ V_{th}}$$

Notes

In this application assuming the supply voltage is 4.5V and Vth = 200mV with an a value α of 1.5 and driving a line with characteristic impedance of 120Ω yields the following values:-

R_1 = 2.2kΩ
R_2 = 120Ω
R_3 = 110Ω

The values of R_1, R_2, and R_3 only apply for receivers at the extreme of the line; if there are more receivers on the line then fail safe can be accomplished by multiplying the values of R_1 and R_3 by half of the number of receivers on the line. This is done by assuming the input stages of all the receivers are the same, all R_1 resistors are the same, and that all R_3 resistors are the same. Since all of R_1 and all of R_3 resistors will be in parallel, their overall resistance will be divided by half the number of receivers. If there is a large number of receivers on the line there is a danger of R_3 becoming too large and forming a large potential divider with the input resistance of the receiver, normally around 18kΩ.

Use of Protocols- Synchronous Serial Communication

The use of line terminations to effect a fail safe is not a recommended practice. The recommended practice is to use software protocols. Protocols come in many forms (two of which are explained below) and provide a set of rules which define the meaning and order in which data should be sent. In particular, they can be used to provide a fail safe feature and be used to avoid contention. Contention occurs when several drivers try to address the link at the same time. This can lead to high current sinking or souring leading to excessive thermal dissipation in the drivers. Fail safe is ensured by allowing the receiving station to respond to valid data only., This is achieved by sending a preamble before each data packet . The preamble consists of a pre-determined pattern of bits, which signals to the receiver that valid data is about to follow. Anything other than this preamble should be ignored by the receiver.

Party Line Protocol Formats

Party line applications use either half duplex or full duplex transmission. Half duplex's transmission mode is where two terminals (a driver and receiver) can communicate with each other bidirectionally over the same link, but they cannot transmit simultaneously. A party line transmission line format can be achieved using half duplex by multiplexing between a number of driver/receiver pairs. Full duplex communications involves the simultaneous, two way flow of data from driver/ receiver pairs.

A communication line uesd in a multiplexed operation such as the half duplex party line system reduces wiring costs when compared to the simplex operation (simplex one driver for one receiver). Only one line is needed to implement the communication system, though control of the multiplexing does require complex protocol or handshaking circuits.

A typical (simplified) protocol sequence would contain the following elements;

i) **Driver requests access to communication link (bus)**
ii) **Link controller responds to request and gives go ahead when bus is free**
iii) **Driver gains bus mastership and sends data which is preceded by a destination code**
iv) **Receiver sends an acknowledgement**
v) **Driver receives confirmation and releases the bus**

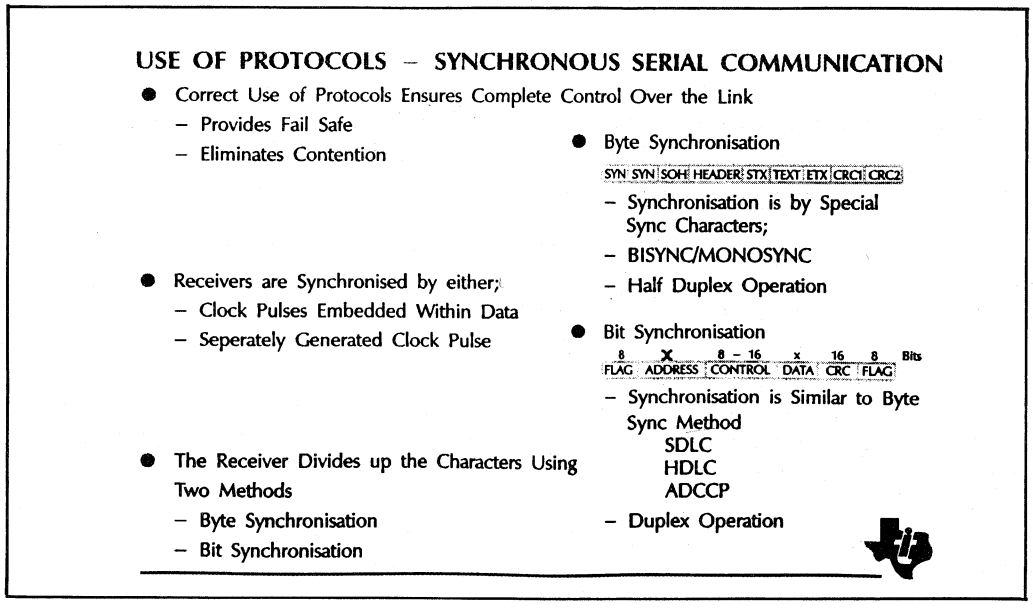


Figure 15a - Use of Protocols in Synchronous Serial Communications

Synchronization

Some form of synchronization is necessary for the receiver to determine the start and finish of the received bits. Two schemes, with many variations, are adopted; *Asynchronous* and *synchronous.*

Notes

Asynchronisation, or start-stop bit communication, uses a system where characters are sent one at a time, without necessarily having any fixed time relationship between each other. In such a case the driver sends start bits followed by the information field, followed by one or more stop bits. This informs the receiver that information data will follow the start bit and will end prior to the stop bit. The data is usually broken into small groups of 8-bits, one byte, which is preceeded with a start bit and concluded with a stop bit. This is one of the schemes employed by RS-232.

Synchronous transmission is used to transmit complete blocks of data at one time.In synchronous transmission the duration of each bit is the same. With all characters being the same length the receiver only has to identify the first character and then clock the others in at a predetermine rate.

Serial synchronous communication uses a similar scheme and either embeds the timing information in the data or provides a separate clock signal. However the bit stream still has to be divided up into the individual characters. There are two main methods of achieving character synchronization: *Byte synchronization and bit synchronization.*

Byte synchronization, one of the first synchronous methods to be introduced is best known by IBM's bisync and monosync . Synchronization is achieved by using special *SYNC* characters which are transmitted in between data packets. The receiver continually monitors this transmission and uses it to synchronize itself . After receiving one (monosync) or two (bisync) sync pulses the receiver is said two be in the synchronized mode and is ready to receive data. Synchronization is ensured by re-sending the sync bits every few hundred characters, for this reason data is grouped together in frames or packets which start with sync characters. Each frame is 8-bits long

The bisync protocol also defines a structure for a frame that includes control information and error checking capability. The figure shows the basic frame structure with the sync characters followed by the header field. *SOH* identifies the beginning of the header block. The *header* field is user defined and generally contains control specific information such as rest data link, message numbering priority ..etc. Start of text, STX, identifies the end of the header field and defines the beginning of the text field. The text or data field contains application specific information which must be sent to the application controller intact. ETX signals, end of text, and CRC1 and CRC2 are used as cyclic redundancy check bits. Notice that STX, ETX etc.. are the standard ASCII control codes. Bysync is essentially a half duplex system because each frame requires an acknowledge from the receiver before commencing with the next frame. Obviously sending acknowledging codes back and forth reduces the data rate, and to overcome this bit synchronization was developed.

SDLC (synchronous data link control), again made popular through IBM, was one of the first bit synchronization protocols available. The CCITT also adapted this standard for their high level data link (HDLC) protocol. Both are very similar to the CCITT X25 layer 2 packet switching local area networking standard. Initially bit sync looks very similar to byte sync , ie during data null periods sync pulses are sent over the link to synchronise the receiver and driver. However after the sync period the data may be grouped in any number of bits. Byte-sync systems are restricted to 8-bit packets. In SDLC and HDLC, messages are formatted into frames with each frame being divided into fields. The start flag is the sync data while the

address field contains the destination address to select the required receivers. The control field can be configured as either an information field or supervisory field. The information field, which is the usual format, contains status information on the number of frames sent or received. Data field follows and contains application specific code. The supervisory or management frame is used to acknowledge successful receipt of data. CRC is used for error checking and flag is the next sync signal.

Party Line Considerations

The following points should be considered for correct party line operation;

i) Each driver must have a three-state logic capability, two logic states and a high impedance mode. Also at any one instance it is likely that all drivers could be in the high impedance state, thus leaving the bus floating. A receiver should be able to detect this situation and protect against any spurious information - fail safe design.

ii) Receivers may oscillate if left unconnected, which might affect other used receivers in the same package. Therefore it is recommended that all unused receiver inputs should be tied to defined logic states.

Notes

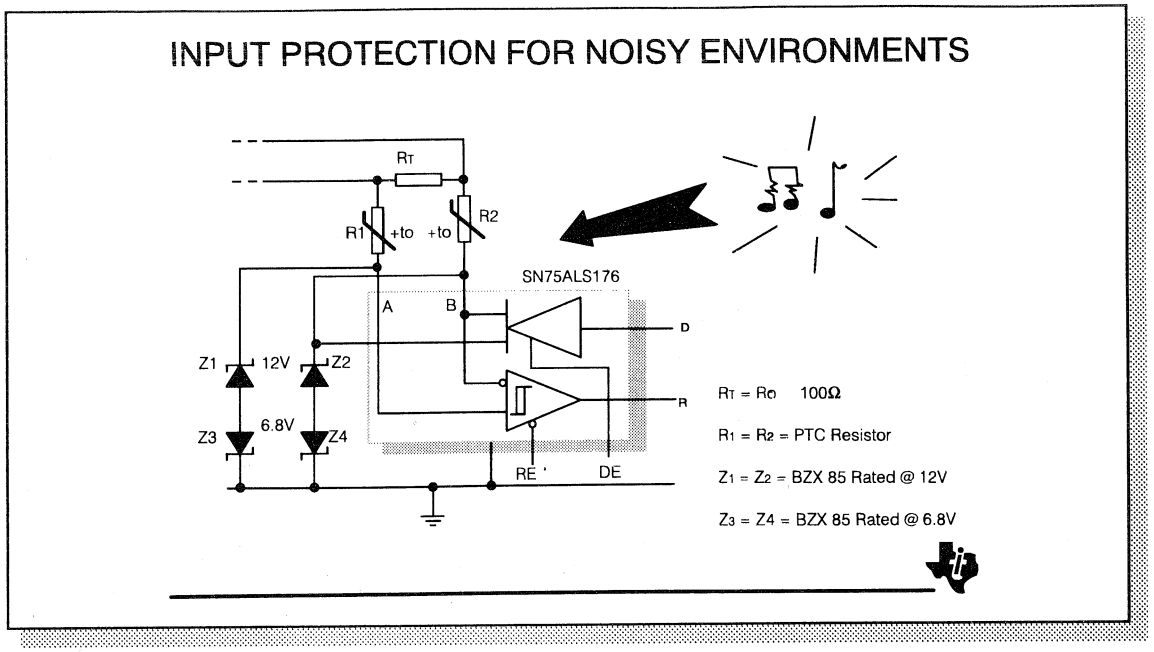


Figure 16 - Input Protection In Noisy Environments

In addition to fail safe protection, applications often require protection against excessive noise voltages.

Often when sending data over long distances or in electrically hostile environments, i.e. factory automation, the noise immunity afforded by the differential transmission scheme, and in particular the wide common mode voltage range of RS-485 is insufficient. This figure shows how external diodes offer transient spike protection for the SN75ALS176 RS-485 transceiver.

R_T is the usual termination resistance and is equivalent in value to the characteristic impedance of the line. Positive Temperature Coefficient resistors, R_1 and R_2, provide current limiters for the diode chain. Provided their ambient temperature resistance is kept below 50Ω they will be transparent during normal usage and will not alter the termination value or attenuate the driver output voltage.

Z_1 and Z_2 are chosen to protect the input from positive spikes greater than 12 V whilst Z_3 and Z_4 protect the device from negative going spikes greater than -6.8 V.

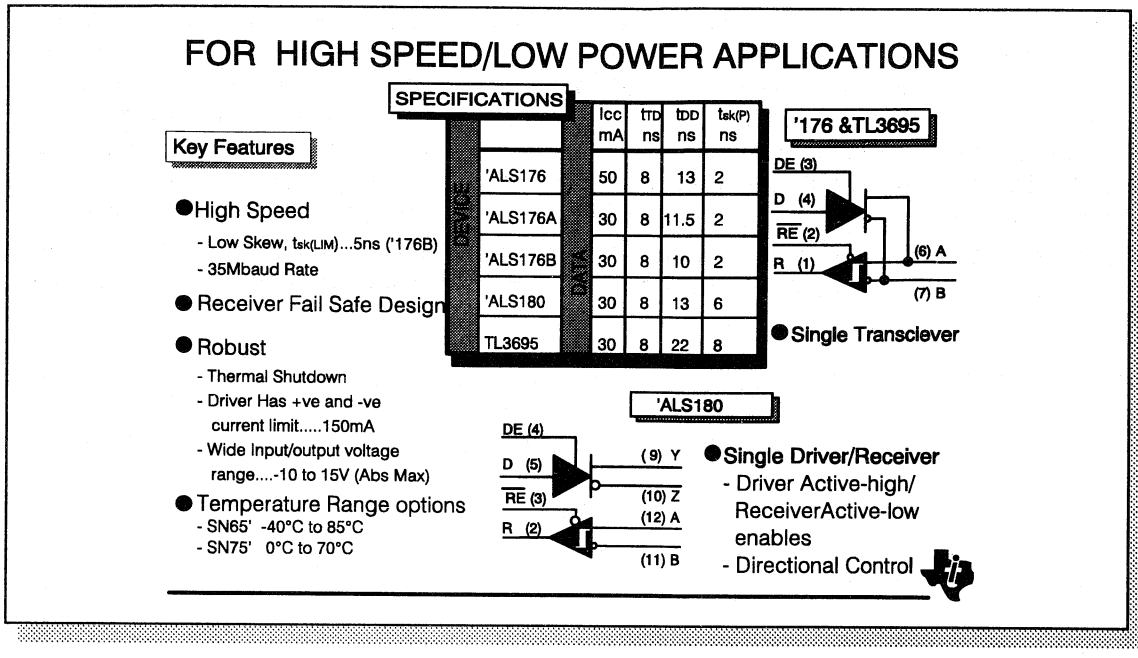


Figure 17 - SN75ALS' Series for High Speed/Low Power Applications

Product Description

In the previous noise protection example, the SN75ALS176 was introduced. This device forms just part of a range of high performance single line driver/receiver options available for RS-422 and RS-485 applications. Some key benefits of this range are discussed in the following text.

The range of devices shown in the figure are all high speed low power monolithic integrated circuits, designed for bidirectional data communication on multipoint bus transmission lines. The SN65ALS176, SN75ALS176 series and TL3695 are single differential transceivers, while the SN65ALS180 and SN75ALS180 are a single differential driver/receiver pair.

All devices are designed for balanced transmission lines and meet EIA standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

Notes

The SN65ALS176, SN75ALS176 series and TL3695 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver's differential outputs and the receiver's differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or V_{CC} = 0V. This port features a wide positive and negative common-mode voltage range making the device ideal for party line applications. All devices are available in either 8-pin dual-in-line plastic (P) or 8-pin plastic small outline surface mount (D) packaging.

The SN75ALS180 contains many of the same features listed above. However, the driver outputs and receiver inputs are not internally connected together but are brought outside the chip, offering a separate driver and receiver function. For this reason the SN65ALS180 and SN75ALS180 are housed in a 14-pin dual-in-line plastic and 14-pin small outline plastic packages. This arrangement makes the SN75ALS180 ideal for full duplex operation.

Product Differentiation

The SN75ALS176 series allows the designer to select between ac performance levels. The figure shows the maximum propagation delays and skew specification for the range. The SN75ALS176B offers the highest speed performance with a maximum differential output delay time of 10ns. With a minimum specified value of 5ns the device is capable of data rates in excess of 60 Mbaud (as per RS-485 specification).

Perhaps even more importantly, especially for high speed multi-channel applications (for example SCSI), is the low skew value, $t_{sk(LIM)}$. In this instance skew is specified as the difference between the maximum and minimum differential output delay times, T_{DD}. The SN75ALS176B has a minimum $t_{sk(LIM)}$ value of 5ns. This value is used to determine the delays in signals between channels in the system. The pulse skew, $t_{sk(P)}$, is specified as a minimum value of 2ns (See 'A discussion of Skew' in the 'The specifications and Transmission line practicalities 'section for further information).

The TL3695 provides the same functionality as the 'ALS76 series of devices, but is aimed at lower performance lower cost systems.

As the application areas for multi-point differential standards standard widen so to do the applications for the transceiver function.

On such emerging application is in the industrial environment, to connect between control modules (Masters) or process sensors (slaves). For this reason Texas Instruments has included the '65' temperature range option which extends the temperature range from the basic 0°C to 70°C option to -40°C to 85°C.

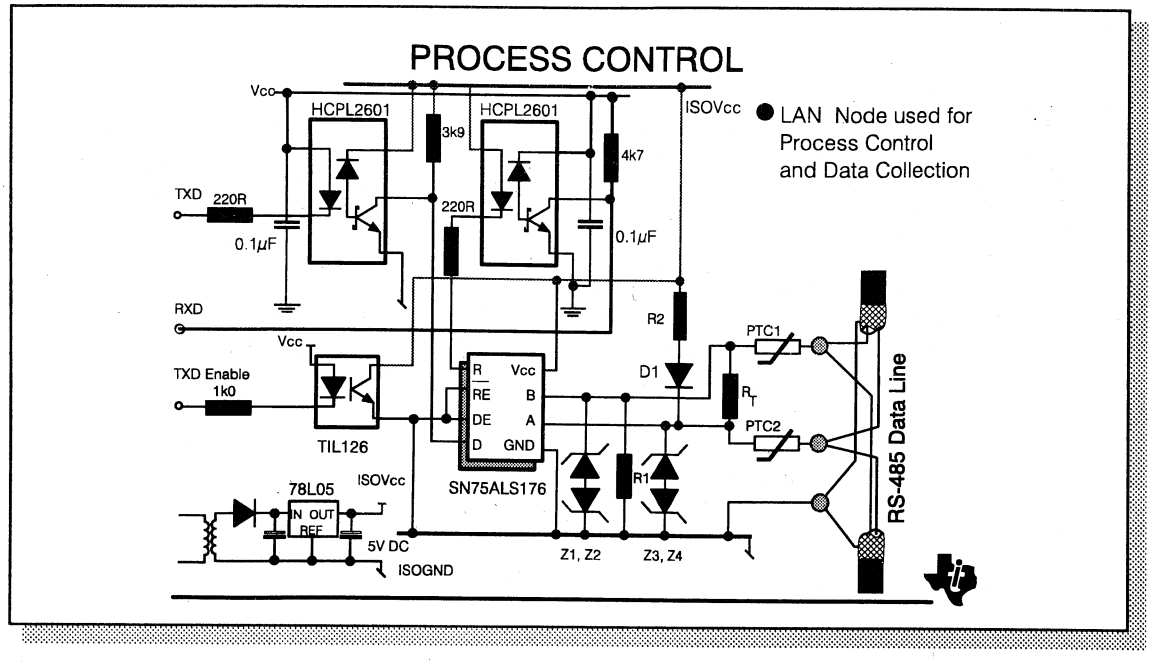


Figure 18 - Process Control Application

Process Control

In the previous sections the need for line termination, receiver fail safe and noise protection was highlighted. All these elements can be found in an industrial process control and data collection application, which is shown in the figure.

The need For Galvanic Isolation

The capability of meeting toughened noise legislation is a key requirement for many new end products and applications. Computer and industrial serial interfacing are areas where noise can seriously affect the integrity of data transfer, and a proven route to improved noise performance for any interface system is galvanic isolation.

Notes

Such isolation in data communication systems is achieved without direct galvanic connection or wires between drivers and receivers. Magnetic linkage from transformers provide the power for the system, and optical linkage provides the data connection. Galvanic isolation removes the ground loop currents from data lines and hence the impressed noise voltages which affect the signal are also eliminated. Common mode noise effects can be completely removed and many forms of radiated noise can be reduced to negligible limits using this technique.

Taking a more practical view of where problems are likely to occur when using a galvanic interface, can be found in the industrial environment. For example consider the case when the interface node, shown in the figure, connects between a data logger and a host computer via the RS-485 link. When an adjacent electric motor is started up, a momentary difference in ground potentials at the data logger and the computer may occur due to a surge in current. If no isolation scheme is employed for the data communication path, data may be lost during the surge interval and in the worst case damage to the computer could occur.

Circuit Description

The schematic shown forms an interface, one node, for a "distributed controlling, regulation and supervision (DCRS) system". Such a scheme could be used in a 'Field bus' type application. Transmission takes place via a 2-wire bus, formed by a twisted-pair, shielded cable connected in a ring circuit. Other nodes, master or slaves, may be distributed along the bus in an arbitrary fashion and may be separated hundreds of metres in distance.

The bus driver used is the **SN65ALS176**, chosen for its high data rate capability and low power consumption. Low power is crucial in this type of application since many remote outstations will either be battery operated or require battery back-up capability. The '65' option was chosen for its industrial temperature range of -40°C to 85°C.

Transceiver protection circuitry is formed by Z_1,Z_2,Z_3 and Z_4 along with current limiters PTC_1 and PTC_2 (see previous example). Line termination is formed by a combination of R_T, R_1 and R_2. The values of which can be calculated as follows;

$$R_1 = R_2 < 0.5 \times Z_O \times [1 + V_{CC}/V_{TH}]$$

and

$$R_T = Z_O [1 + V_{TH}/V_{CC}]$$

Using a cable with a characteristic impedance of $Z_O = 120\Omega$ and a desired V_{TH} of 200mV, requires $R_1 = R_2$ to be around $1.6k\Omega$ in value. The terminating resistor, R_T would be in the order of 124Ω.

The inclusion of $R_1 = R_2$, provides a receiver fail safe to open line conditions by biasing the polarity of the line to a logic '1' under line idle conditions.The values of $R_1 = R_2$ are best kept as low as possible to increase the noise rejection when the line is left floating, but they will place some loading onto the driver.

Galvanic isolation is afforded by means of three optocouplers/optoisolators. The HCPL2601 is chosen for its high data rate capability, t_p = 75ns (max), and its high voltage isolation.

The HCPL2601 is designed for use in high speed digital interfacing applications that require high voltage isolation between the input and output. Its use is highly recommended in extremely high ground noise and induced noise environments.

The HCPL2601 consists of a GaAsP light emitting diode and integrated light detector, composed of a photodiode, a high gain amplifier and a Schottky clamped open collector output transistor. An input diode forward current of 5mA will switch the output transistor low, providing an on state drive current of 13mA (eight 1.6mA TTL loads). A TTL input is provided for applications that require output transistor gating.

Housed in a single 8-pin dual-in-line plastic package the HCPL2601 is characterised for operation over the temperature range of 0°C to 70°C. The internal Faraday shield provides a guaranteed common mode transient immunity of 1000V/μs.

A 0.1μF capacitor has been connected between V_{CC} and ground to improve switching performance.

Automotive Applications

Other emerging application areas are in the automotive industry, where even higher demands are made on the temperature range options of line interface circuits. One such area is the use of data transmission devices in low power data distribution systems, known as multiplex wiring.

Although the gradual trend in automotive applications is towards full multiplex wiring, where one common bus runs throughout the car (described below), an interim solution is to use several buses serving common systems.

Notes

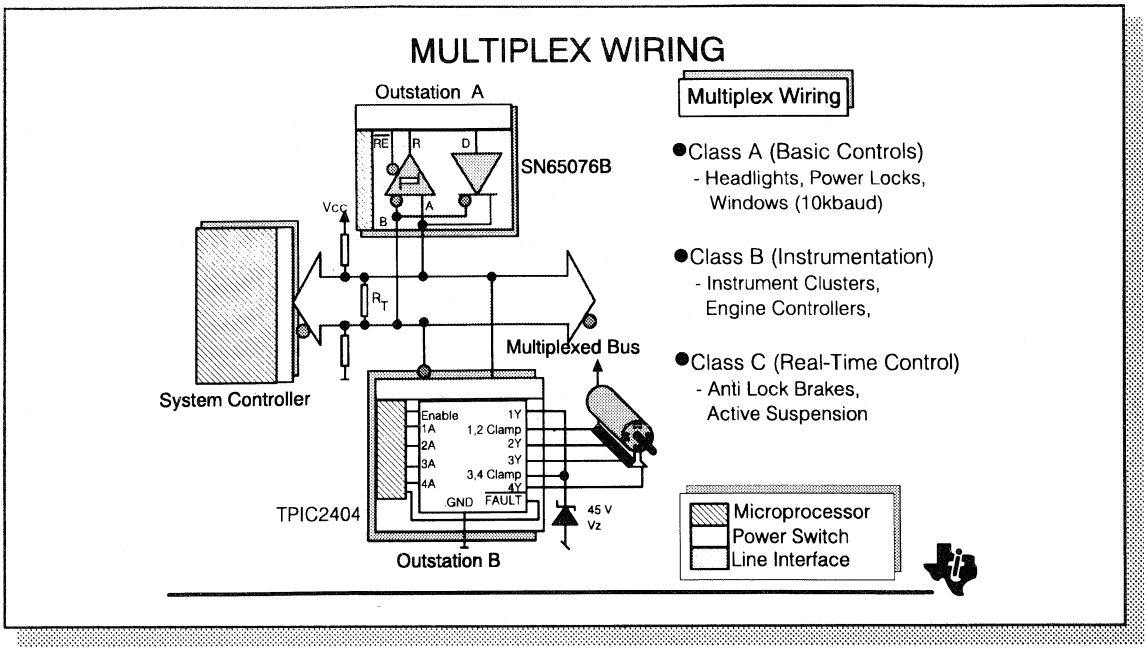


Figure 19 - Multiplex Wiring

Multiplex wiring is seen as a way to replace the costly and cumbersome conventional wiring harness that runs throughout the car. This harness, made up of thick copper wire and heavy duty switches is used to deliver the full load current from the battery to the load (actuator, lamp..etc) This approach as well as being costly is heavy, very difficult to test for faults, repair and is inflexible. Although the use of multiplexing is ultimately seen as giving cost advantages its more immediate use is to fix the afore mentioned problems.

In a typical multiplexed system, a central controller will communicate with 'outstations' (which house both the control switches and load drivers) via a common distributed bus. Typical components of the system, shown in the figure, will require a system controller, differential line driver/receiver and intelligent power switch.

The central controller is responsible for implementing the communications protocol, which allows data, status, address and control information to be exchanged with the outstations. Part of the information exchange could be diagnostic data from the outstation power switch, used for driver instrument panel information or fault diagnosis during repair.

The central controller communicates over the bus via line interface devices. Due to the electrical hostile environment and the need for high reliability (especially in safety critical applications) a differential data transmission scheme is used which gives increased noise immunity.

The final requirement is for a local intelligent power device, which exchanges the low voltage TTL/CMOS logic level from the interface device to a high current, high voltage level to control the actuator. In addition to their power transfer characteristics, these devices should provide

simple error sensing capabilities which can detect device or actuator problems. Such a device could be the **TPIC2404** which is a monolithic high-voltage high-current quadruple low-side switch.

Automotive data buses can be broken down into three main categories;

Class A buses include basic controls, such as headlights, power locks and widows;

Class B buses cover instrument clusters, engine controllers, trip computers and other areas requiring exchange of information;

Class C buses, which are the furthest from implementation, include real-time control applications, for example anti-lock brakes, active suspension systems, and other engine controls.

The application and position of the outstation dictates the temperature range required from the interface circuit. For example outstations situated in the engine compartment will require a wider operating range than an outstation situated behind the instrument cluster.

Product Support

Texas Instruments has an on-going programme to provide interface devices which support all the major automotive standards. These standards include the SAE J1850 standard and European standards CAN and VAN. Of particular note are the LinBiCMOS developments for the J1850 standard. These devices are differential current mode line/drive receive devices which contain over 300 logic gates for memory buffering, thus allowing message handling capability. Use of LinBiCMOS provides the robustness, wide voltage ranges and extended temperature ranges required for automotive applications.

Early implementors of partial multiplex wiring systems have capitalised upon the advantages offered by the SN65176B device. However for real high temperature application, (i.e. outstation situated in the engine compartment) further temperature range extensions are required. For this reason the **SN65076B** was developed, and is characterised for operation from -40°C to 105°C. Special selections may extended this range further still.

The SN75076B achieves this high temperature range of operation by application optimisation, i.e. by eliminating all unnecessary functions the device's power dissipation can be kept to a minimum. For example, complicated enabling schemes are not required since most

Notes

automotive electronic designers using the SN75176B hardwire the driver input either high or low and apply the signal input to the enable. This provides one active state (driver enabled) and one passive state (driver disabled). To enable this to function correctly a three resistor termination network is required, such that resistors polarise the line to the opposite polarity as the driver leaves its active state. Therefore the driver input circuitry and one half of each input are redundant. The SN75076B removes this circuitry, thus reducing its device power dissipation. Additionally the cable lengths are quite short so there is no need for a high current drive capability Hence the SN75076B has an output current drive capability of only ±10mA, which while reducing the power dissipation overheads further, is still more than adequate for multiplex wiring applications.

Product Description

The SN65076B and SN75076B differential bus transceivers are monolithic integrated circuits, designed for bidirectional data communication on multipoint bus transmission lines. They have been optimised for use in noisy environments, for example automotive, where a low impedance termination to ground is required.

The SN65076B and SN75076B combine a differential line driver and a differential line input receiver, both of which operate from a single 5V power supply. The receiver has an active-low enable. The driver's differential outputs and the receiver's differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or V_{CC} = 0V. This port features a wide positive and negative common-mode voltage ranges making the device ideal for party line applications.

The driver is designed to handle loads up to 10mA of sink (B I/O) and source (A I/O) current. The driver features positive and negative current limiting and thermal shut-down for protection from line fault conditions. Thermal shut-down is designed to occur at a junction temperature of approximately 150°C in the P package and 170°C in the D package. The receiver features a minimum input impedance of 12kΩ, an input sensitivity of ±200mV, and a typical hysteresis of 50mV.

Both devices are available in either 8-pin dual-in-line plastic (P) or 8-pin plastic small outline surface mount (D) packaging. The SN65076 is characterised for operation from -40°C to 105°C and the SN75076 is characterised for operation from 0°C to 70°C.

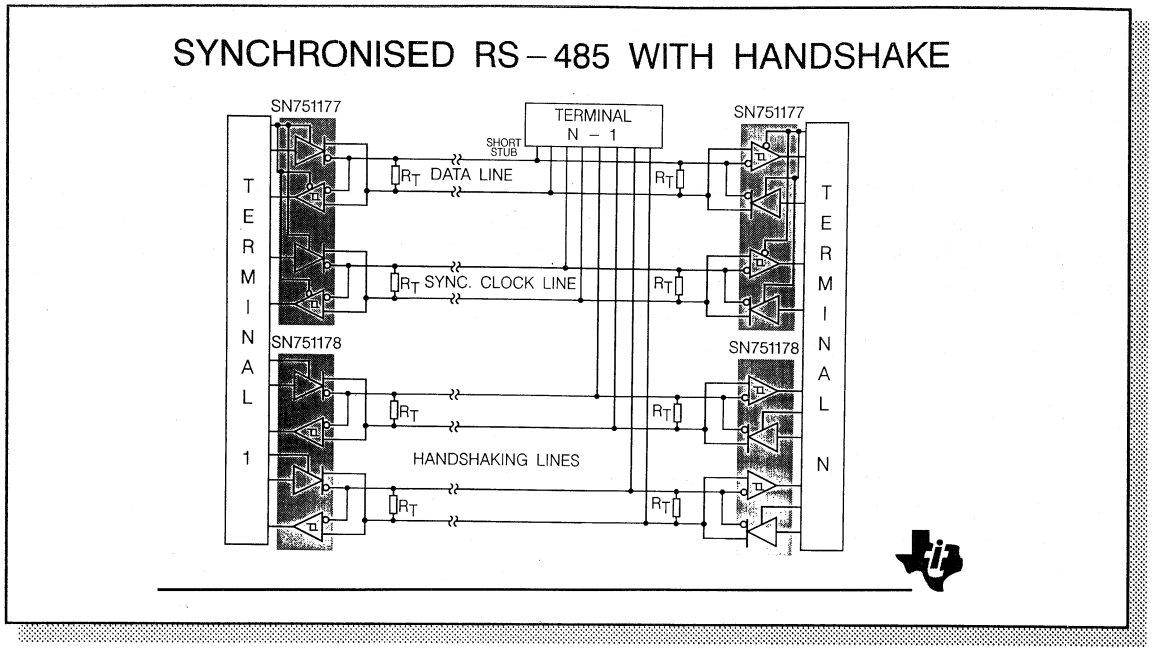


Figure 20 - Synchronised RS-485 with handshake

Boost the Data Rate

Most RS-485 systems operate with a single twisted pair as the data transmission medium limiting the data transfer to asynchronous mode. In addition, the single line must also transfer receiver address, start and stop bits and a preamble to enable the receiver logic to distinguish between data or rubbish on an idle line. These additional transferred bits impact the speed of operation on the data line.

Alternatively, synchronised data transfer can be implemented by adding an additional sync. clock line as shown on the figure, and can be further complemented with the addition of a couple of handshake lines. The overall transfer of the "real data" can be significantly speeded up, as most of the control bits used in asynchronous mode will be eliminated from the data path.

Notes

Specifically, synchronous data transfer benefits from applications where complete blocks of data can be transferred because the usual requirement in asynchronous transfer for breaking the data down in small groups of 8-bits (proceeded with a start bit and concluded with a stop bit) is eliminated.

Several terminals or station can be connected to this synchronised RS-485 system. The number of stations is only limited by the usual rules for RS-485. Daisy-chain connection between terminals is required unless each terminal is connected to the main data path via a short stub as the shownfor terminal number N - 1.

Why use the SN751177 and SN751178 ?

The SN751177 contains two drivers and two receivers in a single 16-pin package. Each pair of drivers and receivers has a common enable line. Upon transmission, both the data and sync. clock drivers are enabled allowing synchronous transfer of data. When shifting to receiver mode, both drivers are disabled, and the two receivers are enabled simultaneously. Due to the complementary enabling schemes for drivers and receivers (logic 1 enables the drivers but disables the receivers, and logic 0 the opposite), it is possible to connect both driver and receiver enable signals to the same control output. This reduces the number of I/O's required.

The SN751178 also contains two drivers and two receivers in a 16-pin package, but offers a different enabling pattern. The two receivers are always active and listen continuously to the handshake lines as necessary. However, the two drivers can be independently enabled as required by a handshaking scheme.

In summary, the SN751177 and SN1178 offer a simple but versatile solution sunchronous transfer of data at high speeds. Their configuration as two driver/receiver pairs adds to the effectiveness of the application

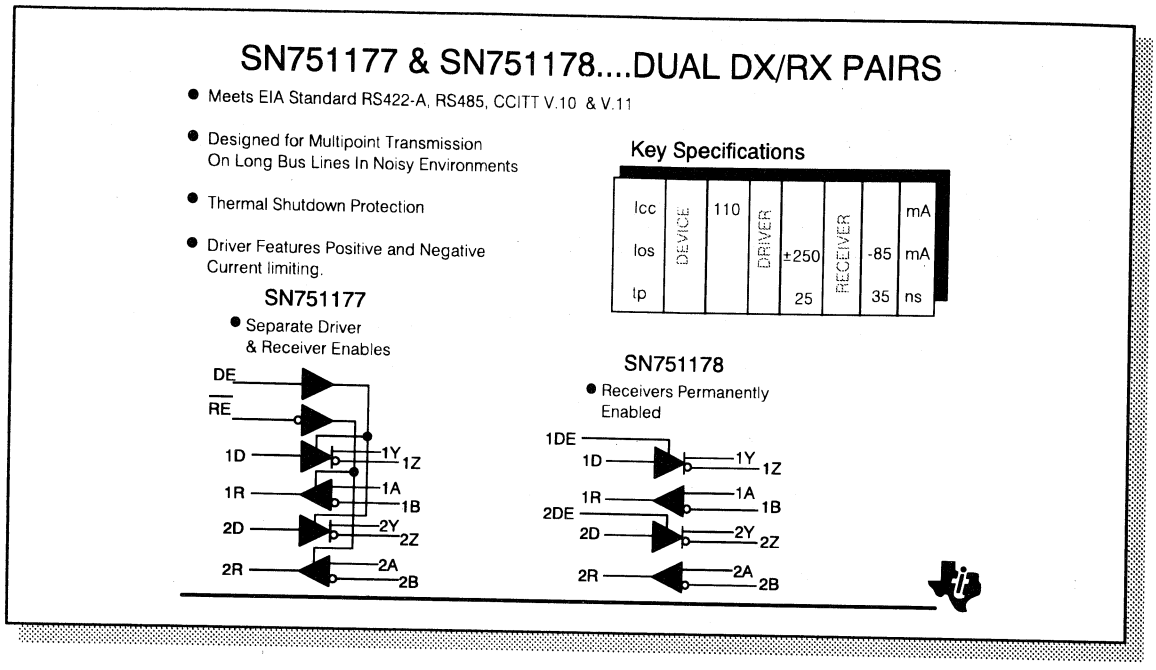


Figure 21 - SN751177 and SN751178 Dual DX/RX Pairs

Product Description

The SN751177 and SN751178 dual differential drivers and receivers are monolithic integrated circuits designed for balanced multipoint bus transmission at data rates up to 10Mbaud. They are designed to improve the performance of full-duplex data communications over long bus lines and meet EIA standards RS-422, RS-485 and several CCITT recommendations.

The SN75117 and SN751178 driver outputs provide limiting for both positive and negative currents and thermal shutdown protection from line fault conditions on the transmission line.

The receiver features include a high input impedance of 12kΩ, an input sensitivity of ±200mV over a common-mode input voltage range of -12 V to +12V and a typical hysteresis of 50 mV. A fail safe feature ensures that if the receiver inputs are open, line idle, the receiver outputs will always be high.

Notes

The SN751177 drivers and receivers are enabled in pairs. An active-low RE enables both receivers, whilst an active-high DE enables both drivers. The SN751178 has an enable for each driver, whilst its receivers are permanently enabled. Choice of enabling scheme offers flexibility in application, allowing use as repeaters, direction control or data lines in full, half duplex and simplex modes of operation.

Both the SN751177 and SN751178 are characterised for operation from -20°C to 85°C, and are available in 16-pin dual-in-line plastic packages.

Future developments of these products will include ALS-Impact™ versions resulting in lower power consumption and increased speed.

Impact is a trade mark of Texas Instruments

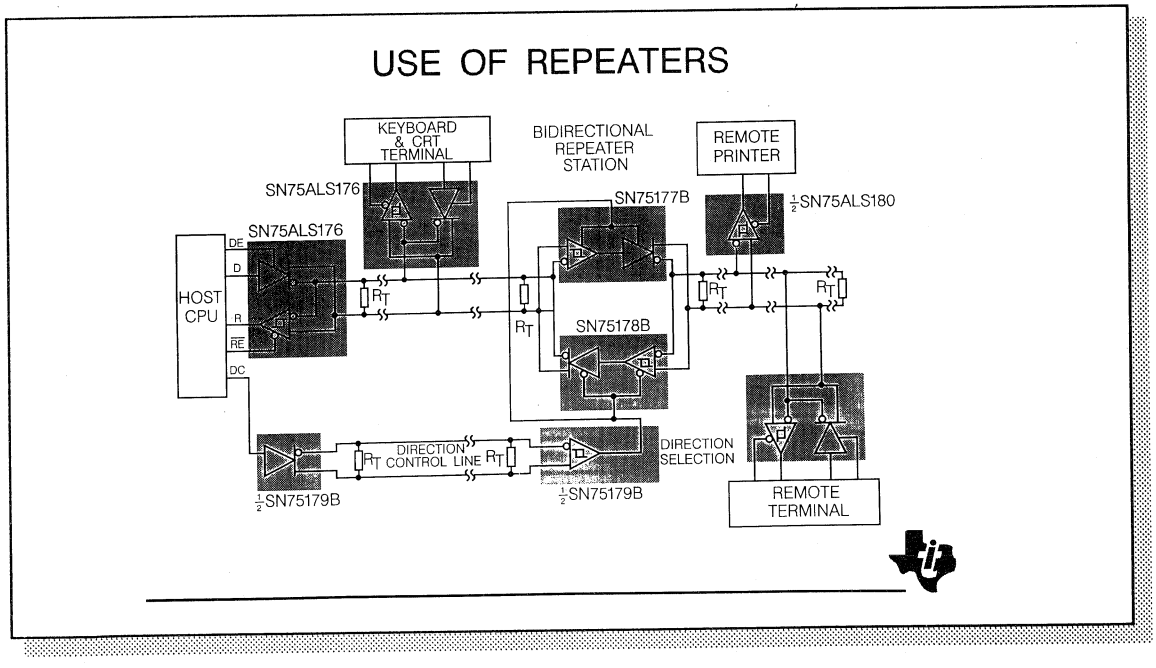


Figure 22 - Use of Repeaters

The Need for Repeaters

The major advantage of RS-485 is that it permits multiple drivers and receivers to operate over a 2-wire bus, thus setting up a party-line architecture. When such a data communication bus system is transmitting data over lines as long hundreds of meters or even thousands of metres, attenuation is often experienced between a driver at one end and a receiver in the other end (over long distances the cable's resistance does have an effect). Such systems can benefit from the use of signal restoration by means of bus repeaters.

Similarly, when more than 32 unit loads are connected to a bus, requirements for additional buffering arise. A bus repeater has in this function a different role from restoring the original signal namely to drive another 32 unit loads.

Repeater Solutions

Bus repeaters in data communication systems receives degraded signals from the transmission line, squares up the pulses, and retransmits the signals onto the line to the receiving station. Because the original transmitted signal is restored (squared up), the communication system becomes less susceptible to noise and other types of interference on the lines.

The shown "use of repeaters" application for bidirectional control of an RS-485 bus with long transmission lines is implemented with a bidirectional repeater station. Two types of repeaters are available: One version is enabled by a logic 1 control signal and the other by a logic 0. Thus, without any glue logic you can design a fully bidirectional repeater station that restores signals from both directions on a line

Enabling and disabling of the repeater drivers and receivers and thereby the data direction is controlled by the host microcontroller. In data communication systems where no host CPU controls the data direction, intelligence needs to build into the repeater station to maintain system control. This allows also for independent communication on each side of the repeater station providing additional flexibility and faster overall data exchange.

Recommended Products

Dedicated products designed specifically for repeater purposes are the SN75177B and SN75178B. Employing these repeater devices in simple repeater stations as the shown, completely eliminates the need for any glue logic due to their enabling scheme. For repeater stations including protocol controllers may also benefit from devices such as SN751177 and SN1178 with their multiple drivers and receivers.

Notes

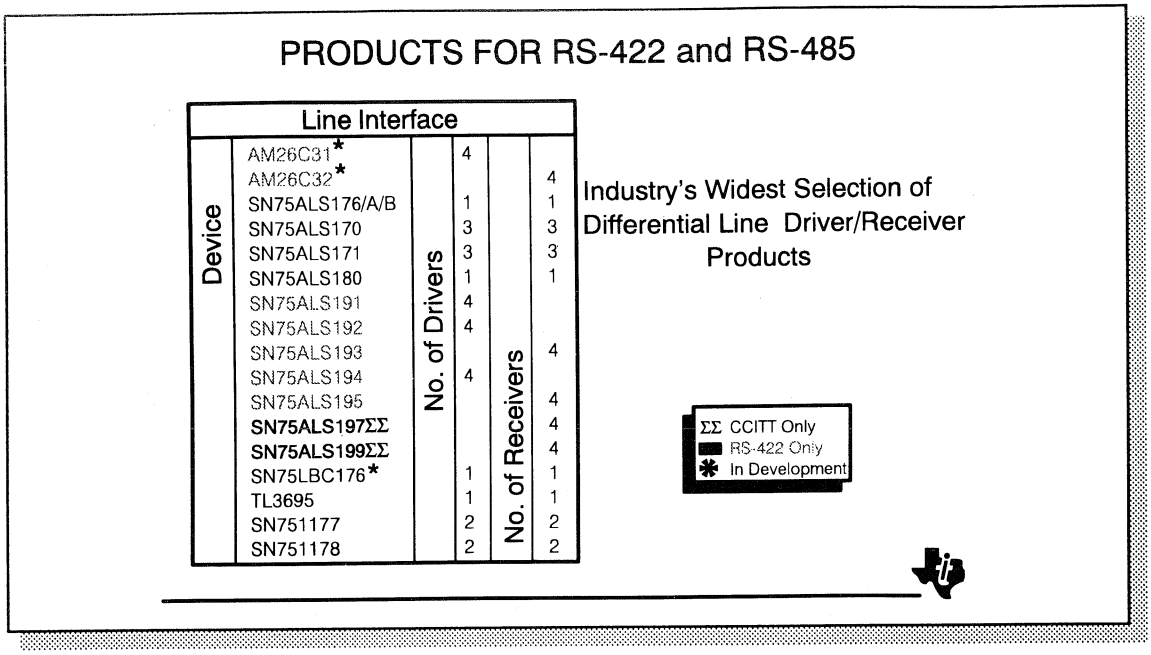


Figure 23 - New Products For RS-422 and RS-485

The figure shows the range of devices available for the EIA RS-422 and RS-485 standards. Of particular note is the trend towards devices combining low-power and high-speed capabilities which also offer a variety of enablling schemes and multiple driver/receiver combinations. Also of note are the SN75ALS170, SN75ALS171 and SN75LBC176, these are the subjects of the following section.

The ANSI Small Computer Systems Interface

Introduction

The following Section describes briefly the range of products available for the Small Computer Systems Interface, SCSI. A more detailed discussion of SCSI can be found in the data transmission glossary section.

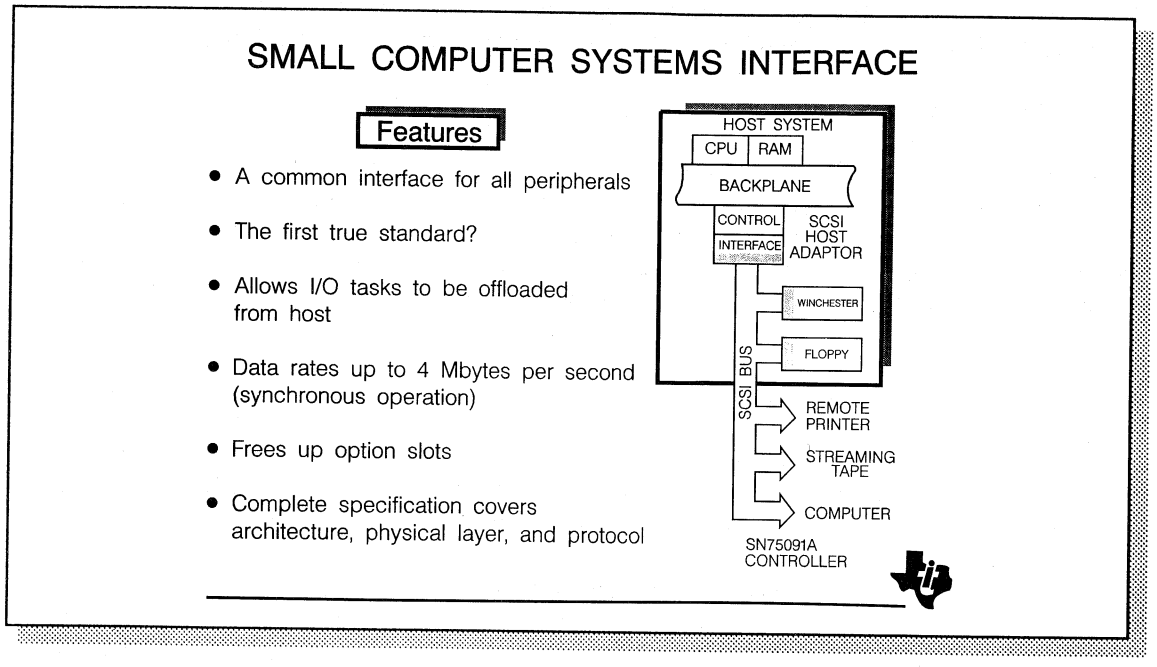


Figure 24 - Small Computer Systems Interface

The ANSI SCSI interface is used to form the connection between computers and their peripherals. These peripherals may be disk drives, optical storage devices, scanners, tape drive, laser printers..etc all of which may be connected together via a common bus system.

Notes

Moreover, the standard embraces the mechanical, electrical and functional requirements for a small computer input/output bus interface and contains command sets for intelligent peripheral devices In particularly the needs of storage devices commonly used in small computer systems are addressed.

The key use of any dedicated interface control circuitry is to off-load all the interfacing activity from the CPU. Employing a dedicated peripheral interface allows the CPU to concentrate on more computational activities whilst the peripheral controller takes care of all the timing and data exchanges between peripherals. The SCSI takes this one stage further by presenting the same interface irrespective of peripheral type or manufacture.

The SCSI Advantage

SCSI offers advantages to both the equipment user and the equipment vendor. Users benefit from increased system performance and a wider choice of compatible peripherals available 'off the shelf, which are not system specific. Vendors benefit by not having to design individual interfaces for each different disk drive or peripheral that they supply. Standardisation between manufacturers increases the size of the potential market for the product.

SCSI is capable of supporting communication between multiple computers as well as computer to disk drive for example. Also, disk to disk data transfers can take place which execute completely independently from computers on the bus. The bus is therefore 'intelligent'. This is one of the prime reasons for an intelligent I/O bus, like SCSI, to off-load some of the more mundane but time intensive I/O cycles from the host CPU.

SCSI can support up to eight peripherals (including the master). Each peripheral can in turn support a further eight logical units, which can drive up to 256 logical subunits. Thus a total of 14, 000 peripherals can be supported on one SCSI bus providing there is one host and each peripheral is a logical subunit. Since a computer only needs one host adaptor, it would be unrealistic to need to drive more than 14,000 peripherals, only one option slot is required on the system backplane. For example, here is now no for separate RS-485, Ethernet or tape streamer interface cards

The SCSI may be configured to operate in asynchronous or synchronous mode. Further more it can be either single ended or differential. An asynchronous system operated with single ended transmission would be used for short distance communication and would permit a line length of up to 6 metres at a data rate of 1.5 Mbytes/second. Whilst a synchronous system with differential transmission would drive a line of 25 metres in length at a data rate of 4 Mbytes/second.

It should be noted that the differential interface used complies to the EIA RS-485 standard.

In the simplified diagram shown, each peripheral including the host, will require a SCSI controller. The SCSI controller is responsible for passing information from the SCSI bus to the host µP bus or control electronics situated in the peripheral. It ensures that all data transfers and bus communication complies to the SCSI protocol.

Additionally each peripheral will require up to 18 line drive/receive devices to implement the SCSI bus, which consists of data-bits, parity-bits, and control-bits.

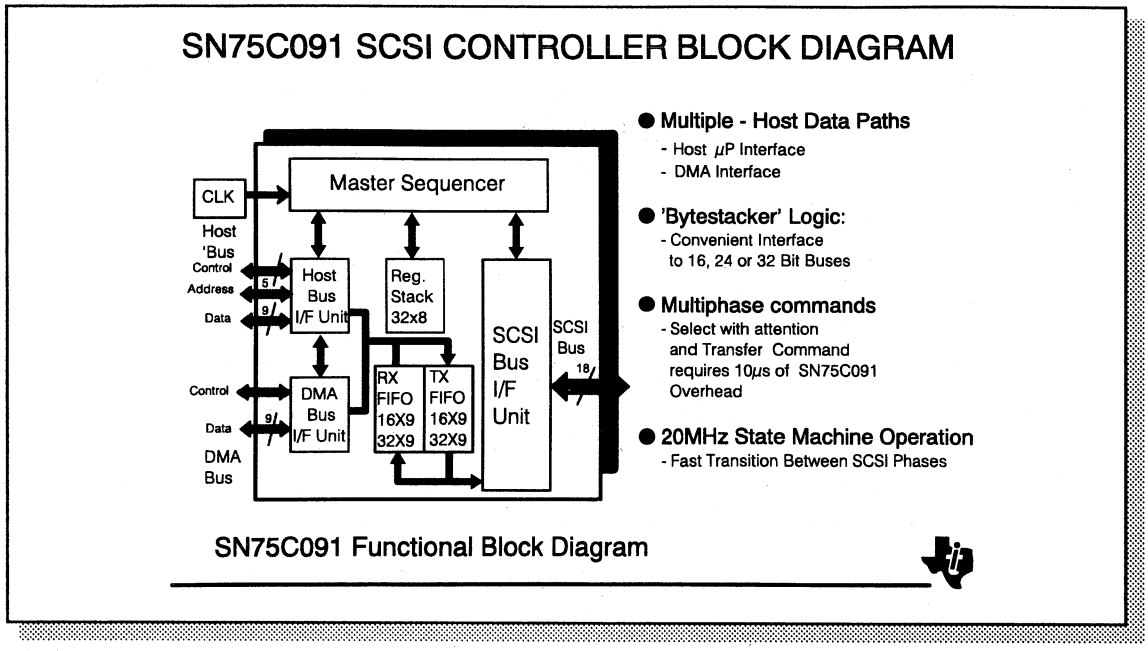


Figure 25 - SN75C091A SCSI Controller Block Diagram

Powerful, Flexible and Easy to Implement

Today's systems designers regard SCSI (Small Computer System Interface) as the interface of choice for many applications. Originally designed for PC hard disk systems, SCSI is now being implemented in a variety of applications, such as tape drives, minicomputers, engineering work stations, optical disks, laser printers and many more.

To meet your interfacing needs, Texas Instruments introduces the SN75C091A SCSI bus controller. The SN75C091A meets the ANSI X3T9.2 standard and provides additional unique features over and above those of other SCSI controllers. The most important and powerful features include:

Notes

* **Multi-phase commands -**
  Each command executes a series of SCSI phases, reducing interrupts. This minimizes microprocessor (µP) intervention and increases throughput. For example, one command performs a complete initiator transaction from arbitration to command complete in as little as 12 µs.

* **Byte Stacker -**
  Provides an efficient method of converting words (up to 32 bits) into 8-bit SCSI bytes and back again. This allows convenient interface to 16-, 24-, or 32-bit buses.

* **Multiple-host data paths -**
  Separate DMA (direct memory access) and µP interfaces allow the µP to interrogate the SCSI controller during command execution without disrupting the data transfer.

SCSI provides system flexibility along with the compatibility and speed you need to improve and upgrade your system. Able to perform both initiator and target roles, the SN75C091A is designed for high-end applications transferring data synchronously or asynchronously at speeds up to 5 megabytes per second. **The device also conforms to single-ended transmission requirements incorporating on-board drivers, eliminating the need for external transceivers.**

The SN75C091A gives you the ability to control many operations that would often require undivided attention from the µP. Freeing the µP from these dedicated tasks, the SN75C091A SCSI controller improves your system's speed and performance.

This device is available now in a 68-pin plastic leaded chip carrier (PLCC).

Enhanced Features	Benefits
*** Multi-phase Commands**	Minimizes µP intervention and increase throughput.
*** Byte Stacker**	Provides flexible interface capabilities to 16-, 24- or32-bit busses.
*** Multiple Host Data Paths**	Allows for interrogation of the SCSI controller without disrupting data transfer.
***20-MHz State Machine Operation**	Permits fast transition time between SCSI phases providing a dramatic increase in performance.
***Separate 32-byte Receive and Transmit FIFO's**	Provides a data path buffer freeing µP to perform other tasks.
***Automatic Handling of Save Data Pointer Messages**	Relieves µP from the need to perform interim data pointer updates

AN OBJECTIVE COMPARISON OF SCSI CONTROLLERS

DESCRIPTION		TI SN75C091	ADAPTEC AID–6250	EMULEX/NCR ESP	NCR NCR5385E	MD MD33C93
Speed	ASYNC (Mbytes/S)	3+	3	3	3.0	1.5
	SYNC (Mbytes/S)	6	5	5	None	4
	Max SYNC offset (bytes)	15	8	15	None	5
Data buffering	Separate RX and TX FIFO's	Yes	No	No	None	No
	FIFO depth	16	8	16	–	5
	Width	9	8	8	–	8
Parity	Host/SCSI/both	Both	Both	SCSI	SCSI	SCSI
	Error options	5	3	1	2	2
	Pass–through	Yes	No	No	No	No
Host I/F– Reg. addressing	Direct MUX/non–MUX/both	Both	Both	N–MUX	N–MUX	MUX (some)
	Indir MUX/non–MUX/both	None	None	None	None	Both
Host I/F– Register access	Burst DMA supported	Yes	No	No	Yes	No
	Others	AFIFO	None	None	None	DBA
Host I/F ports	Dual ported	Yes	Yes	No	No	No
	Data I/F size (pins)	9	9/18	8	8	8
CMD chaining	# of CMDS supported	Good	?	Limited	None	3
Messages	# of MSG supported	Good	?	Limited	None	Limited
Diag support	# of options	Good	None	None	Good	None
Interrupt logic	# of options	Good	Limited	Limited	Limited	Limited
Package	PLCC – # pins	68	68	68	68	44
	DIP – # pins	No	No	No	48	40
Other features	BYTE stacker control lines	Yes	None	None	None	None
	Optional halt on ATN	Yes	No	No	No	No

Figure 26 - An Objective Comparison of SCSI Controllers

Important Notice

The table shown lists out the key parameters for a SCSI controller. The list is by no means exhaustive and the reader is urged to consult the various manufactures literature for the most up to date and accurate information. Although believed to be correct, no design decision should be undertaken on the basis of this information.

SN75C091A Position in The Market

By comparison of the figures the SN75C091A offers both the lowest SCSI and CPU bus overhead. This is borne out by studying parameters such as speed, data buffering, availability of DMA, message handling and interrupt logic. The additional feature of byte stacker should also be comprehended.

Notes

The SN75C091A is aimed primarily at multitasking PC's or workstations that need to off-load much of the mundane interface activities. Other applications can be found in server systems where the SN75C091A is used to interface to vast banks of disk drives. The SN75C091A is also well suited to high performance disk drive systems utilising the high performance features that SCSI can offer. For example the copy command. Initialising the copy command causes the disk drive to first act as target, to access the data, and then as initiator to copy the data to other nodes.

Data Support

In support of the SCSI controller the SN75C091A, Texas Instruments has released a comprehensive **data manual**, which contains over 60-pages of detailed information.
See the literature list for ordering details.

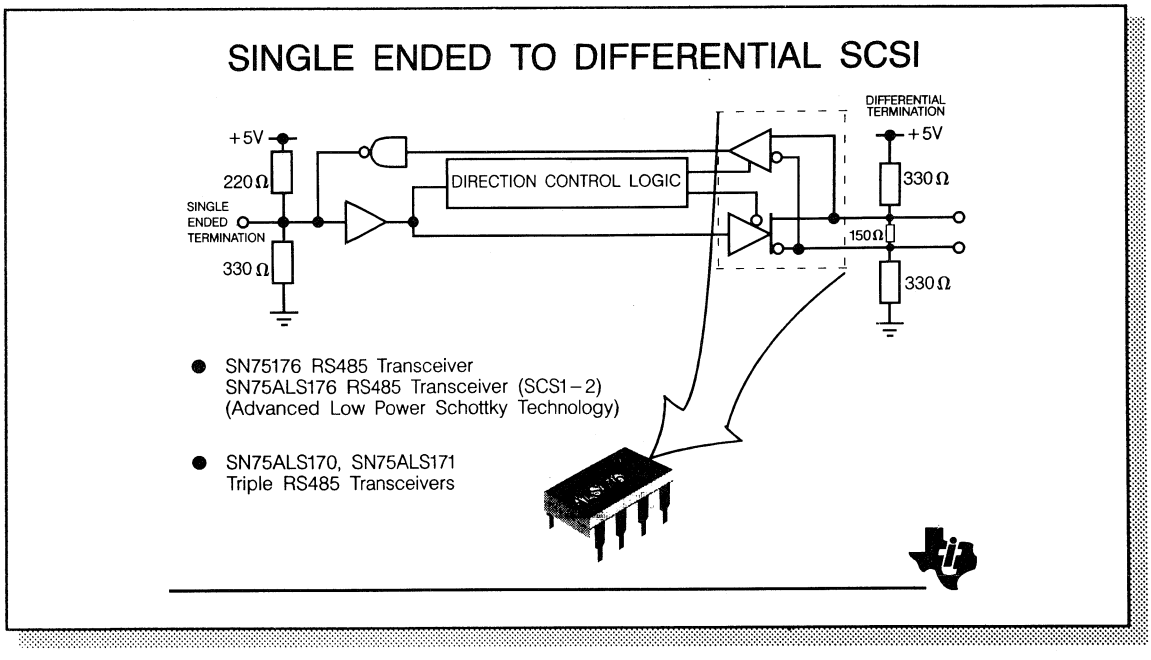


Figure 27 - Single Ended to Differential SCSI

As briefly mentioned earlier, differential SCSI is often desirable for driving longer line lengths (ie cabinet to cabinet) or where noise interference is a potential problem. Unfortunately most controllers only have single ended drive capability, this figure shows the basis of a single ended to differential output converter.

The single ended output is used to drive the TTL compatible inputs of the SN75ALS176. Direction control can be implemented using PAL's which control the driver and receiver pins on the SN75ALS176. The diagram also shows the single ended and differential line terminating techniques.

Most SCSI controllers for single ended implementation usually incorporate the required 48mA drivers on-chip while those designed exclusively for differential bus operation (without 48mA drivers) require an external differential line interface. In either case the range of Advanced Low power Schottky devices from TI are ideal for this interface.

The advanced low power schottky devices feature low power and high speed capability making them ideal for SCSI operation. The SN75ALS176 is a single transceiver housed in an 8-pin package, with a maximum data rate capability of 37 Mbaud. The SN75ALS170 and SN75ALS171 are triple versions with different enabling schemes allowing for half duplex and full duplex operation. These devices are discussed in more detail in the following text.

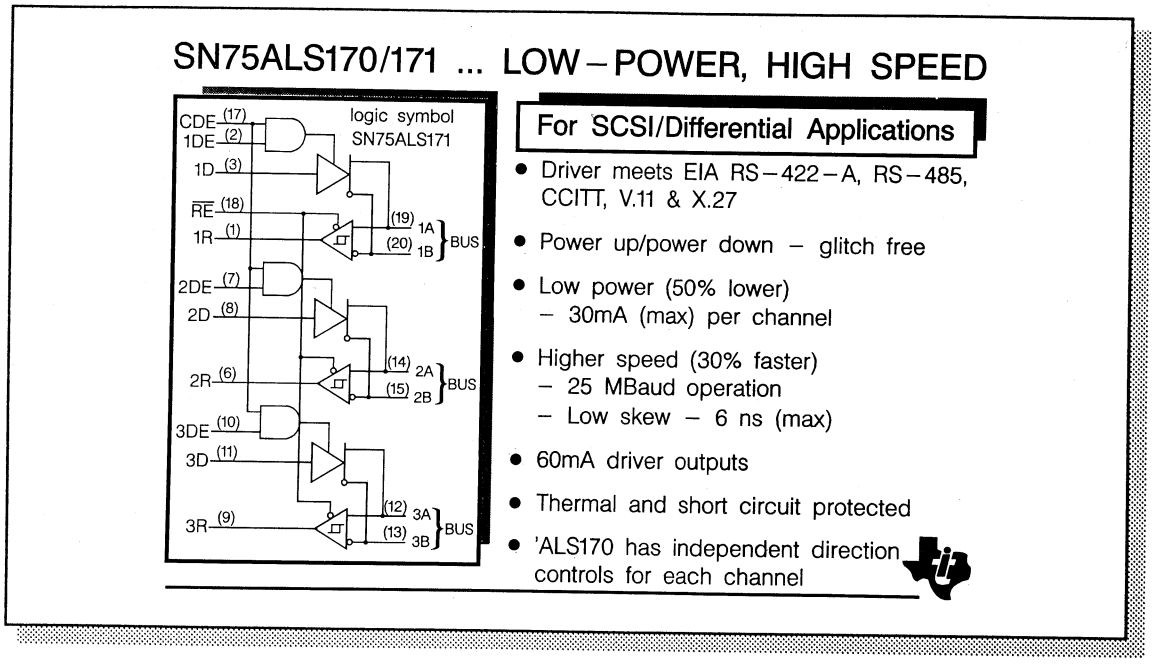


Figure 28 - SN75ALS170/171....Low-Power and High Speed

Product Information

The SN75ALS170 and SN75ALS171 triple differential bus transceivers are monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines.

Drivers and receivers in the SN75ALS170 have active-high and active- low enables, respectively, which are internally connected together to function as a direction control. The SN75ALS171 has individual active-high and active-low, respectively. The driver differential output and the receiver differential input pairs are internally connected together to form a differential input/output (I/O) bus ports that are designed to offer minimal bus loading when either the driver is disabled or V_{CC} = 0V. These ports feature wide positive and negative common-mode voltage ranges making them ideal for party line applications.

Designed using a low-power high-speed Advanced Low power Schottky process these devices offer a 30 % improvement over Low Power Schottky technology devices, 30mA(max) per channel and a 50% increase in speed performance, 25Mbaud capability.

The SN75ALS170 and SN75ALS171 are characterised for operation from 0°C to 70°C, and are available in either 14-pin ceramic (J), 20-pin wide body surface mount (DW) or 14-pin plastic dual-in-line (N) packages.

Figure 29 - The SCSI Interface (See Opposite)

There are a number of transceiver considerations to be accounted for when defining the interface for high performance systems such as the SCSI bus.

Although much detail is contained within the ANSI SCSI specification concerning most aspects of the electrical interface, ac considerations are not. The standard defines the overall bus timing requirements but the budgeting of timing error contributions is left to the system designer.

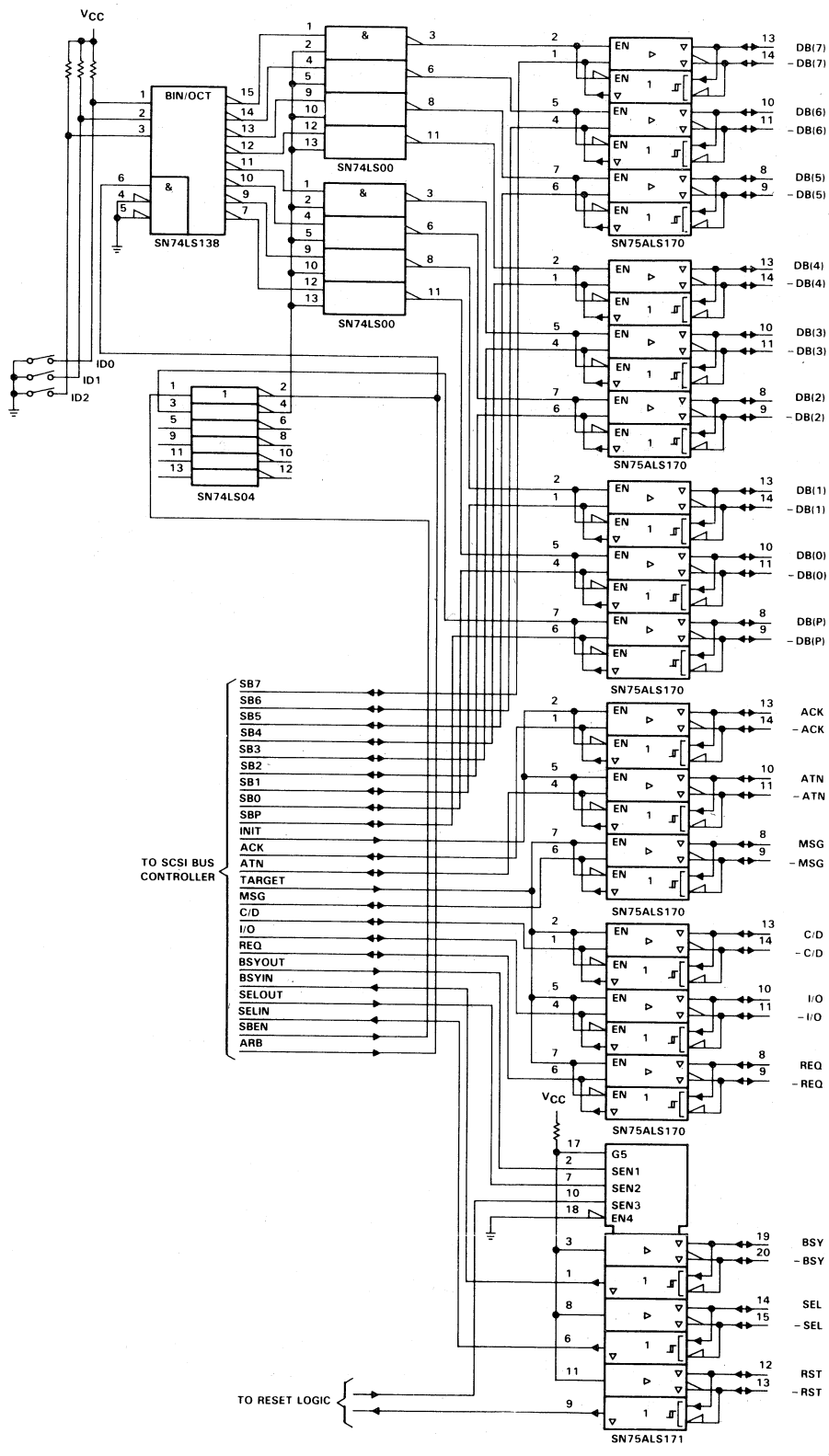
One of the most important transceiver parameters is $t_{sk(LIM)}$ or 'Skew Limit" This is normally known as the channel-to-channel or bus skew and is merley the difference between the minimum and maximum propagation delay times. This number represents the maximum time that a signal can lead or lag the same signal on another channel, regardless of the electrical path or the driver or receiver involved. The smaller $t_{sk(LIM)}$ the faster the bus will operate. Other "skew" contributers must also be considered to give the complete picture, for example pulse or device skew , $t_{SK(P)}$

The SN75ALS170 and SN75ALS171 have a $t_{sk(LIM)}$ of 10ns, while for even higher performance the SN7ALS176 has a speed graded versions available, giving options of 10, 7.5 or 5ns.

The figure shows a typical differential SCSI bus implementation, not shown for simplicity is the differential terminating scheme. The SCSI data bus is presently 8-bits wide, requiring eight transceiver devices. With the adittion of a parity bit and a nine channel command and control channel the total number of interface lines grows to eighteen. This can be implemented using just six SN75ALS170 or SN75ALS171.

The flow and exchange of information over the SCSI bus is controlled by a series of distinct transactions. There are up to eight transitions, or phases, and the SCSI bus must be in one of these phases at any one time. These phases determine the direction and content of the data lines. Three of these phases require a unique identifier (SCSI ID) which identify the SCSI device. This implementation uses the SN75LS138, which is a three to eight line decoder/multiplexer. This device is used to convert a hardwired selected binary address to assign the SCSI ID via the data bit enables during the Arbitration, Selection or Reselection phases of the SCSI bus.

The busy, Reset and Select lines of the SCSI bus are "wired-or" lines that can be driven by multiple devices simultaneously. The SN75ALS171 has been designed specifically for these lines. These signals are driven through the enable inputs to the driver.


VCC
BIN/OCT
SN74LS138
SN74LS00
SN74LS00
SN74LS04
ID0
ID1
ID2
SN75ALS170
SN75ALS170
SN75ALS170
SN75ALS170
SN75ALS171
DB(7)
-DB(7)
DB(6)
-DB(6)
DB(5)
-DB(5)
DB(4)
-DB(4)
DB(3)
-DB(3)
DB(2)
-DB(2)
DB(1)
-DB(1)
DB(0)
-DB(0)
DB(P)
-DB(P)
TO SCSI BUS CONTROLLER
SB7
SB6
SB5
SB4
SB3
SB2
SB1
SB0
SBP
INIT
ACK
ATN
TARGET
MSG
C/D
I/O
REQ
BSYOUT
BSYIN
SELOUT
SELIN
SBEN
ARB
ACK
-ACK
ATN
-ATN
MSG
-MSG
C/D
-C/D
I/O
-I/O
REQ
-REQ
G5
SEN1
SEN2
SEN3
EN4
BSY
-BSY
SEL
-SEL
RST
-RST
TO RESET LOGIC

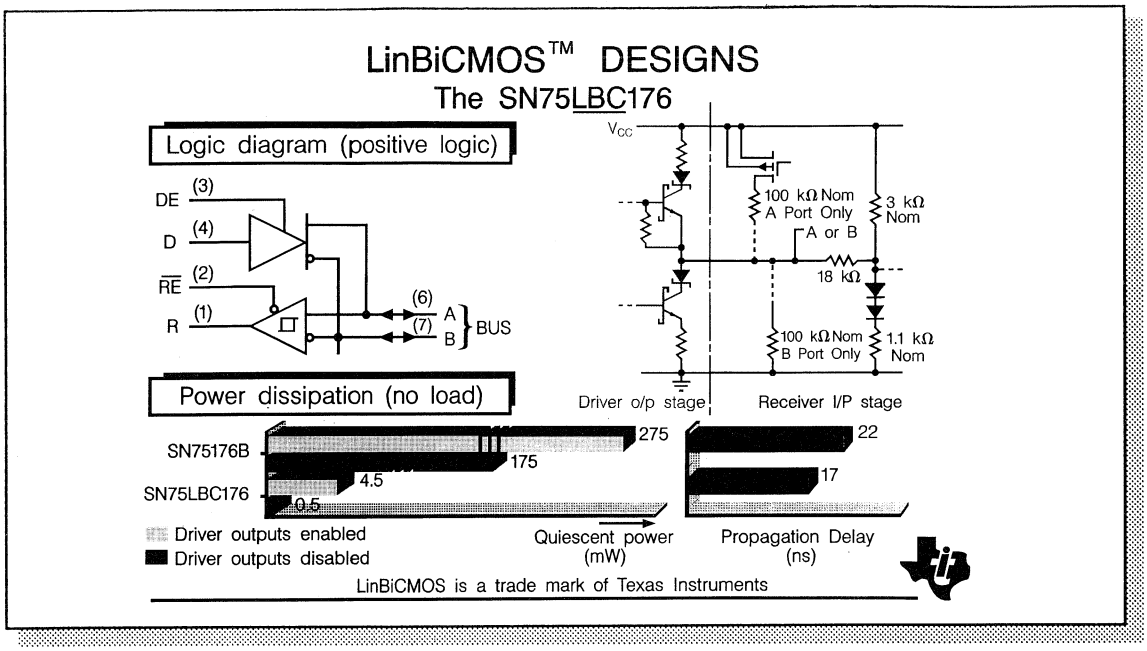


Figure 30 - Introducing The SN75LBC176

Product Features

The SN75**LBC**176 and SN65**LBC**176 are LinBiCMOS™ versions of the ALS176.

LinBiCMOS is a merged process which combines the low power advantages of analogue CMOS with the high voltage and speed capabilities of analogue bipolar. Using the LinBiCMOS process allows the '**LBC**176 to achieve a power supply consumption of **100µA (max),** no load conditions. Furthermore this is achieved without the usual speed penalties, the '**LBC**176 has a differential-output delay time of just **17ns(max)**, making it capable of data rates in excess of 17Mbaud (as per RS-485 specification).

The figure shows graphically the total power dissipated by the SN75LBC176 versus the standard bipolar part.

Reducing the SCSI Power Budget

This power consumption saving is best illustrated from a systems point of view. The worst case power consumption for a differential SCSI system is when all driver outputs are enabled (driving the line). Depending upon the driver output source impedance the output I^2R losses in the driver output circuit can be as high as 140mW.

Considering as an example 8-bit differential SCSI node operating as a target in 'data out' mode, which could conceivably drive fourteen of the eighteen SCSI, we can calculate the total power supply overhead;

$P_O = (V_{CC} - V_{OUT}) \times I_{OUT} \times n$ Where n = Number of channels

Therefore;

$P_O = 2.3V \times 60mA \times 14 = 1960\ W$

Power Dissipated in SN75C091A Controller

$P_{CQ} = 30mA \times 5\ V = 150mW$

Switching losses = 200mW (Estimated value)

Total dissipated in controller P_{CQT} = **350mW**

Power Dissipated in Transceivers ('176)

$P_{TQD} = 14 \times 41mA \times 5V = 2870mW$ (driver enabled, receiver disabled)

$P_{TQR} = 4 \times 55 \times 5 = 1110\ mW$ (Receiver enabled, driver disabled)

Total Power dissipated in SN75176 transceiver $P_{TT1} = 3970mW$

Total interface power dissipation = $P_{TT1} + P_{CQ} + P_O$ = **6280mW**

Power Dissipated in Transceivers ('LBC176)

$P_{TQD} = 14 \times 0.9mA \times 5V = 63mW$ (driver enabled, receiver disabled)

$P_{TQR} = 4 \times 3.9 \times 5 = 78\ mW$ (Receiver enabled, driver disabled)

Total Power dissipated in SN75**LBC**176 transceiver $P_{TT2} = 141\ mW$

Total interface power dissipation = $P_{TT2} + P_{CQ} + P_O$ = **2451mW**

Using the SN75LBC176 gives a power saving of nearly **4W**.

Notes

This power saving has been estimated by systems designers as high as $30/Watt in terms of reduced system design effort and increased reliability!

For future 16-bit SCSI systems the savings will be even more dramatic. Also, the LinBiCMOS process low power consumption and ease of integration makes the opportunity to integrate several devices onto on chip a reality. For example, TI is currently developing a range of devices that integrate multiple transceiver onto a single chip. The first of which contains six transceivers and will be available shortly.

A LinBiCMOS process has several advantages over a 'stetched' digital CMOS process. Firstly the analogue bipolar structures make the device inherently more robust and capable of operating within wide voltage ranges. Secondly the LinBiCMOS process makes use of fast bipolar schottky transistors, capable of 3GHz operation, allowing high data rates to be achieved. Also employing these transistors in the output stages eliminates the "latch-up" phenomena which plagues digital CMOS processes. Even when employing clever design or processing steps, the threat of latch up in CMOS structures cannot be totally ignored.

Study The Alternatives

Other semiconductor manufactures have made bold claims about their '485 device capability, capitalising on low power consumption due to the use of a N-Well CMOS process.
However this low power consumption is at the sacrifice of speed performance, and is only a part solution for high performance RS-485 or SCSI applications.

The SN75LBC176 is the only real solution!

Product Description

The SN65**LBC**176 and SN75**LBC**176 are high speed low power monolithic integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. Both devices are designed for balanced transmission lines and meet EIA standards RS-422-A and RS-485, CCITT recommendations V.11 and X.27, and ISO 8482:1987(E).

The SN65LBC176 and SN75LBC176 combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5V power supply. The driver and receiver have active-high and active-low enables, respectively, which can be externally connected together to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimal loading to the bus whenever the driver is disabled, or V_{CC} = 0V. This port features a wide positive and negative common-mode voltage ranges making the device ideal for party line applications. Both devices are available in either 8-pin dual-in-line plastic (P) or 8-pin dual-in-line plastic surface mount (D) packaging.

Both the driver and receiver are available as cells in the Texas Instruments LinASIC^{TM} cell library.

LinASIC is a trade mark of Texas Instruments.

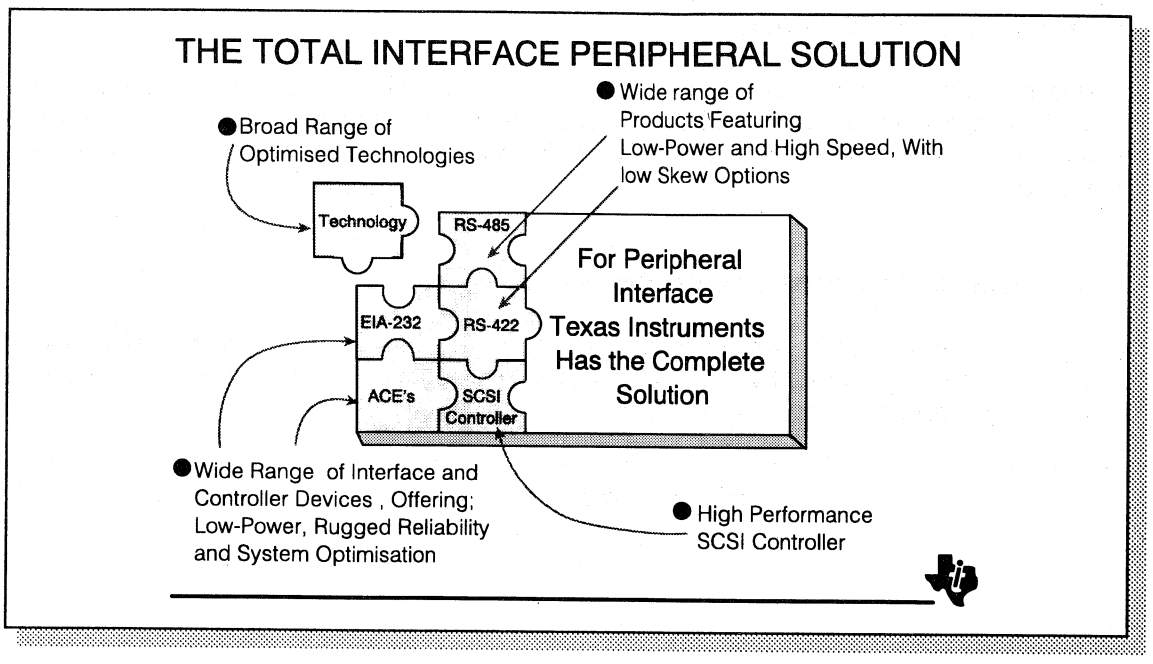


Figure 31 - The Total Peripheral Interface Solution

The range of products discussed throughout this section demonstrate the commitment made by Texas Instruments to the field of peripheral interfacing. Use of leadership technologies has enabled high performance line drive/receive functions to be produced and highly integrated controller functions. Key highlights are summarised below;

i) Technology

Broad range of technologies available from high density digital CMOS to high voltage, high speed analogue bipolar. Also increasing use of merged technologies offering the advantages of both bipolar and CMOS.

ii) Products for EIA-232

Use of optimised bipolar process to give low-power BiMOS driver/receiver range of products, optimised for common EIA-232 applications. Highly integrated controller functions containing up to two serial ports, one parallel port and FIFO'S for high end applications.

Notes

iii) Products for RS-422/RS-485

A wide range of devices suitable for many applications, from high speed disc drives to industrial and automotive applications. Particular emphases has been placed on low-power, high-speed devices offering low skew options for both telecommunications and disk drive applications.

iv) Products for the Small Computer Systems Interface

A highly optimised controller function specifically targeted towards high performance applications. Well supported by a range of transceiver options, which reduce system power supply consumption and reduce chip-count.

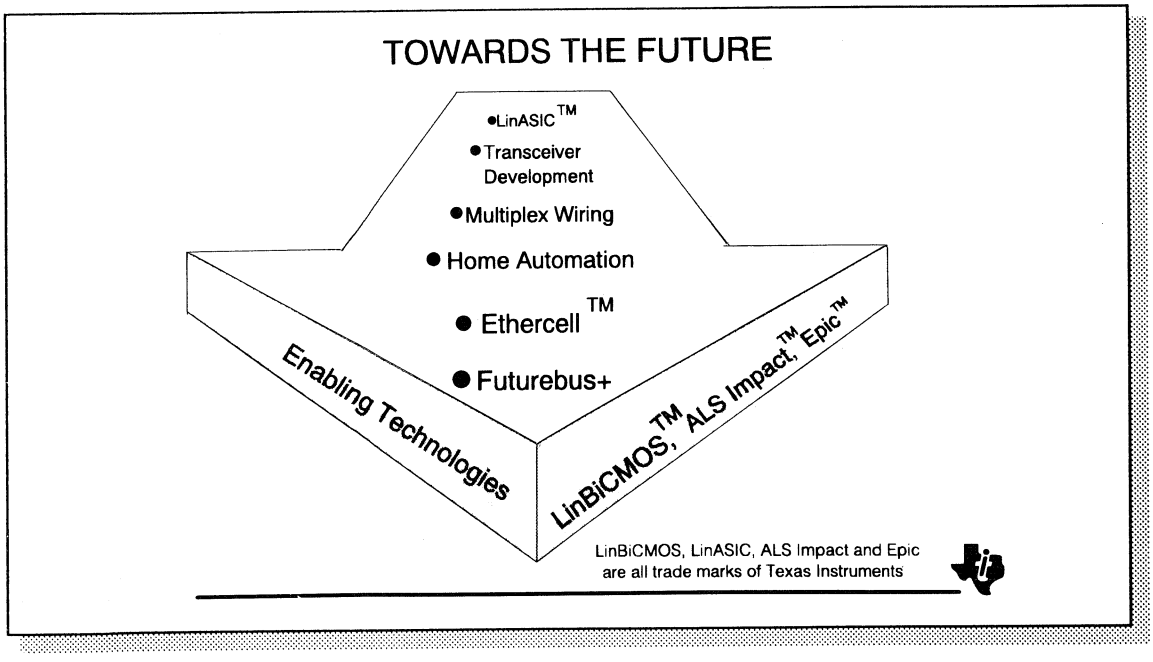


Figure 32 - Towards The Future

The products discussed in this book reflect only part of Texas Instruments' total data transmission product range. Their product developments extends well beyond simple EIA line drive/receive functions to the use of new technologies (giving high performance line drive/receive options) and to new product development for emerging markets. Such examples where TI is set to make significant contributions are in the fields of automotive multiplex wiring, home automation, futurebus+ and Ethernet™, in addition to their continuing use of LinASIC™ for high volume customer defined products.

While a detailed discussion of these product areas is beyond the scope of this text a global overview is given below. For further information on these subjects the reader is urged to contact their nearest TI office.

Automotive Multiplex Wiring

In addition to standard catalogue products, the SN65176 and SN65076, TI is currently developing line drive/receive products to support all major industry standards. These standards include the J1850 and CAN and VAN specifications. Of particular note are the LinBiCMOS developments for the J1850 standard, which in addition to the fully differential current mode line drivers/receivers contain over 300 gates of logic used to provide memory buffering giving message passing capability.

Ethernet™

TI's Data Transmission group entered the Ethernet arena ,with the SN75ALS085, as a result of a customer development programme. The SN75ALS085 was designed for the LAN Access Unit Interface (AUI) and comprises dual driver/receiver with loop-back control. The LAN AUI allows the number of connections made to the Ethernet cable (tap) to be increased from one to eight. The SN75ALS085 is an optimised device designed specifically for this function. The next generation devices currently in development use a cell based approach, termed Ethercell™, to develop a range of optimised transceiver devices for Ethernet. New developments include devices for Ethernet's twisted pair specification.

Home Automation

TI will continue with its Consumer Electronics Bus (CEBus) developments by producing both controller and modem functions complaint to the new CEBus specification (when finalised). In addition it is developing products for the Smarthouse™ specification.

Ethercell is a trade mark of Texas Instruments.

Notes

Futurebus+

Futurebus+, IEEE 896, is a high performance backplane standard which is under sponsorship from the IEEE.

The backplane is the primary interface between the CPU and option cards in the PC card frame. It forms the main communications highway for data, control, status and address information. It allows the CPU to address option memory, LAN adaptors, co-processors, disc controllers or server networks...etc.

Although there are many backplane standards currently available they fall short of in meeting the demands of todays high performance systems. Systems which use state of the art RISC architecture and employ multi caching techniques. For these reasons the IEEE 896 futurebus+ specification was developed, and has been the result of many years effort from academics, systems designers and semiconductor manufactures alike.

TI has played an active part in the definition of the futurebus+ standard and is well placed to introduce supporting products.

TI's futurebus+ chip-set developments will result in a family of devices that support the entire futurebus+ cost/performance spectrum, ranging from industrial computing platforms to supercomputers. A recently announced joint/development/alternate source agreement with Philips Components-Signetics will ensure standardised silicon for futurebus implementors all devices will be made available from both companies and fabricated using their own processes, thus providing industry with true alternate sources.

A further agreement between Force Computers, provides a systems integrators perspective to TI's chip-set development. Force a major VME product manufacture, and TI will jointly develop a cache optimised parallel protocol controller.

Product development comprises, a range of transceivers designed using BiCMOS and a range of controller chips. The transceivers will include 7-bit, 8-bit and 9-bit devices, with and without latches, and an arbitration contest transceiver. The controller developments will include parallel protocol controllers, arbitration controllers, packet data FIFO's and data path units.

LinASIC™

TI will continue with its leadership linear cell methodology to design customer defined products for high volume applications.

LinBiCMOS...The Last Word

The underlying trend in all these areas is the use of the merged analogue/bipolar and digital/ CMOS process- LinBiCMOS. This process has as been demonstrated many times and will enable TI to maintain its leading position as supplier of quality data transmission products.

Transmission Line Fundamentals

Transmission Line Fundamentals

Before studying the more practical considerations of implementing a digital data link, an understanding of the signals behaviour is needed. More specifically a method of identifying potential problem areas, and the ways in which to overcome them is necessary. By an appreciation of this first section the reader will be better placed to understand the limitations placed on digital data transmission systems.

System Careabouts

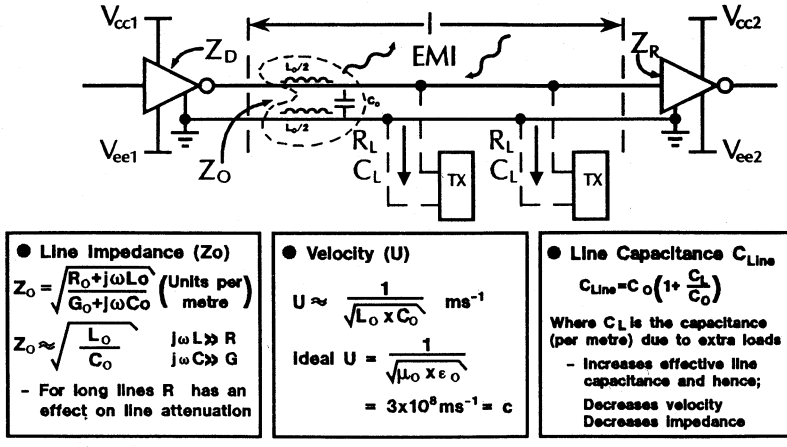


Figure 01 - System Careabouts

For identification and simplicity digital communication within a system can be divided into three distinct areas;

i) **Transmission of digital data between integrated circuits on the printed circuit board.**

ii) **The transfer of data between circuit boards via the system backplane.**

iii) **The transfer of data between separate equipments or peripherals over still longer distances, for example by using serial communication standards like EIA-232 or RS-485 links.**

Notes

In the first two instances, printed circuit board and backplane communications, data transfer usually takes place with TTL or CMOS logic level signals. Even so, the speed of the backplane system will be slower than that of the printed circuit system, simply because of the differences in electrical characteristics between the printed circuit track and backplane wiring. These differences in electrical characteristics become even more conspicuous when using high speed, long distance communication links such as the multipoint RS-485 standard.

At low data rates a cable can be regarded as a pure short circuit, and it can be assumed that the propagation delay of the signal along the cable is negligible and will not impact on the overall system performance. However as data rate and distance increase then the speed and shape of the data signal starts to be governed more by the electrical characteristics of the cable, ie its capacitance, inductance and resistance. This leads to a certain amount of degradation in the signal quality. Not only will a signal degrade due to the electrical properties of the cable, it also suffers degradation from external sources of interference. It is obvious therefore that these limitations should be comprehended into the design of a digital data communications link, after all a cable is not always "just a piece of wire".

As a final note, it should be emphasised that the problems encountered with digital signals on printed circuits and backplanes are exactly the same in nature as those encountered with the comparatively long distance systems that we are discussing here. In practice though, the digital design engineer is often better equipped to deal with the former class of problem.

Transmission Line Considerations

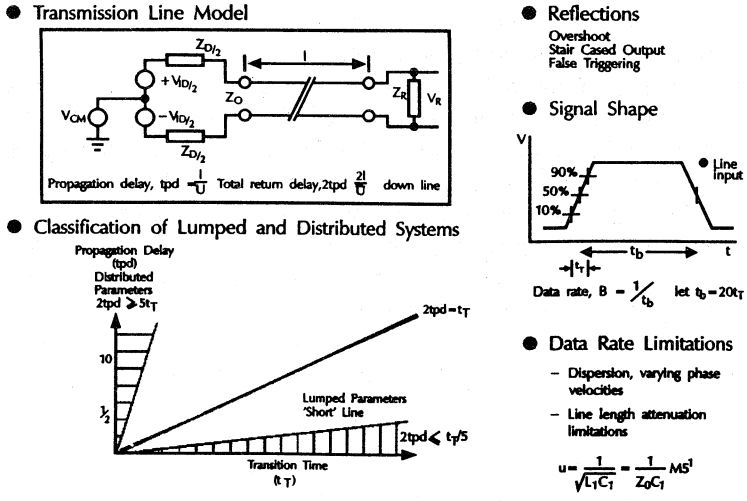


Figure 02 - Transmission Line Considerations

Having reviewed some of the key factors characterising a transmission line, the behaviour of the signal must now be considered. More specifically a method of identifying the class of data link must be made.

A digital data link can be classed in two modes; A transmission line (Distributed parameters) or short wire (lumped parameter model). A distributed parameter model models the connecting circuit in terms of distributed parameters (inductance, capacitance, resistance, conductance), rather than as an equivalent lumped load on the line. The transmission line can be considered in terms of an infinite number of small filter sections making up the line. The result is that a transmission line is said to have a characteristic impedance, Z_0, which is independent of distance along the line and represents the voltage and current relationship for a waterfront at any point as it travels along the line.

The transmission line will always consist of two conductors. The current will flow in opposite directions in each of the conductors. In the single ended case, one of these conductors is the ground wire.

Notes

The speed that a pulse travels at along a transmission line approaches that of the speed of light. The limit to the actual speed will very much depend on the type of cable used.

All cables can be thought of as transmission lines; but the term, transmission line, is used with differing meanings. If the signal starts to change at the transmitter output at one end of the line, the effect of this change will eventually be seen at the other end of the line. A reflection of the signal will occur, which will eventually return back to the transmitter terminals. If this happens before the original transmitted signal has risen to its peak value then the line will normally be treated as a lumped parameter system rather than as a true transmission line. This is because the line itself does not greatly influence the performance of the system. A general rule of thumb for determining if a system should be treated as a true transmission line can be formulated. If the risetime , t_T, of the signal is much less than the round trip propagation delay, $2t_{pd}$, of the signal from transmitter to receiver and back to transmitter, then the cable can be treated as a transmission line and not as a lumped parameter model. A better model is given by allowing 10 one way propagation delays, t_{pd}, to occur during the transition edge time.

When the cable is operating like a transmission line, extra loads in the form of transmitters and receivers can be added , providing that they do not cause too great a shunting effect on the line. These extra loads, if they are evenly distributed along the line, can be treated as an extra distributed capacitance along the line adding to the effect of the line capacitance and inductance. The extra devices will decrease the line impedance and reduce the speed of the signal along the line.

In the case of the lumped parameter model the line to represent a pure fixed load to the transmitter device. For example, the capacitance of the line will be modelled as a fixed value which effectively limits the output voltage slew rate of a transmitter device that can supply a finite amount of current to the line.

Transmission Line Reflections

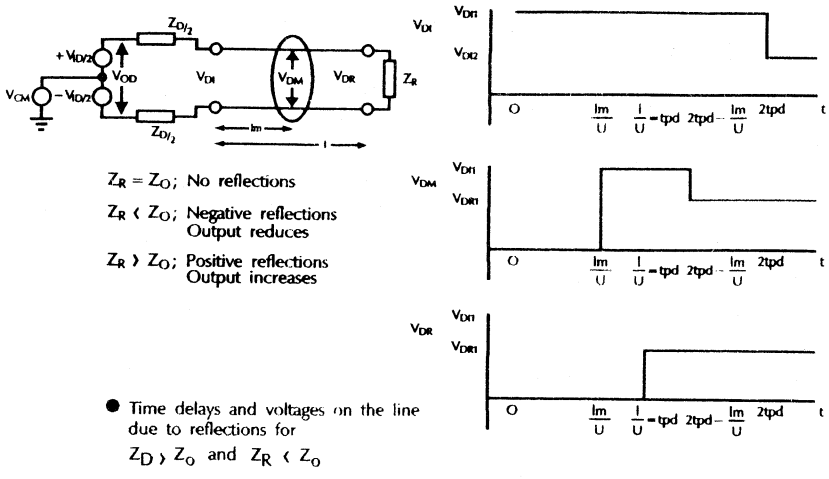


Figure 03 - Transmission Line Reflections

Imagine a driver circuit driving the line. When the driver output voltage changes state, the driver appears to see the effective characteristic impedance of the line, Z_O. This will cause the voltage at the output of the driver circuit to reduce as a result of the potential divider action formed by Z_O and the driver circuit output impedance, Z_D.

It is useful to consider that at any point along the line, the source impedance will appear as Z_O, and the load impedance will also appear as Z_O. This gives the impression that the line is being driven by a voltage source, V_{IE}, of twice the magnitude of the line voltage.

If when the signal reaches the receiving end of the line it sees a terminating impedance equal to the impedance of the line that it is already travelling on (Z_O), it will interpret this as a continuation of the line. The voltage on the line will not alter and the current flowing along the line will flow through the termination resistor and back to the driver via either ground or the other line in the system. Operation of the circuit as just described would result in optimum data transmission efficiency, with little or no signal reflections. However, circuit operation in the real world is not always so perfect.

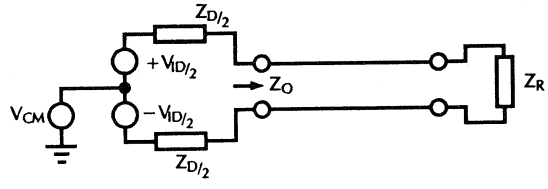
Notes

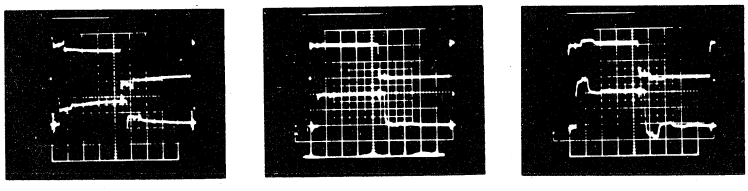
If the termination impedance dis-similar to the characteristic impedance of the line itself, the voltage at the termination point will alter. The voltage at the termination point is dependent on the relative size of the termination impedance to the line impedance. If the termination impedance is higher than the line impedance, the line voltage will increase causing a positive voltage reflection of the signal. When the termination impedance is lower than the line impedance, the line voltage will decrease leading to a negative reflection. The same effect will occur at the driver output terminals due to impedance mismatches between driver and line..

Reflections at each end of the line will eventually settle and leave a constant d.c. voltage on the line. The value of this voltage is equal to the ideal open circuit output voltage multiplied by the termination impedance divided by the sum of the driver output impedance and termination impedance.

Reflections as described can cause problems when driving lines at high frequencies. False triggering of the receiver can occur, and the repeated signal reflections mean that signal waveshapes are distorted.

Typical Reflections Due to Mismatching





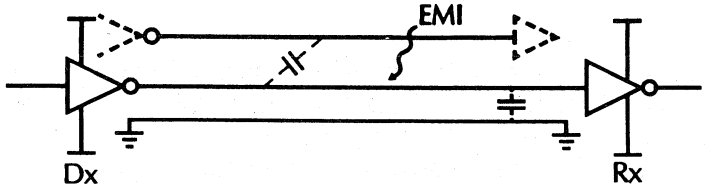
$Z_R < Z_O$ $Z_R = Z_O$ $Z_R > Z_O$

Figure 04 - Typical Reflections Due to Mismatching

The accompanying graphs prove the theory developed by comparing the signal quality between correctly terminated and incorrectly terminated lines. In all cases the top trace represents the output from the driver as presented to the line, while the bottom trace is the line input to the receiver.

For ZR < ZO it can be clearly seen that the effect of the reflection voltage (top trace) is to reduced the incident step voltage. Similarly the reflection voltage has an effect for ZR > ZO, only this time the reflection voltage causes the termination voltage to be greater than the incident voltage. The ideal condition, ZR = ZO, produces a termination voltage relatively free from reflection voltages, and results in maximum power being delivered from the driver to receiver.

Single Ended Line Considerations



System	Advantages	Disadvantages
Single–ended eg. RS–232 V.28 RS–423 V.10	● Low cost ● Simple	● Susceptible to – Noise & crosstalk – Ground shifts ● low data rates ● short lengths
Differential eg. RS–422 V.11 RS–485	● Noise & cross talk rejection ● Ground shift rejection ● higher dates ● longer line lengths	● More signal wires ● moderate – high cost ● More Complex

Figure 05 - Single Ended Line Considerations

Single ended data transmission systems consist of a signal line on which data is sent down and a ground line through which the current returns. A direct result of this is that the ground line forms part of the transmission line, which can be of benefit in some circumstances but not in others.

One of the major benefits, and most obvious, is that a single ended system is the cheapest solution in terms of cabling costs. In general terms it requires only half the cable of a differential system. It is also relatively simple to install and operate.

The main disadvantage of the single ended solution is its poor noise immunity. Because the ground wire forms part of the system, any transient voltage or shifts in voltage potential may be induced (from nearby high frequency logic or high current power circuits), leading to signal degradation ultimately leading to false receiver triggering. For example, a shift in the ground potential at the receiver end of the system can lead to an apparent change in the input switching threshold of the receiver device, thus increasing susceptibility to noise.

Notes

Another common problem area with single ended systems is the effect of crosstalk between adjacent signal lines and the coupling into the line of noise from other sources. The line is both inductive and capacitive so will be susceptible to both electrostatic and magnetic coupling.

The crosstalk pick-up in the line is related to the effective coupling capacitance and the terminating impedance of the line. The higher the impedance of the termination circuit, the greater the induced voltage due to crosstalk. The induced voltage due to crosstalk also increases as the frequency or edge speed of the crosstalk signal increases.

These problems will normally limit the distance and speed of reliable operation for a single ended link.

The induced noise can be reduced by;

i) Limiting the slew-rate of signals so that they do not cause crosstalk to be induced onto other lines

ii) Limiting the line length.

iii) Shielding the signal conductor.

While the system noise could be reduced by:-

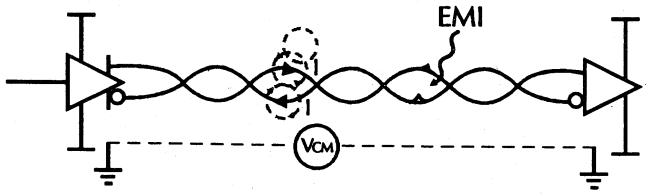
i) Isolating the signal ground from power conductors. (E.g. keep signal grounds separated as far as possible from power grounds.)

ii) Ground wires should be as low as impedance as possible.

iii) Use star ground system configurations

Some of these techniques are used in systems such as EIA--232 and the forthcoming Futurebus+ backplane system, which limit the slew-rate of signals by capacitive means (EIA-232) and by intentional generation of trapezoidal signals (Futurebus+).

Differential Line Considerations



System	Advantages	Disadvantages
Differential RS–422 V.11 Rs–485	● Noise & cross talk rejection ● Ground shift rejection ● Higher data rates ● longer line lengths	● More signal wires ● Moderate – high cost ● More complex
Single–ended RS–232 V.28 RS–423 V.10	● Low cost ● Simple	● Susceptible to – Noise & crosstalk – Ground shifts ● Low data rates ● low line lengths

Figure 06 - Differential Line Considerations

A differential communication system involves the use of two signal carrying wires between transmitter and receiver, such that the signal current flows in opposite directions in each wire. The net effect of doing this is that the receiver is only concerned with the *difference* in voltage between the two wires. The absolute value of the d.c common mode voltage of the two wires is not important. In practice, transmitters and receivers have a finite common mode voltage range in which they can operate.

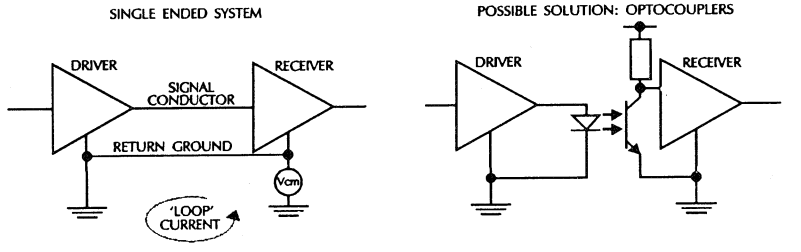
The use of a differential communications interface allows transmission of higher data rates over longer distances to be accomplished. This is because the effects of external noise sources and crosstalk effects are much less pronounced on the data signal. Any external noise source coupling onto the differential lines will appear as an extra common mode voltage which the receiver is insensitive to. The difference between the signal levels on the two lines will therefore remain the same. By the same argument, a change in the local ground potential at one end of the line will appear as just another change in the common mode

Notes

voltage level of the signals. The differential output to the line will also provide a doubling of the driver's single-ended output signal. Twisted pair cable is commonly used for differential communications since its twisted nature tends to cause cancellation of the magnetic fields generated by the current flowing through each wire, thus reducing the effective inductance of the pair.

The main disadvantage of a differential system lies in the fact that two cables are required for each communication link. This increases system cost, but provides superior performance when data is to be transmitted at high rates over a long distance.

Serial Grounding Schemes



1. Ground loop current flows due to apparent difference in ground potential (Vcm).
2. Ground loop current flows due to external interference.
3. Not suitable for long distance or noisy environments.

1. Optocoupler electrically isolates driver from receiver. Only 'signal' is transmitted.
2. Optocouplers capable of operation upto 10 Mbits/sec

Figure 07 Serial Grounding Schemes

Setting the Scene

Grounding should be considered early in the design phase of a party line system, there now follows a brief discussion of the grounding considerations.

A 'ground' is an assumed arbitrary point of zero potential, and a ground connection is a tie to a point as close as possible to a ground potential. The objective of any grounding technique is to provide a path to earth of as lo as resistance or impedance as possible. The reason for this is quite clear, the flow of current causes a voltage drop that is directly proportional to the resistance of the path to ground. Any resistance that results in unwanted difference of potential is the source of coupling to other circuits. The above may seem obvious but it emphasises the importance of principles like single point grounding in high performance linear circuits and the need to separate 'noisy' digital grounds from 'quiet' analogue grounds in a circuit. Of course the analogue and digital grounds will have to be combined at some point in the circuit, the terminals or at the zero volt bus bar for example.

Single Ended Transmission

For single ended data transmission it should be possible to transmit the data along a signal conductor to the receiver and then return the current to the zero volt potential. In ideal circumstances, the 0V connection at the driver and receiver devices should be at the same potential. However, in long line applications, what happens in practice is that there is an apparent change in local ground or 0V potential at one end of the system. This is represented in the figure by Vcm in series with the receiver ground. Vcm will cause the incoming signal to appear to have a reduced common mode voltage (assuming Vcm is positive). Vcm can reach values of several volts which could cause the link to fail. For example, if the receiver input switching threshold was set at 1V and Vcm was 5V, then the incoming signal would need to have an effective value of 6V just reach the receiver's input switching threshold.

An obvious way to prevent the situation just described is to ensure that both receiver and driver have a common ground reference. This can easily be achieved by connecting a signal return/common ground reference. However,doing this can introduce another problem known as a 'ground loop' or 'earth loop'. This is formed because current is now free to flow as shown in the loop made up from the signal return wire and the earth path. Since Vcm is in this loop, current flows. If the loop encompasses many pieces of equipment, then the net results is that each equipment ground (or I.C. ground) will have a different potential (something to be avoided).

In addition to the ground loop current that flows due to differing ground potentials, inductive coupling of signals external to the circuit into the ground loop is also another area of concern. The ground loop is prone to this
effect since it forms a loop of large area and low impedance and is therefore highly inductive. In low frequency voice grade circuits, the interference is commonly found in the form of a.c. hum picked up from nearby power supplies.

Therefore, single ended communication is not recommended for use in noisy environments due to interfacing coupling or for use over long distances if there is a possibility of ground shift.

A more complete solution to the problem of ground shift and interference involves the use of opto-couplers in order to electrically isolate the output of the driver from the receiver input. This is shown in general form in the figure. Since there is no electrical connection between driver and receiver, then no earth loop is formed. Modern opto-couplers also have extremely good rejection capability to high frequency common mode signals; as high as 10kV/ms and can operate at up to 10Mbaud (HCPL2601 from TI).

Notes

Differential Grounding Schemes

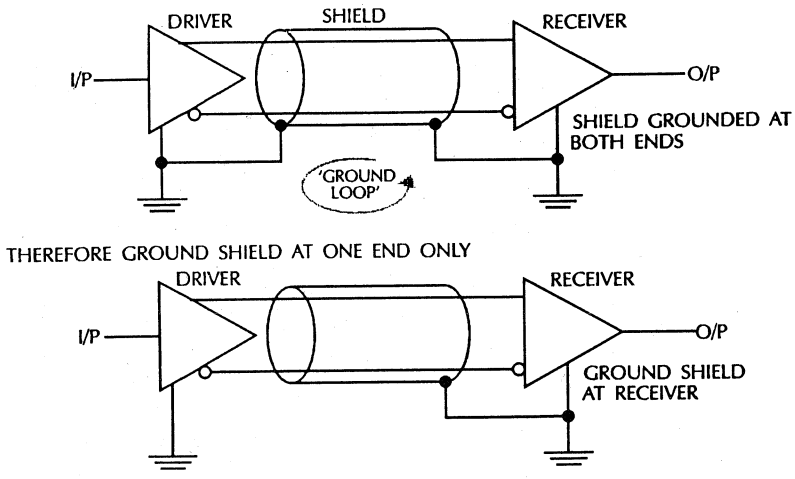


Figure 08 - Differential Grounding Schemes

This figure illustrates a very simple guide-line for dealing shield grounding in differential systems. If the shield is grounded at both driver and receiver ends, then a possible ground loop path exists which can lead to problems already described.

The answer is to ground the shield only at the receiver end. This ensures that a ground loop current cannot flow. The shield therefore acts as a low impedance path to ground for externally interfering signals.

Driver Configurations

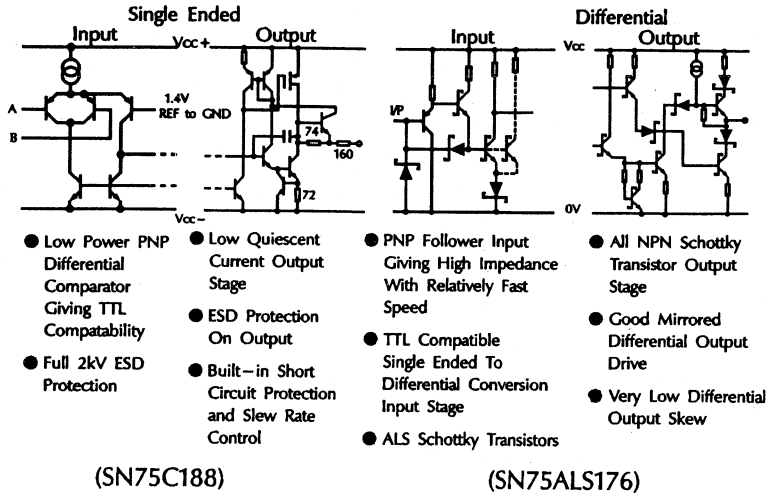


Figure 09 - Driver Configurations

The two basic formats for data transmission systems; single ended and differential, have differing current and voltage requirements. As a consequence there are differences in the internal structures of the semiconductor integrated circuits that are used to drive lines in each of the two formats. The biggest difference lies in the design of the output stage circuitry of the devices.

Until recently, the semiconductor technologies used to manufacture line interface circuit devices have all been based upon those technologies and processes used to build digital logic circuits. This resulted in circuits having mainly bipolar NPN structures. For example the change from ordinary bipolar to low power schottky (LS) advanced low power schottky (ALS) technologies in digital logic devices, was closely followed in line circuit devices.

Notes

In recent years though, there has been a change in the digital logic field towards device structures based upon CMOS processes. CMOS offers the obvious attractions of low quiescent power consumption and operating speed comparable to that of many bipolar technologies. The same change in technology for line circuits has not been so fast. One of the primary reasons for this is the need to make output transistor stages very large in CMOS technology to enable them to source the required high currents (as much as 250 mA). The input capacitance of these large CMOS stages also require much higher drive currents from the bias circuits. At high frequencies of operation CMOS line circuits therefore lose some of their attraction because bias currents become so high. It is also difficult to build CMOS devices that could withstand the relatively high voltage levels used by some slower, older line interfaces, for example EIA-232.

The most promising route forward in technology for line interface devices would appear to be through the use of a BiCMOS technology. Such progress has again already been made in the digital logic field. BiCMOS technology combines the speed and high voltage capability of bipolar processes with the low supply currents and high input impedances of a CMOS process.

Consideration of the circuit schematic for the input stage of most line driver circuits will show them to be TTL compatible. The SN75C188 quad EIA-232 driver and SN75ALS176 RS485 transceiver demonstrate this. The inputs of both devices feature a reversed bias diode and resistor to the positive supply and an effective two forward diode drops to ground. This is a similar configuration to that found in a standard TTL gate and results in the 0.8V and 2.0V TTL threshold levels. However, the SN75C188 has been designed for dual rail applications and so shifts the 0-5 V input voltage to the +/-12V output voltage range. Since it is designed to drive differential lines, the SN75ALS176 includes a single to differential converter stage consisting of a latch with an extra invertor structure.

Single ended line drivers are normally used to transmit data at lower speeds and require less output current drive capability They are therefore good candidates for implementing in a lower power process technology. An new generation of EIA-232 devices built using a BiMOS process has emerged to make low power consumption a reality. The new Generation of low power BiMOS devices includes quad drivers and receivers (SN75C188/198/189), both triple and quad combined driver/receivers (SN75C1406/1154) and a mixed three channel driver and five channel receiver (SN75C185).

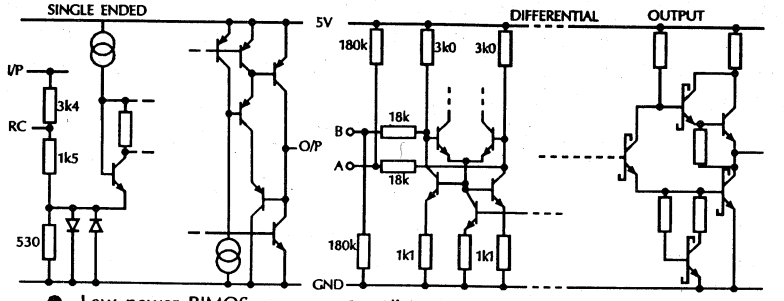
The new BiMOS technology devices offer more advantages than just reduction in power consumption; slew rate limitation of the EIA-232 signal to 30V/us is carried out on-chip. This obviates the need for external capacitors.

Another feature which has been introduced to single ended systems such as EIA-232, even though they were never intended to be used in such a manner, is the capability to disable the output from the line. This is possible when using devices such as the SN75C198, LT1030 or LT1080. This has a major effect in saving the standing current that normally flows in the EIA-232 line.

High speed differential output drivers, the SN75ALS176 for example, use an all schottky npn totem-pole output stage. This increases the output switching speed performance over technologies using pnp transistors in critical signal paths. The advanced low power schottky technology (ALS) also substantially reduces supply current consumption over standard LS npn structured devices (SN75176).

As the data rates demanded from systems increase, switching speeds in differential driver outputs also increase. However, since the outputs are complementary in nature, it is essential that the two outputs change state at the same time. Totally simultaneous switching when driving a long cable is almost impossible to achieve, but the excellent signal skew specifications for 'ALS devices make them suitable for the most demanding applications.

Receiver Configurations



- Low power BIMOS technology
- Low voltage threshold for bipolar to unipolar logic levels
- Built – in filter

(SN75C189)

- All NPN input and output stages
- High speed schottky NPN output stage
- High precision differential input stage
- High input impedance
- ± 7V outside supply rail common mode range

(SN75ALS176)

Figure 10 - Receiver Configurations

The design of a line receiver circuit is also dependent upon the type of data transmission system it is ended to work in. The key operational parameters to be specified include:

Notes

i) **Differential or single ended inputs.**

ii) **Input signal switching threshold.**

iii) **Input signal common mode range.**

iv) **Speed/power requirements.**

The design of a single ended receiver is usually simpler than that of its differential counterpart. The signal input stage to a single ended receiver is similar in function to a voltage comparator circuit. The input signal is compared to an internal reference and the output switched accordingly.

New generation EIA-232 receivers, constructed using BiMOS technology, have been designed to meet new systems' power saving requirements. They also include line noise rejection filter circuits in their design, providing further system integration. The filters incorporated into the receiver are capable of rejecting voltage noise and glitches on the line which are less than 1us duration. This feature saves on board space and reduces external component cost. The output stage of the SN75C189 receiver circuit has been designed using a low power common emitter circuit.

Differential receiver circuits have to operate in the presence of large common mode d.c. voltages at the input terminals, while still maintaining a good differential accuracy. This is achieved by making the heart of the receiver a high speed differential amplifier. The common mode range of this amplifier is small, so as to maintain its gain accuracy and speed. However, in order to cope with the large common mode input voltages, from -7V to +12V, the input circuitry incorporates a potential divider network that reduces the effective common mode input voltage while still maintaining a high input impedance. The network clamps the common mode part of the signal to a constant level suitable to the differential amplifier stage. The same resistive network also provides the large minimum input impedance required to meet RS-485 requirements.

The output stage of these receivers uses an ALS npn transistor network which provides the high speeds demanded by the RS-485 system, while maintaining a good power consumption at these speeds

The ANSI Small Computer Systems Interface (Tutorial)

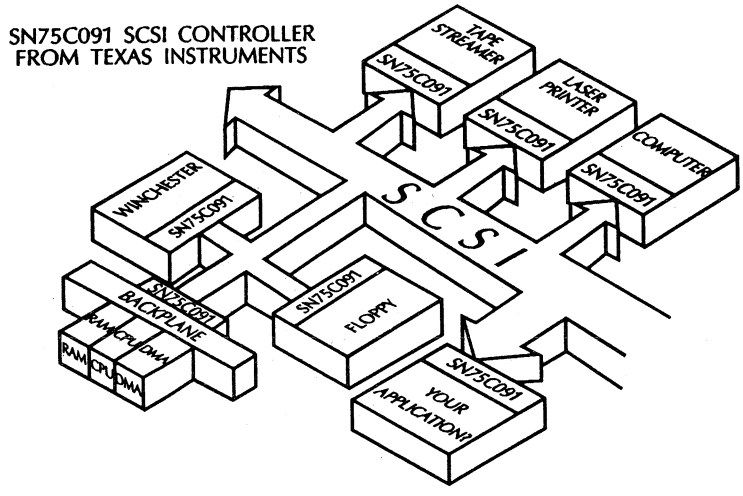


Figure 01 - Small Computer Systems Interface Solutions

SCSI interface can be used to connect computers, disk drives, optical storage devices, laser printers, scanners, tape drives etc. together using a common bus system. Moreover the standard specifies the mechanical, electrical and functional requirements for a small computer input/output bus interface and command sets for intelligent peripheral device types, particularly storage devices commonly used with small computers.

The SCSI Advantage

SCSI offers advantages to both the equipment user and the equipment vendor. Users benefit from increased system performance and a wider choice of compatible peripherals available 'off the shelf, which are not system specific. Vendors benefit by not having to design individual interfaces for each different disk drive or peripheral that they supply. Standardisation between manufacturers increases the size of the potential market for the product.

SCSI is capable of supporting communication between multiple computers as well as computer to disk drive for example. Also disk to disk data transfers can take place which execute completely independently from computers on the bus. The bus is therefore 'intelligent'. This is one of the prime reasons for an intelligent I/O bus, like SCSI, to off-load some of the more mundane but time intensive I/O cycles from the host CPU.

A Brief History of SCSI

SCSI has been an official ANSI standard since 1986 (X3.131-1986), however its roots go back much earlier to the IBM mainframes of the early 1960's. (*ANSI stands for American National Standards Institute, which has been responsible for such international standards as*

the ASCII 7-bit data code.). The early IBM 360's had a byte-wide I/O bus known as the *block multiplexer channel* which had the capability to communicate with several peripherals at once. The IBM bus, also known as the *OEM channel* , soon became the defacto interface standard for peripheral manufactures. However it was realised that this was fast giving IBM an unfair competitive advantage over other computer manufacturers. Consequently in the early 1980's ANSI began work on a non-propriety bus called IPI , Intelligent Peripheral Interface. This was in fact a superset of IBMs' OEM channel. Concurrent with this development Shugart Associates (a disk drive manufacturer) were working on a flexible I/O interface. This interface known as the SASI (Shugart Associates System Interface) soon became adopted by many major OEM's, leading to its natural adoption by ANSI. This fitted well into ANSI's portfolio who now had a high performance I/O standard in the guise of IPI and a lower performance standard in SCSI. However with the advent of SCSI-2 the difference between IPI and SCSI has diminished.

SCSI Specification

SCSI is implemented on a 50 way bus made up of data-bits, parity-bit, ground lines, power line and control lines. The data lines are used to transfer data, command status and message information. While the control lines provide the necessary sequencing and handshaking information to control the flow of information. The number of pins used depends upon whether differential or single ended SCSI is being implemented, SCSI supports both. Differential SCSI offers the highest noise immunity and allows for transmission up to 25 metres, differential SCSI conforms to the EIA-RS485 specification and is generally recommended for cabinet to cabinet links. Differential SCSI uses all 50 lines where many of the odd-numbered pins form the differential signals with the corresponding even-numbered pins. Single ended SCSI is less immune to noise and consequently is used for shorter distances, up to 6 metres, this usually limits it to inter-cabinet communications. In a single ended system all unused odd-numbered pins are grounded (except pin 25) to provide additional shielding between the signal lines, see figure 02 for details of SCSI pin assignments.

Notes

SIGNAL	PIN NUMBER	PIN NUMBER	SIGNAL
SHIELD GROUND	1	2	GROUND
+DB(0)	3	4	-DB(0)
+DB(1)	5	6	-DB(1)
+DB(2)	7	8	-DB(2)
+DB(3)	9	10	-DB(3)
+DB(4)	11	12	-DB(4)
+DB(5)	13	14	-DB(5)
+DB(6)	15	16	-DB(6)
+DB(7)	17	18	-DB(7)
+DB(P)	19	20	-DB(P)
DIFFSENS	21	22	GROUND
GROUND	23	24	GROUND
TERMPWR	25	26	TERMPWR
GROUND	27	28	GROUND
+ATN	29	30	-ATN
GROUND	31	32	GROUND
+BSY	33	34	-BSY
+ACK	35	36	-ACK
+RST	37	38	-RST
+MSG	39	40	-MSG
+SEL	41	42	-SEL
+C/D	43	44	-C/D
+REQ	45	46	-REQ
+I/O	47	48	-I/O
GROUND	49	50	GROUND

Figure 02 - Differential SCSI Pin Assignments

As well as providing for differential or single ended communication the SCSI bus can operate in either asynchronous or synchronous mode. Asynchronous mode allows transfers of up to 1.5 Mbytes/sec whilst in synchronous mode transfer rates of up to 4 Mbytes/sec are permitted.

How Many Peripherals ?

SCSI can support up to eight peripherals (including the master). Each peripheral can in turn support a further 8 logical units, which can drive up to 256 logical subunits. Thus a total of 14,000 peripherals can be supported on one SCSI bus if there is one host and each peripheral is a logical subunit.

Texas Instruments supports the SCSI standard with the *SN75C091A* controller chip. Each peripheral in a SCSI system is fitted with a SCSI controller which is responsible for passing information from the SCSI bus across to the host µP bus or control electronics in the peripheral. The SCSI controller ensures that all data transfers and bus communications take place as per the SCSI protocol.

Typical SN75C091A System Configuration

- On-Chip Byte Stacking Logic
- Seperate Host & DMA Data Path
- 32 Byte Transmit & Receive FIFOs
- 8 High Level Multiphase Commands
- 8 PIN PLCC or ASIC Macrocell
- Low Power CMOS Technology

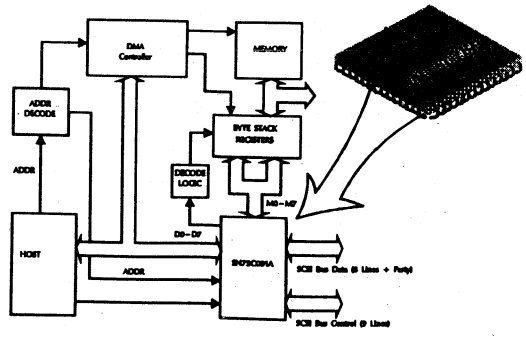


Figure 03 - Typical SN75C091A System Configuration

Before a typical SCSI implementation can be discussed it is necessary to have a basic understanding of the SCSI signal lines and the bus phases. This is best attempted by dividing the standard up into its two main areas, the physical layer and the logical layer.

Physical Layer

The physical layer sets a standard for the interconnecting of the SCSI devices. All devices must be daisy chained together using a common 50 way cable, since the signal is half duplex both ends of the bus must be correctly terminated. Differential and single ended systems may not be used on the same bus.

Logical Layer

This contains information on the protocol and timing aspects of the SCSI interface. The SCSI bus operates in a series of distinct transactions , known as bus phases, at any one time the SCSI bus must be in one of these states. The phases determine the direction and content of the data lines. The eight possible phases are; *Bus free, arbitration, selection, reselection, command, data, status and message.* Arbitration is optional although it is implemented by most controllers, the SN75C091A for example. The sequencing and handshake information to control the transition between phases is handled by the 9 control signals,

Notes

The phase diagram in figure 04 shows the relationship between these phases. The SCSI has no bus master, ie the usual master/slave aruguement is not true as in theory each peripheral as well as host controllers can act as either initiators or targets.

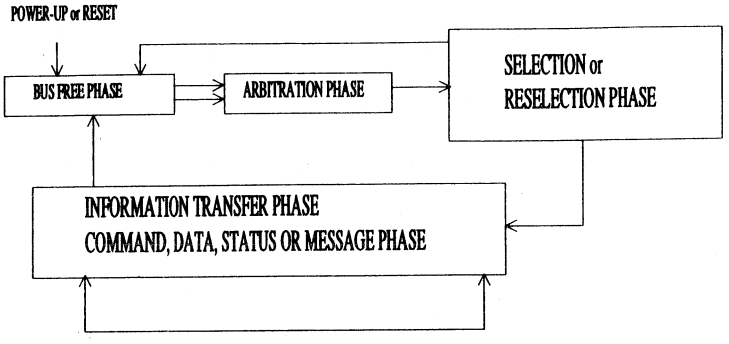


Figure 04 - SCSI Bus Phases

BusFree. All sequences begin in the bus free phase, this is the only phase in which the BSY signal is not inserted and indicates that no modules have control of the bus.

Arbitration. In this phase all potential masters on the bus compete for bus ownership. The phase begins when an initiator attempts to gain control of the bus by asserting its BSY signal and sets its data bits to correspond with its SCSI ID. The highest ID wins and the others back off permitting the now bus master to continue his transaction by asserting the SEL signal .

Selection / reselection. The arbitration phase is followed by the *selection* or *reselection* phase. Here the initiator selects a target by placing the targets ID and its own ID on the bus (while SEL is asserted) and releases BSY. If the target is valid it responds by asserting BSY allowing the initiator to release SEL.

Command phase is now entered which is now controlled by the target. The reselection phase occurs when a target wins the arbitration and re-establishes contact with an initiator that had previously sent it a command. The control signals used in this transaction are the C/D , I/O, REQ, ACK and MSG, the combination of signals is best explained by consideration of figure 05.

MSG	SIGNAL C/D	I/O	PHASE NAME	DESCRIPTION
0	0	0	DATA OUT	Initiator sends data to target
0	0	1	DATA IN	Target sends data to initiator
0	1	0	COMMAND	Initiator sends status to initiator
0	1	1	STATUS	Target sends status to initiator
1	0	X		(Reserved)
1	1	0	MESSAGE OUT	Initiator sends message to target
1	1	1	MESSAGE IN	Target sends message to initiator

Figure 05 - Information transfer phases and SCSI control signals

In the command phase the target requests a command from the initiator, either data in, data out, status, message in or message out. The data-in and data-out phases are self explanatory, in the status phase the target sends a status byte indicating the success or failure of a command. Message in and message out are used to pass messages between the communicating modules. Typical messages could include; command complete or initiator detected error.

Thorough discussion of the SCSI transactions is beyond the scope of this seminar. However there are numerous articles, data sheets and the standard itself which provide valuable sources of information.

The block diagram demonstrates how a typical SCSI bus can be implemented using TI's SN75C091A. This particular implementation uses separate 091 DMA port and 091 host bus port. Whilst separate DMA and host ports are not always required they are a necessary feature for high speed transactions. For example whilst the DMA could be actively transferring data the host port could be used for conveying status information to the host. The

Notes

diagram does not show all of the chip connections. For instance, DMA request lines are not shown. (This simplifies the diagram.) Other key features of the SN75C091A are as follows;

- **On-chip byte stacking logic for easier interfacing to 16,24,32 bit host bus.**
- **Separate data paths for host bus and DMA bus.**
- **32 byte deep transmit and receive FIFOs with parity bit.**
- **8 high level multi-phase commands, minimizes processor interrupts.**
- **68 pin PLCC package or ASIC macrocell.**
- **Low power CMOS technology.**

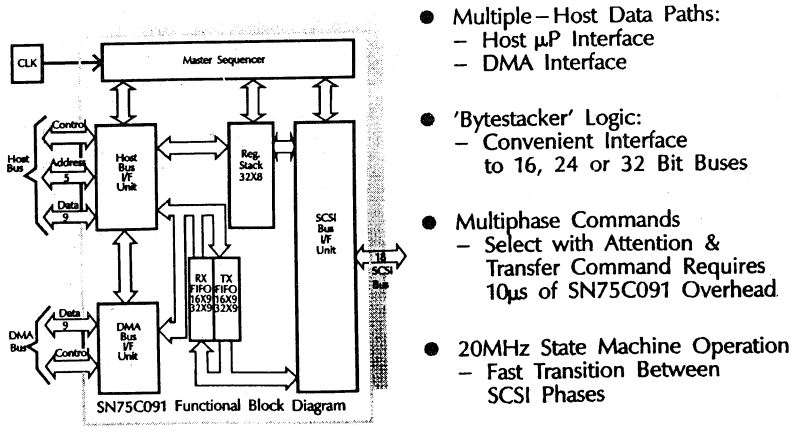


Figure 06 - SN75C091A SCSI Block Diagram

This figure shows the internal architecture of the SN75C091A and serves to highlight several key features.

- **Separate interface ports for host µP data bus and host DMA bus.** Separate data ports are not always required but in a high speed system the DMA port could be transferring data continuously, whilst at the same time the host µP could be interrogating the SN75C091A controller for status information.
- **On-chip 'byte stacker' logic.** This is a novel feature that is designed to make it easier to interface to host backplanes with 16, 24 or 32 bit wide buses. The SN75C091A actually generates the decoding signals necessary to control external latches that are used to multiplex the 16 , 24 or 32 bit host bus down to the 8 bit needed by the SN75C091A.
- **Multi-phase commands.** For example the SN75C091A can complete a select with attention and transfer command within 10 µs.

A comprehensive set of 'multi-phase' commands exist: Commands are passed across to the SCSI command register from the peripheral driver software resident in the host system. These commands are of two types; interrupting & non-interrupting. As their names imply, they differ in whether or not an interrupt is generated to the host to indicate completion of the command. Non-interrupting commands complete within a few clock cycles. Interrupting commands take from ten to several thousand clock cycles. The interrupting commands are further divided into two subsets, single phase & multi-phase commands. Single phase commands generally only execute one (or more) SCSI bus management phase or one info phase eg. arbitration & selection, data transfer phase or send command phase. An interrupt is generated at the completion of the command.

The multi-phase commands usually include at least one information transfer phase and one or more bus management phase. They can therefore be thought of as high level commands that group together several smaller commands into one instruction.Interrupts are handled internally to the SN75091A during execution of the multi-phase commands. This reduces the overhead of the host processor. For example, the multi-phase command 'select with attention & transfer, is a single command that represents a very common SCSI sequence ie. bus arbitration, target selection, send ID message, send SCSI command, send or receive data, receive status, and receive a command complete message.This command only requires a total of 10 μs of SN75C091A processing time (assuming an infinitely fast target response). This is due to the fast state machine design which operates at 20 MHz. Many competition parts use processor type structures which have to clock through their SCSI instructions at a slower pace.

Notes

Single Ended to Differential SCSI

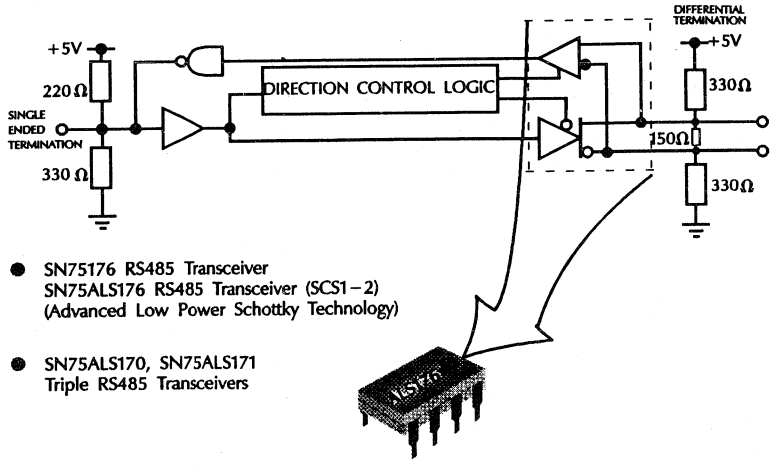


Figure 07 - Single Ended to Differential SCSI

As briefly mentioned earlier, differential SCSI is often desirable for driving longer line lengths (ie cabinet to cabinet) or where noise interference is a potential problem. Unfortunately most controllers only have single ended drive capability, this figure shows the basis of a single ended to differential output converter.

The single ended output is used to drive the TTL compatible inputs of the SN75ALS176. Direction control can be implemented using PAL's which control the driver and receiver pins on the SN75ALS176. The diagram also shows the single ended and differential line terminating techniques.

Most SCSI controllers for single ended implementation usually incorporate the required 48mA drivers on-chip while those designed exclusively for differential bus operation (without 48mA drivers) require an external differential line interface. In either case the range of Advanced Low power Schottky devices from TI are ideal for this interface.

The advanced low power schottky devices feature low power and high speed capability making them ideal for SCSI operation. The SN75ALS176 is a single transceiver housed in an 8-pin package, with a maximum data rate capability of 37 Mbaud. The SN75ALS170 and SN75ALS171 are triple versions with different enabling schemes allowing for half duplex and full duplex operation.

Notes

Data Transmission Trouble Shooting Guide

PROBLEM	PROBABLE CAUSE (S)	CORRECTIVE ACTION(S)
1. Damage to line receivers	a) common-mode noise b) differential noise	a) eliminate overstress voltage or current b) change to wider Vcm line receiver
2. Damage to line drivers	a) common-mode noise	a) eliminate overstress voltage or current
3. Data corrupted after establishing connection	a) transient noise	a) error detect and resend data b) add transient noise immunity
4. Failing EM emission requirements	a) common-mode noise	a) add common-mode noise immunity b) eliminate source of noise
5. Damage to terminating resistors	a) transient noise b) insufficient power ratings	a) add protection circuitry b) derate power rating by 50%
6. Data corrupted when adding or removing nodes to bus	a) power up/down "glitch" b) low bus impedance with power off	a) use line drivers with power up/down glitch-free circuitry b) use line drivers specified for high impedance with VCC=0
7. Crosstalk between adjacent cables in bundle	a) capacitive coupling	a) use balanced (differential) twisted pair interface b) add individual shields c) reduce driver output slew rate d) reduce driver output voltage swing
8. Interface IC overheats	a) load impedance too low b) bus contention	a) remove extra terminating resistors b) use higher Zo cable c) fix arbitration software
9. Impedance mismatches	a) no impedance matching resistor at cable end(s) b) long stub lengths c) nonuniform twisting of cable d) wrong value terminating resistor for cable being used	a) terminate cable with resistor equal to cable Zo b) shorten stubs off of main data line (daisy chain) c) use controlled impedance data cable d) lower data transmission rate or distance
10. Differential noise	a) signal wires not twisted b) current flowing through shield c) nonmonotonic driver output	a) used twisted signal cable b) terminate shield at one end only

PROBLEM	PROBABLE CAUSE(S)	CORRECTIVE ACTION(S)
11. Common-mode noise	a) capacitive coupling to outside world b) ground loops c) asymmetric driver outputs	a) add over-all shield b) eliminate ground loops c) add shields to each signal pair d) add protection circuit to data line e) transformer couple to data line f) terminate with Zo/2 from line to ground at receiver g) specify differential driver with low delta Voc
12. Open circuit fail-safe	a) no or too large of pull-up and pull-down resistors on receivers	a) use resistors low enough to maintain Vt max with Iin max b) use line receiver with fail-safe resistors internal
13. Terminated fail-safe	a) differential voltage not driven to Vt max at receiver b) protocol logic allows indeterminate state c) line pull-up and pull-down too large	a) change software to eliminate indeterminate state b) add offset voltage greater than Vt max c) reduce line pull-up and pull-down resistor values
14. Receive noise as data	a) terminated fail-safe	a) add terminated fail-safe offset voltage
15. Transient noise	a) lightning b) adjacent high voltage or current equipment c) RFI	a) add common-mode noise immunity
16. Bus contention	a) arbitration protocol	a) fix software
17. Receive noise after disconnecting cable	a) open circuit fail-safe	a) add open circuit fail-safe circuit

Notes

SECTION 4.
INTELLIGENT POWER

INTELLIGENT POWER INDEX

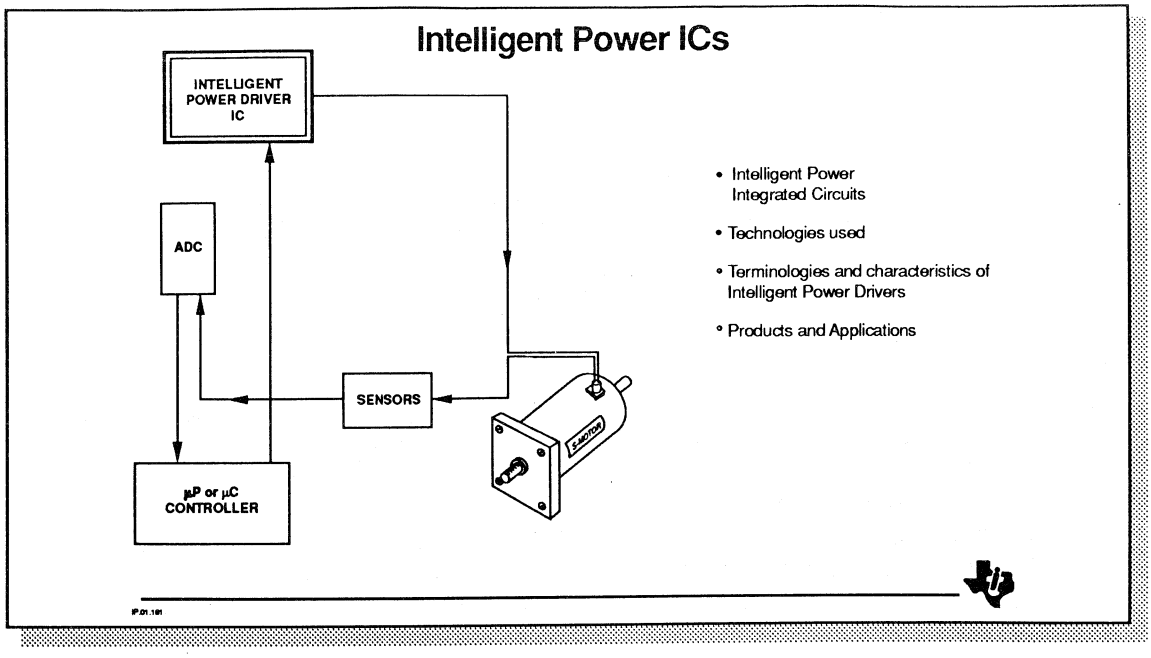


Figure 1 - Intelligent Power ICs

Section Overview

This section of the seminar addresses Intelligent Power Integrated Circuits and will cover:

- **Trends in the Industry**
- **Technologies Used**
- **Terminology and Characteristics of Intelligent Power ICs**
- **Intelligent Power Driver Products**
- **Applications of Intelligent Power Drivers**
- **Thermal considerations**

With the growth of microprocessors and computers used for the control of power equipment such as motors, power solenoids, and relays, has come the need for power drivers with built in protection and control logic. Any Intelligence built into the power drivers results in less effort and time for the already complex controller.

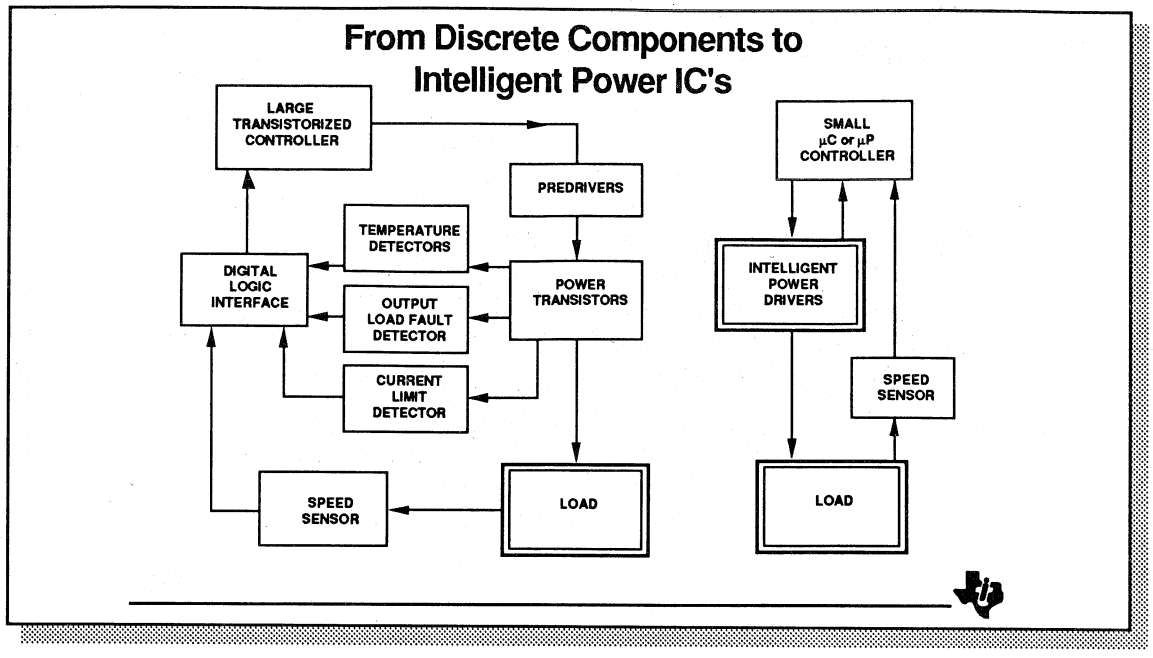


Figure 2 - From Discrete Components to Intelligent Power ICs

The capability of driving power loads reliably with a degree of control and protection from various fault conditions has, in the past, required a lot of discrete products. Today's Industrial, Consumer, and Automotive markets require products that include such functions as:

- **Temperature Detection**
- **Output Fault Detection**
- **Output Current Detection and Limiting**
- **Predrivers**
- **Rapid Load Turn-off Capability**
- **High Output Currents**
- **High Reverse Voltage Capabilities**

Notes

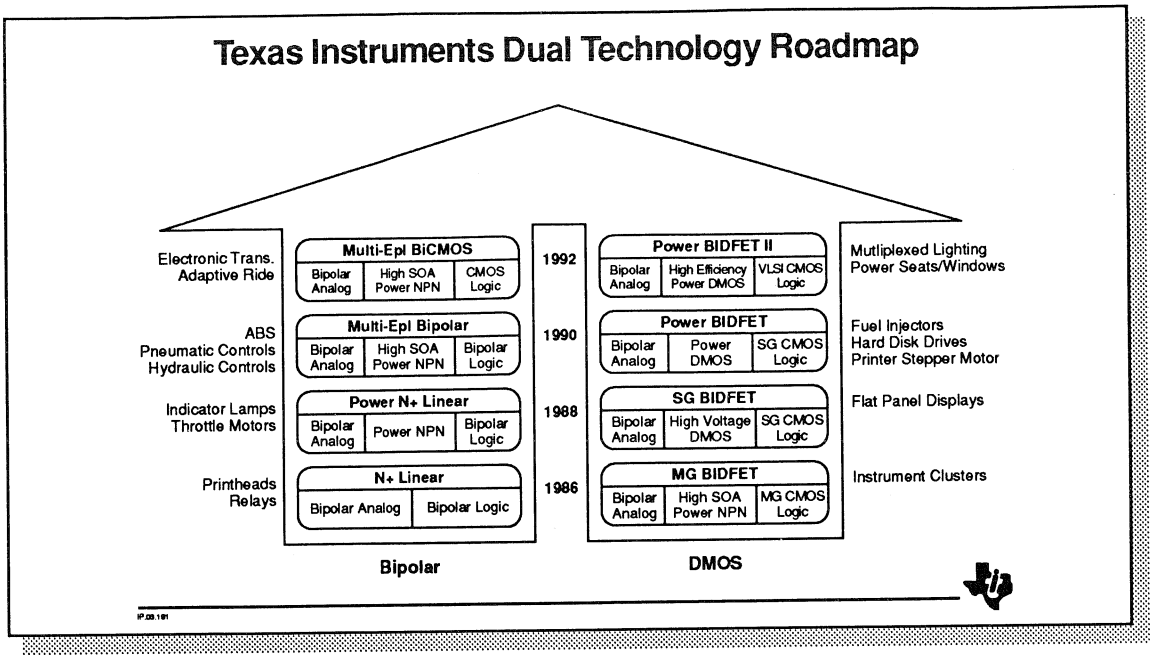


Figure 3 - Texas Instruments Dual Technology Roadmap

To meet the demand for Intelligent Power Drivers in the marked, Texas Instruments has developed new "Advanced Linear Process Technologies" that solves the problems and high cost of implementing power driver functions with discrete circuits.

In the mid '80s standard Bipolar Analog and Bipolar logic were combined on the same chip to implement thermal printer head, LED, relay, and solenoid drivers. These devices provided direct interface between logic control circuits and their higher voltage and current loads.

Developments in BIDFET Process Technology

For high voltage (60 to 125V) display systems, a Metal-Gate BIDFET process was developed. BIDFET is a combination of rugged Analog Bipolar with high speed metal-gate CMOS Logic and a high voltage (150V) Double Diffused MOS (DMOS) process. BIDFET provided a practical way to interface between microcontrollers and complex display systems. Large numbers of discrete power transistors, predrive transistors, and logic interface circuits were no longer required. Many of these early BIDFET drivers were 32 channel devices containing 64 power output switching transistors, predrive transistors, high speed CMOS shift registers and rugged bipolar input stages. As a result of the combined technologies used, BIDFET devices can operate at data input rates of up to 4MHz, switch 125V loads at 20mA and still require only about 25mA of standby current.

In 1988 a dedicated NPN power transistor was combined on the same chip with standard bipolar logic and analog circuits to provide up to 2A output drive. This extended the power IC capabilities to small motors as well as heavy duty solenoids and relays.

About the same time the Silicon Gate BIDFET process was also introduced. With Silicon Gate CMOS logic in place of the older Metal Gate CMOS process, the BIDFET drivers were now faster and at the same time lower in power dissipation. Thus their long time reliability was significantly increased and large flat screen display systems not only became practical but very easy to implement.

Multi-Epi & Power BIDFET Roadmap

In 1990, Texas Instruments made another significant improvement with the Advanced Linear Multi-Epi Bipolar process. This gave, for the first time, a discrete-like power NPN structure on the same chip. Operating currents of up to 10A are implemented with Multi-Epi Bipolar technology.

Power BIDFET was introduced using Advanced Linear Power DMOS and providing higher output currents (up to 3A) and the low r_{DS} on of MOS switches. Power DMOS allows efficient power switching, low internal power dissipation, and therefore high reliability.

The future will give Texas Instruments a "Multi-Epi BiCMOS" technology combining fast and low power CMOS logic with the Multi-Epi Bipolar process. These processes will allow an output current switching of up to 30A. Power BIDFET II allows for a significant increase in the circuit complexity with VLSI CMOS logic and highly efficient Power DMOS. Larger motors and more complex display and/or lighting systems may be driven with these new highly reliable power drivers.

Notes

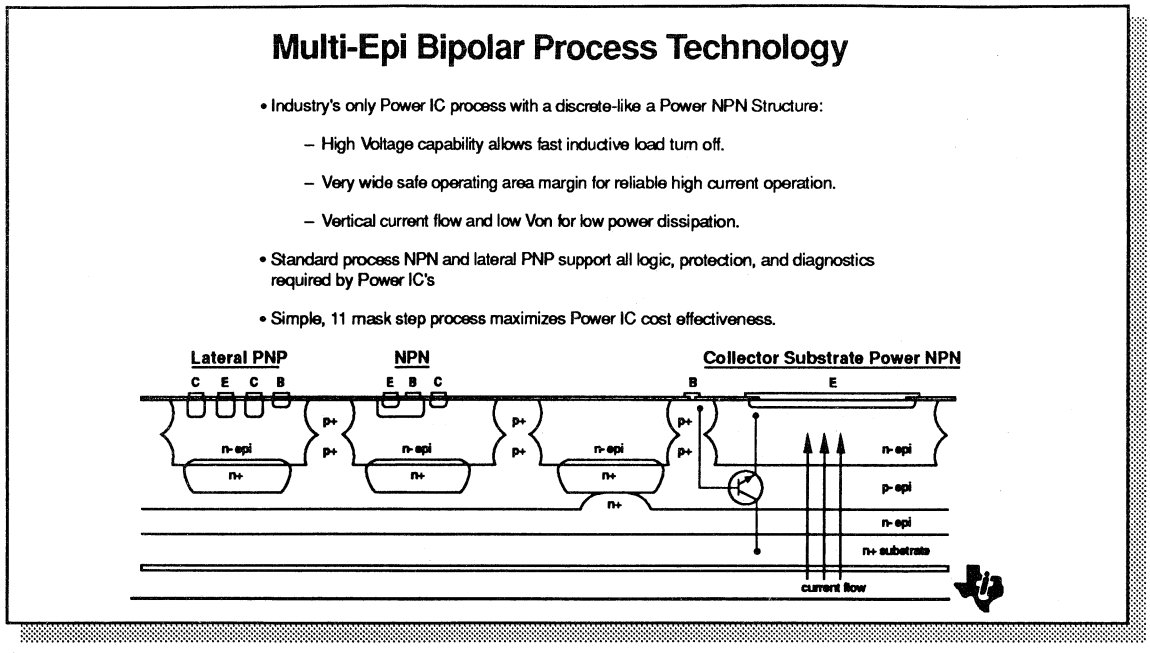


Figure 4 - Multi-EPI Bipolar Process Technology

Process Features

A patented, multi-epitaxial bipolar process, from Texas Instruments was the first to achieve three-dimensional integration. The "Multi-Epi Bipolar" process allows Texas Instruments to make intelligent power ICs by effectively combining small signal logic and control transistors on the same chip with discrete-like NPN power transistors. The Multi-Epi Bipolar IC consists of lateral PNP transistors, standard NPN transistors, and a discrete like vertical NPN power transistor on the same chip. By incorporating special logic and sensing circuits the high voltage, high current chip protects itself from short circuit faults, over current, and over temperature. Diagnostic circuitry can also indicate open circuits and monitor the output voltage.

In multi-epitaxial bipolar ICs, power transistors are usually vertical devices, while logic gates are laterally grown devices. Chip architecture, however, allows integration of high-density CMOS logic as well. Vertically grown epitaxial transistors handle more power than lateral transistors, and are capable of switching up to 20A at 500V with appropriate process adjustments.

No Thermal Runaway

Several benefits are inherent to the multi-epitaxial process. For one, vertical power transistors resist thermal runaway and other undesirable effects such as hot spots and current crowding. As local current density through the base emitter junction increases, the voltage across the vertically integrated ballasting resistor R_{epi} also increases. This reduces the forward bias of

the junction in that area and prevents failure mechanisms such as current crowding and hot spots. Thermal runaway is prevented because the DC current gain has a negative temperature coefficient. That is, temperature rises act to shut off power transistors by a negative feedback mechanism. In conventional bipolar transistors, increasing current heats the semiconductor material, which causes the dc current gain to become larger. At some point, the positive feedback becomes unstable and the device goes into thermal runaway. This condition is prevented by the multi-epitaxial process.

High Voltage Operation and Battery Reversal Protection

Another benefit of multi-epitaxial technology results from the type of isolation that separates high-voltage and low-voltage devices. In multi-epitaxial ICs, power and logic sections are isolated from each other by reverse-biased diodes. This allows power transistors to safely operate at voltages well in excess of 50V.

Isolation junctions also protect the IC during inadvertent battery reversal. Reversal protection is supplied by a junction in series with the supply input, and another in series opposing at the output. Output protection prevents the load from being actuated or destroyed in the event of battery reversal because it blocks reverse current flow between the output pin and the load.

Notes

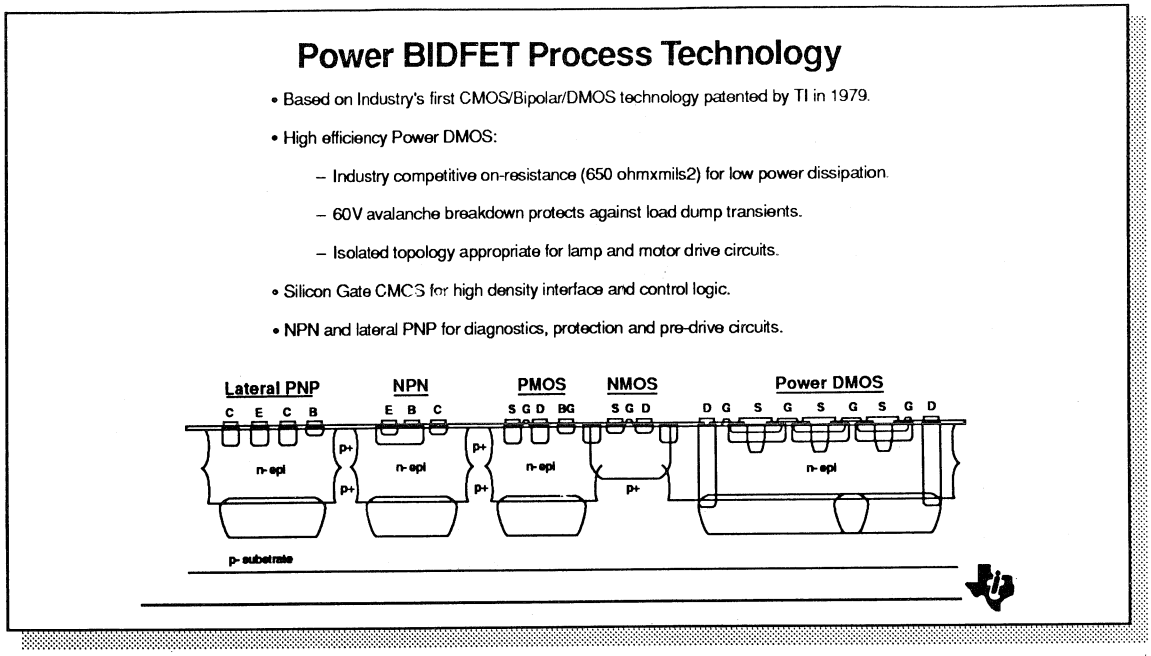


Figure 5 - Power BIDFET Process Technology

Texas Instruments led the industry with the introduction of the first BIDFET technology in 1979. BIDFET is a patented technology merging Bipolar, CMOS and DMOS processes on a single chip. Initial BIDFET products were Display Drivers followed closely by Voltage Regulation products and Telecom products.

More recently (1990) Texas Instruments introduced the first Intelligent power products to include the new "Advanced Linear Power BIDFET" technology. Power BIDFET processes include the following:

- **Bipolar Lateral PNP and standard NPN Bipolar transistors**
  - Rugged-fast input inter-facing
  - Diagnostic and protection logic
  - Predrive circuits

- **Silicon-gate CMOS transistors**
  - High density
  - High speed
  - Low power dissipation
  - Highly reliable logic control functions.

- **Power DMOS transistors**
  - Highly efficient power switch
  - Low on resistance
  - Built in load dump protection
  - Isolated output topollogy

Because the double-diffused metal oxide (DMOS) transistors look resistive between source and drain, and exhibit a positive temperature coefficient of R_{on}, which allows very reliable power DMOS output structures to be designed. The usual bipolar problems of current hogging and thermal runaway are not a problem with the efficient Power DMOS structure.

By merging Advanced Linear silicon-gate CMOS and DMOS processes on the same chip, Power BIDFET has the capability for very high density logic, a particularly advantageous characteristic where system space constraints require consolidation of many peripheral functions on a single chip. Power BIDFET's DMOS efficiency matches the best production capability in the industry.

Notes

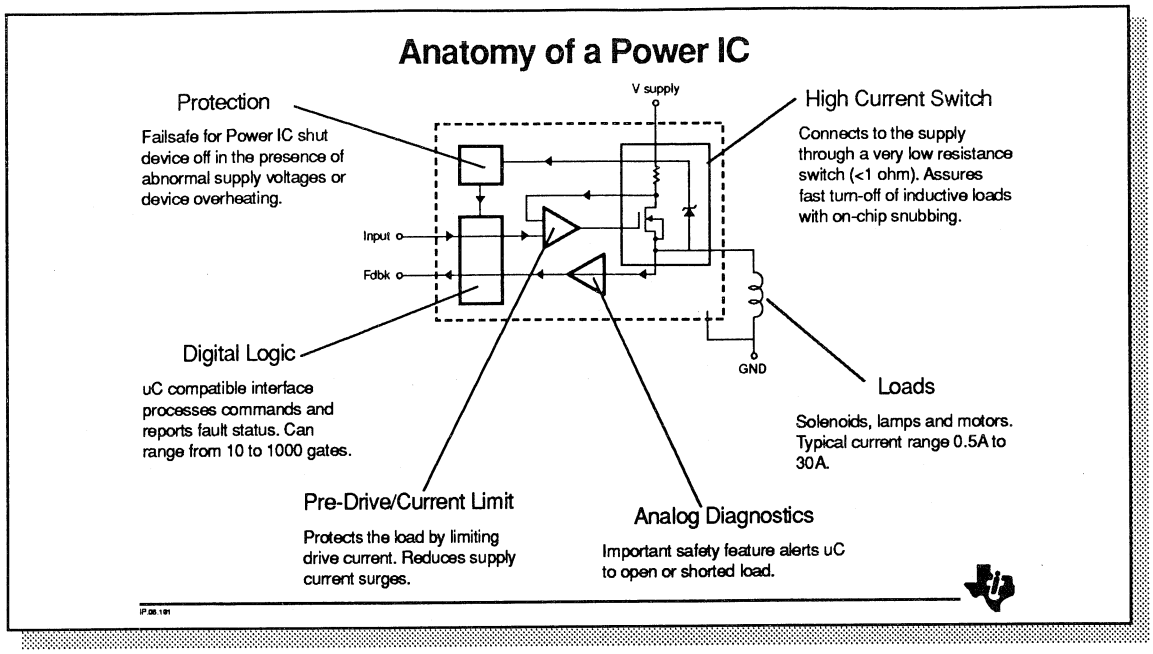


Figure 6 - Anatomy of a Power IC

An Intelligent Power IC is much more than just a high current switch. The following characteristics are desired in any intelligent power drive system:

- **High Current Switch**
  Connects load to the supply through a very low on resistance switch (<1Ω). Results in high efficiency. Fast turn-off of inductive loads is assured with on-chip snubbing.

- **Load Capability**
  Can drive solenoids, lamps and motors with typical currents ranging from 0.5A to 30A.

- **Output Diagnostics**
  Monitors output load conditions and provides the system controller with the status. Output failure modes (shorts or opens) are reported resulting in improved reliability.

- **Predrive Current Limiting**
  Reduces supply line surges and protects the load by limiting drive current.

- **Digital Control Logic**
  Provides the interface to the microcomputer or microcontroller. The control logic handle incoming commands and feedback system fault status. The complexity may range from 10 to 1000 gates depending on the control functions required.

- **Protection**
  Internal failsafe circuits provide the power IC control circuitry with turn-off signals in the presence of abnormal supply voltages or chip overheating.

Intelligent Power ICs are therefore highly fault tolerant with extensive self protection features. In addition device outputs may be of several popular configurations:

1. **High-side drivers**
   Where the outputs are active high driving the load with the low side of the load usually connected to ground. The diagram of the "Anatomy of a Power IC" is of a high-side driver.

2. **Low-side drivers**
   Outputs are active low driving the load with the high side of the load usually connected directly to the supply voltage. In this configuration the supply is always connected to the load.

3. **Totem-Pole or 1/2 "H" drivers**
   Where the outputs are both active high and active low. This allows reversible drive of the load and when two 1/2 "H" drives are found in one device it may be referred to as a full "H" driver and is often used to drive stepper motors and reversible solenoids.

Notes

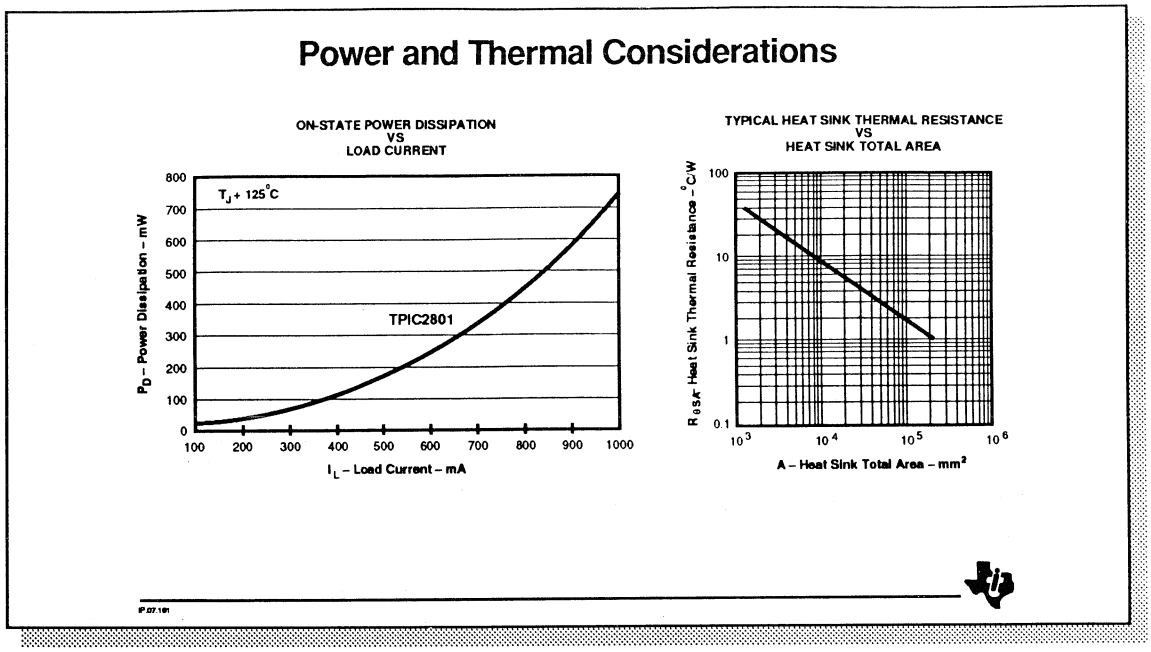


Figure 7 - Power and Thermal Considerations

Typical Example

TPIC2801 with the following **operating conditions**:

- o T_A = 100°C, T_J = 125°C
- o TPIC2801 quiescent current, I_{CC} = 0.15A max. @ T_J = 105°C and V_{CC} = 5V (Data sheet specification).

Output switches Y_0 & Y_4:	I_L= 0.5A each	@ 50% duty cycle
Output switches Y_1 & Y_5:	I_L= 0.7A each	@ 80% duty cycle
Output switches Y_2 & Y_6:	I_L= 0.8A each	@ 100% duty cycle
Output switch Y_3:	I_L= 0.5A	@ 100% duty cycle
Output switch Y7:	I_L= 0.9A	@ 100% duty cycle

Determining Heat Sink Requirements

1. Determine total switch power dissipations

Power dissipation of individual lowside switches, P(Yn), is a function of the output load current given by:

$$P(Yn) = P_D * d * n;$$

where,

P_D = ON-STATE Power Dissipation at the given Load Current
d = Duty Cycle
n = Number of Outputs

The total average power dissipation, $P_{T(av)}$, can now be determined for the TPIC2801 example, by the graph of its Power Dissipation versus Load Current (see Figure). Using this graph and the operating conditions above we find the following:

P(Y0-4)	= 0.17W * 0.5 * 2	= 0.17W
P(Y1-5)	= 0.33W * 0.8 * 2	= 0.53W
P(Y2-6)	= 0.45W * 1* 2	= 0.90W
P(Y3)	= 0.17W * 1 * 1	= 0.17W
P(Y7)	= 0.53W * 1 * 1	= 0.53W
P(quies)	= 0.15A * 5V	= 0.75W
$P_{T(av)}$		= 3.05W

2. Determining the heat sink to the ambient thermal resistance required

Note!! If the $R_{\theta SA}$ (heat sink to ambient thermal resistance) calculated is less than the package $R_{\theta JA}$ (junction to ambient thermal resistance) an external heat sink must be used. For the TPIC2801, $R_{\theta JA}$ is 35°C/W.

$$R_{\theta SA} = \frac{T_J - T_A}{P_{T(av)}} - |R_{\theta JC} + R_{\theta CS}|$$

$$= \frac{125°C - 100°C}{3.05W} - |3.0°C/W + 0.5°C/W|$$

$$= 4.70°C/W;$$

Notes

where,

$R_{\theta JC}$ = Junction to case thermal resistance
= 3°C/W - TPIC2801data sheet specification
$R_{\theta CS}$ = Case to heat sink thermal resistance
= 0.5°C/W - typical with thermal joint compound

As the calculated $R_{\theta SA} < R_{\theta JA}$, a heat sink must be used.

Using the typical example of Heat Sink Thermal Resistance versus Heat Sink Total Area (both sides) we find that A = 0.26 square metres (see Figure).

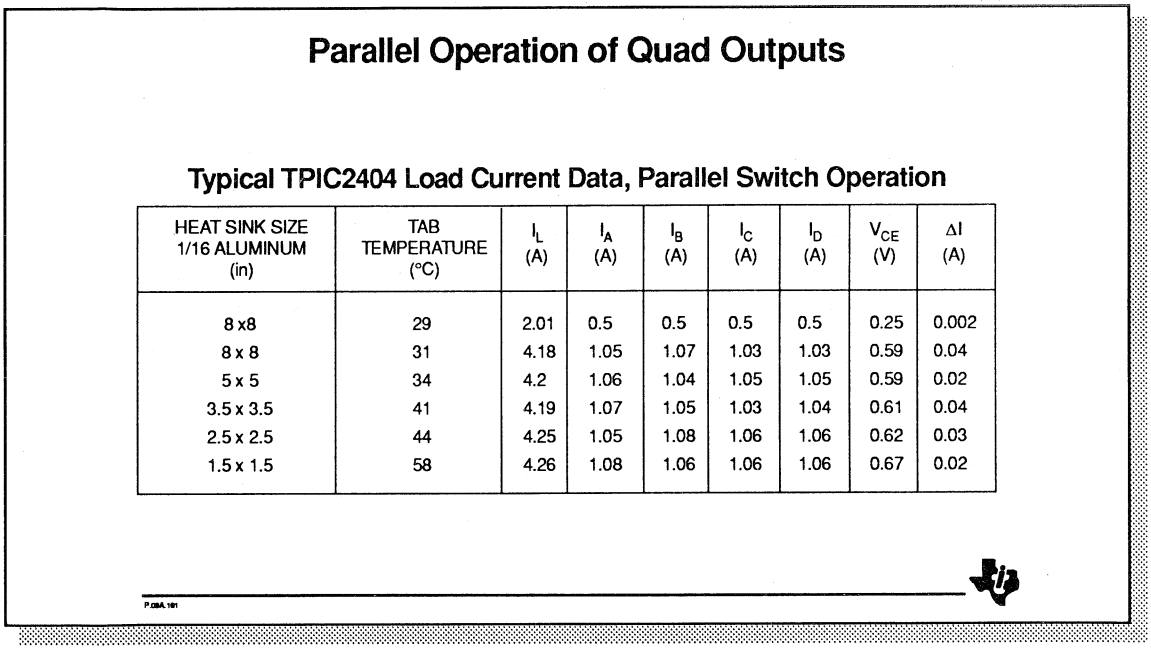


Figure 8 - Parallel Operation of Quad Outputs

Typical TPIC2404 Load Current Data in Parallel Switch Operation

Most of the intelligent power, multi-channel, drivers may be connected for parallel operation. Paralleling the outputs allows for extension of the load current drive capability.

The example shown is for the quad TPIC2404 with 1A per channel output drive capability. The figure illustrates current sharing of the four TPIC2404 outputs to extend the drive capability up to about 4A. The table lists heat sink sizes required for a typical load of 4A operating at an ambient temperature of 25°C. Note that the uniform characteristics of the Multi-epi output drivers results in a current difference, ΔI, measured between any combination of switches is typically no greater than 40mA.

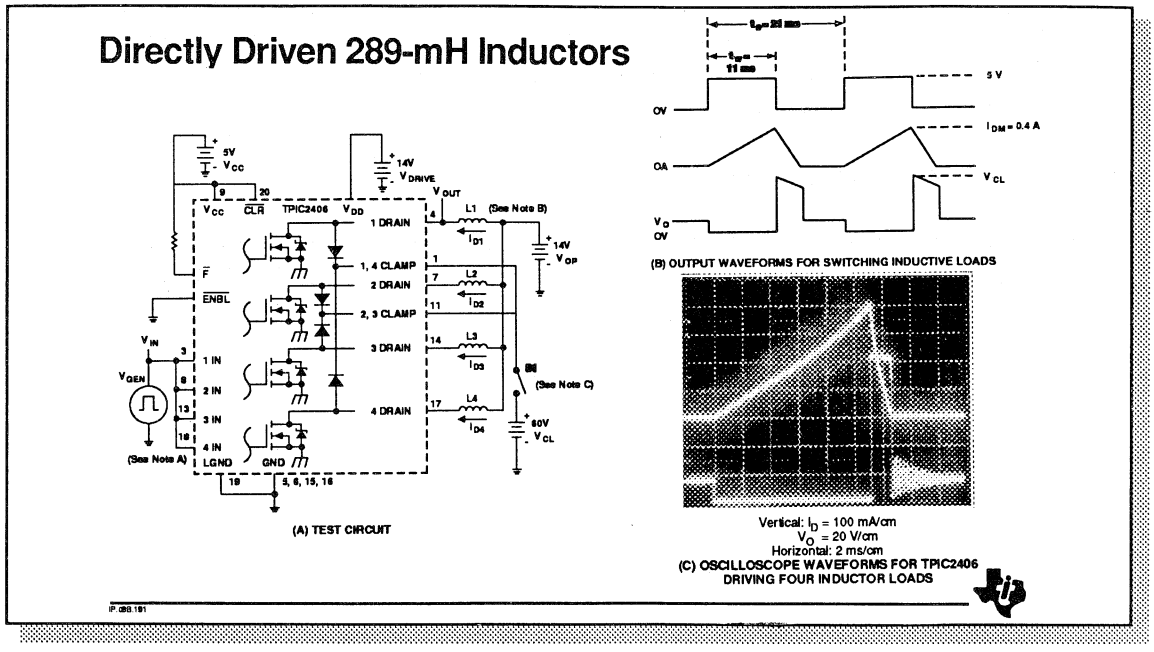


Figure 9 - Directly Driven 289mH Inductors

The TPIC2406 avalanche energy rating of 50mJ per output switch greatly enhances its value in applications requiring an inductive load driver. Therefore, depending on the device's total power dissipation, heat sinking, and operating temperature, inductive loads less than or equal to 50mJ will not normally require an external voltage clamp. If an external clamp is required, included in the TPIC2406 are two pairs of integral transient suppression clamp diodes. One diode pair is connected to the open drains of output MOSFETs 1 and 4, whilst the other diode pair is connected to the open drains of output MOSFETs 2 and 3, as seen in the figure. The absolute maximum voltage rating of the TPIC2406's output MOSFETs and clamp diodes is 60V, which should not normally be exceeded.

The figure shows the test circuit, (a), the output waveforms, (b), and the oscilloscope waveforms, (c), of the TPIC2406 simultaneously driving four 289mH inductors at 48 Hz and a 52% duty cycle switching condition. The TPIC2406 provides a 0.4A maximum current to each output load, which is limited by the 11ms on time and the 289mH/15Ω load.

Notes

As shown by the following equations, each output switch absorbs an inductive energy of 25.7mJ if no external clamp is used, which makes the device's total power dissipation, P_T = 5.16W. Therefore either an external heat sink is required, or an external clamp diode must be used if heat sinking is not available.

Energy and Power Calculations

During the power-on time the inductor's current approximates to a linear ramp, due to the L/R_L time constant being greater than the turn-on time. This results in a mean square drain current of $1/3 I_{DM}^2$, with I_{DM} equal to the peak drain current. Therefore the power dissipated in the output MOSFET, P_{on}, is equal to:-

$$P_{on} = \frac{1}{3} * I_{DM}^2 * r_{DS(on)} * d$$

$$= \frac{1}{3} * 0.4^2 * 1 * 0.52$$

$$= 0.027W$$

When the output MOSFET is turned off, the back e.m.f. generated by the inductor raises the drain voltage, which is internally clamped, to approximately 100V. It is possible to allow internal clamping as long as the criteria stated in note C below are met.

The energy consumed by the output stage when operated without a clamp can be found by using an equation from the JEDEC standard number 10:-

$$E_T = \frac{3 * L * I_{DM}^2 * V_{CL}}{6 * (V_{CL} - V_{OP}) + 4 * R_L * I_{DM}}$$

This equation assumes a linear decay of the current in the inductor. The energy consumed by the output MOSFET can be also found by looking at the exponential decay of the current through the inductor. The current flowing the inductor as it decays will follow the following equation.

$$I_L = \left(I_{DM} + \frac{V_{CL} - V_{OP}}{R_L} \right) * e^{-\frac{R_L}{L} t} - \left(\frac{V_{CL} - V_{OP}}{R_L} \right)$$

Integrating the product of the inductor current and the clamped drain voltage, will give a more accurate answer for the total energy consumed by the output MOSFET. So

$$E_T = \int_0^{t_1} V_{CL} * I_L * dt$$

$$= V_{CL} * \frac{L}{R_L} * \left(I_{DM} - \frac{V_{CL} - V_{OP}}{R_L} \right) * \ln \left(1 + \frac{I_{DM} * R_L}{V_{CL} - V_{OP}} \right)$$

$$= 25.7mJ$$

Where t_1 is the time taken for the inductor current to decay to zero, and is derived from the equation for I_L. Hence the value for t_1 is given by:-

$$t_1 = \frac{L}{R_L} * \ln \left(1 + \frac{I_{DM} * R_L}{V_{CL} - V_{OP}} \right)$$

The power dissipated during the turn-off period, P_{off}, can be equated to the product of E_T and the of switching:-

$$P_{off} = E_T * f$$
$$= 0.0257 * 48$$
$$= 1.23W$$

Hence the total power, P_T, dissipated in the output MOSFET is

$$P_T = (P_{off} + P_{on}) * n + (V_{CC} * I_{CC} + V_{DD} * I_{DD})$$
$$= (1.23 + 0.027) \times 4 + (5 * 0.010 + 14 * 0.006)$$
$$= 5.16W$$

Where;

L	= Load inductance	= 298mH
I_{DM}	= Peak drain current	= 0.4A
V_{CL}	= Max output/clamp voltoltage	= 100V
V_{OP}	= Load supply voltage	= 14V
R_L	= Inductor resistance	= 15Ω
f	= Switching frequency	= 48Hz
d	= Duty cycle (ratio)	= 0.52
r_{DS}	= Drain to source "on" resistance	= 1Ω
n	= Total number of switches operating	= 4

Notes

Notes to the Figure:

A. The pulse generator has the following has the following characteristics: t_r < 10ns, t_W = 11ms, PRR = 48Hz, V_{OUT} = 5V, Z_O = 50Ω. The input pulse duration, t_W, is increased until the peak load current, I_{DM} = 0.4A.

B. Inductors L1 = L2 = L3 = L4 = 289mH/15Ω.

C. If the TPIC2406 is operated on a heat sink capable of maintaining case temperature < 107°C, no external voltage clamp is required and S1 remains open. If case temperature cannot be maintained < 107°C, an external voltage clamp is required and S1 must be closed.

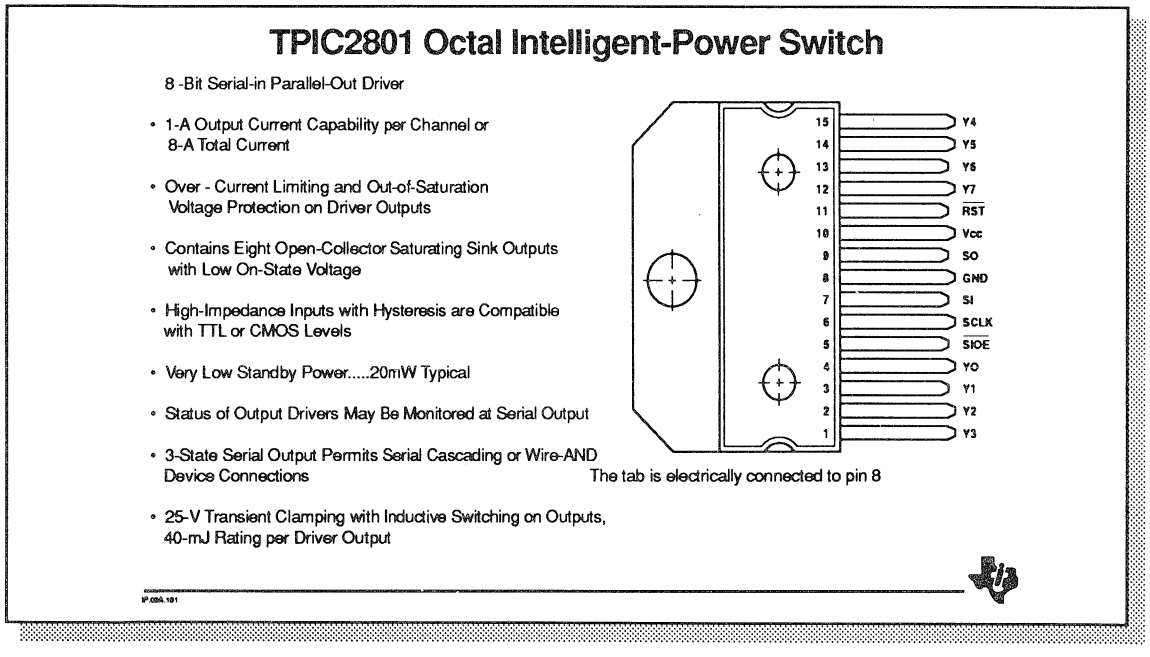


Figure 10 - TPIC2801 Octal Intelligent Power Switch

The TPIC2801 is an octal, **serial in - parallel out** integrated circuit **low-side** driver designed to sink up to 1A and clamping inductive voltage spikes to 30V. Simultaneous operation of the eight outputs will allow up to 8A total drive current. It is packaged in the 15-pin Single-In-Line Package (or SIP). The package designation, following the basic part number, is KV.

Control data is entered into the serial input (SI) and outputs are selected by an 8 bit serial word. Inputs are high impedance with hysteresis for high reliability TTL or CMOS compatibility.

The status of all outputs may be monitored at the serial output. Also, the serial output allows **cascading** of multiple devices for 16, 24, 32 etc. bits of operation.

Although the device has significant output power capability, it has a typical standby power requirement of only 20mW.

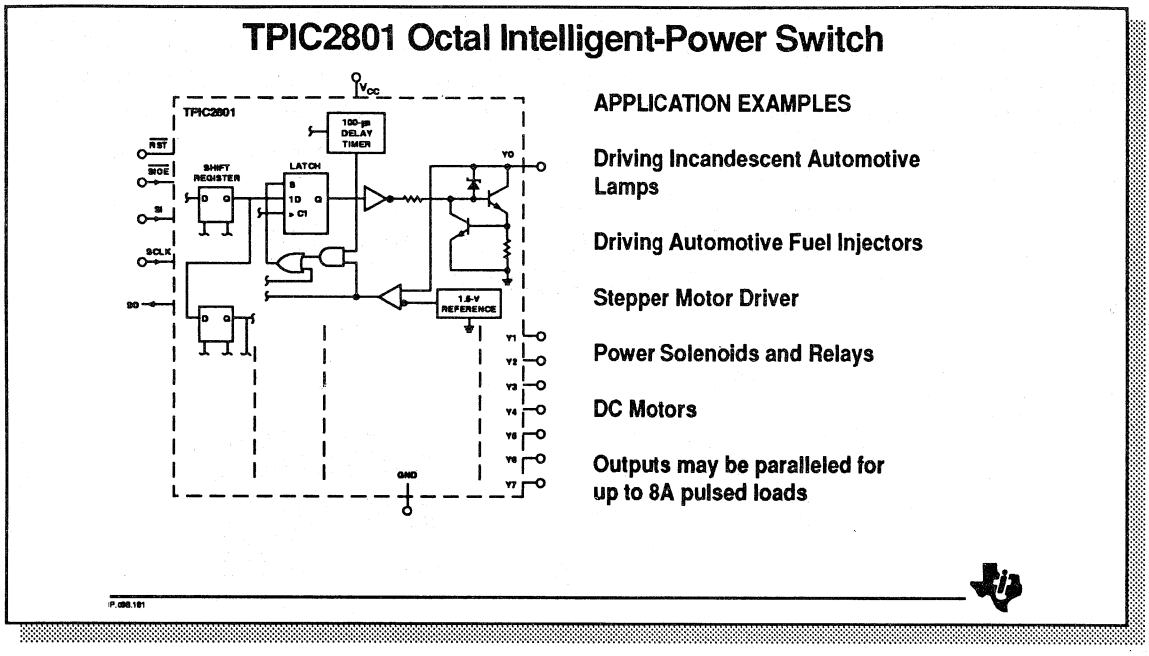


Figure 11 - TPIC2801 Octal Intelligent Power Switch (continued)

In a typical application of the TPIC2801 data is entered into the device serially via SI and goes directly into the lowest bit (0) of the shift register. Using proper timing signals, the input data is passed to the corresponding output latch and output driver. A logic-high bit at SI drives the corresponding output driver (Yn) off. A logic-low bit at SI drives the corresponding output driver on. Serial data is transferred into SI on the high-to-low transition of SCLK (serial clock) input in 8-bit bytes with data for Y7 output (MSB) first and data for the Y0 output (LSB) last. Both SI and SCLK are active when $\overline{\text{SIOE}}$ (Serial Input-Output Enable) is low, and disabled when $\overline{\text{SIOE}}$ is high.

Notes

Each driver output is monitored by a voltage comparator that compares the Y-output voltage level with an internal threshold voltage reference level. This threshold is above the normal output saturation levels and is therefore referred to as the "out of saturation threshold voltage". The logic state of the comparator's output is dependent upon whether the Y-output is greater or smaller than this reference voltage level. An activated driver output will be unlatched and turned off when the output voltage exceeds the out-of-saturation threshold voltage level, except when the internal unlatch enable is low and disabled. A high-to-low transition of $\overline{\text{SIOE}}$ transfers the logic state of the comparator's output to the shift register.

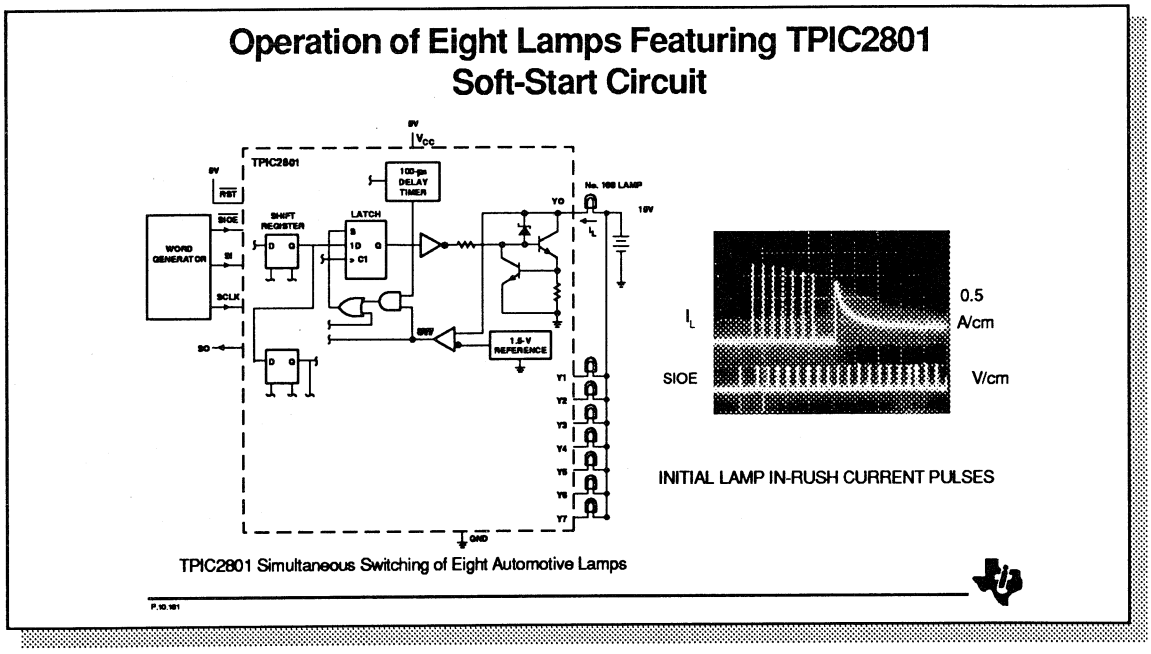


Figure 12 - Operation of Eight Lamps Featuring TPIC2801 Soft-Start Circuit

Soft Start-Up Feature Extends the Lifetime of the Lamps

In this application the TPIC2801 is used to switch eight No. 168 automotive lamps operating from a 15V supply. With the TPIC2801 clock operating at a frequency of 5kHz the scope photo shows that an initial lamp in-rush current of over 1.5A decreases to a value of less than 0.5A in about 120ms.

The rising edge of the $\overline{\text{SIOE}}$ pulse, following the data word, is when shift register data is latched into the parallel latch and the output switches are activated by new data. However, to allow the part to overcome high in-rush currents, such as those from a lamp's cold filament, an internal 100µs delay timer is started at the $\overline{\text{SIOE}}$ pulse rising edge. During this time the switch overvoltage fault shutdown circuit is inhibited. During this 100µs interval the switch is

protected by an internal current limiter, which is set to regulate the current to approximately 1.5A to 1.8A. Once the 100µs delay period has elapsed, the output voltages are sensed by the comparators and any output switch with a voltage higher than 1.5V is latched off. They will remain off until the rising edge of the next $\overline{\text{SIOE}}$ pulse occurs. It is important to note that these current limited, 100µs, soft-start bursts of power not only protect the TPIC2801, but also protect the lamp filament from excessively high and degrading in-rush currents.

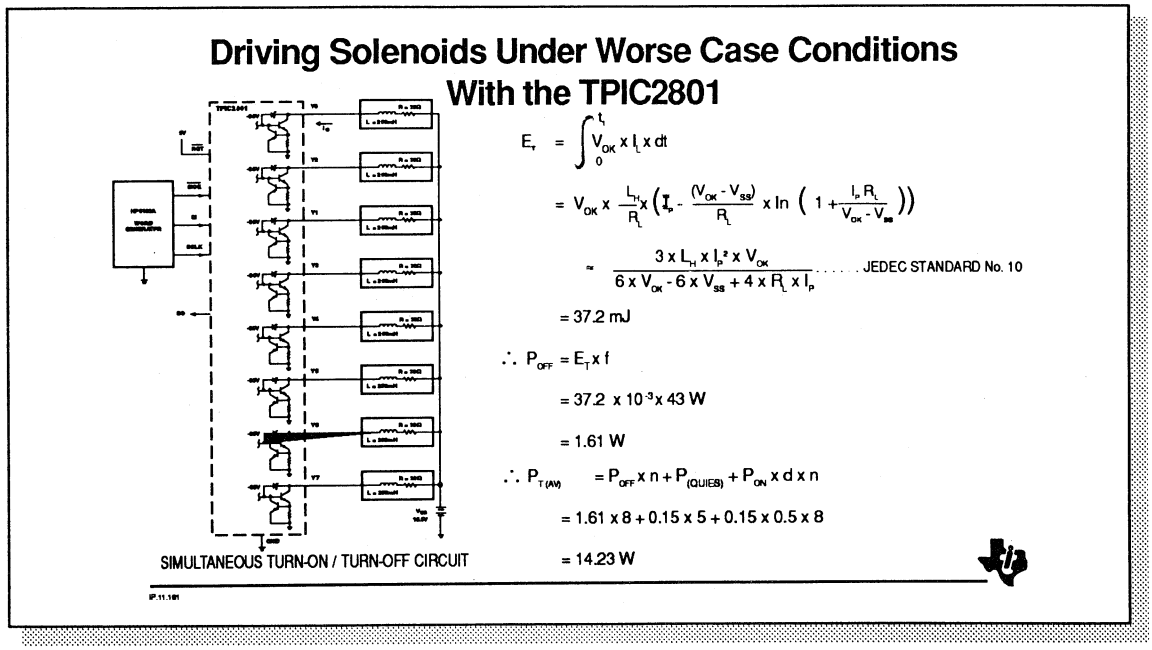


Figure 13 - Driving Solenoids Under Worst Case Conditions With the TPIC2801

Energy Calculation

In this application TPIC2801 is switching eight high-inductance solenoids (R = 30Ω, and L = 250mH) from a 15.5V supply source. The TPIC2801 provides 0.39A current to each inductor with each of it's output switches obsorbing an inductive energy of 37.2mJ per switch cycle as seen in the equation for E_T.

Notes

$$E_T = \int_0^{t_1} V_{OK} * I_L * dt ;$$

$$= V_{OK} * \frac{L_H}{R_L} * \left(I_P - \frac{V_{OK} - V_{SS}}{R_L} * \ln\left(1 + \frac{I_P * R_L}{V_{OK} - V_{SS}}\right)\right) ;$$

$$\simeq \frac{3 * L_H * I_P^2 * V_{OK}}{6 * (V_{OK} - V_{SS}) + 4 * R_L * I_P} \quad \text{... JEDEC Standard Nº 10 ;}$$

$$= \underline{37.2mJ}$$

where,

$$t_1 = \frac{L_H}{R_L} * \ln\left(1 + \frac{I_P * R_L}{V_{OK} - V_{SS}}\right) ;$$

$$I_L = \left(I_P + \frac{V_{OK} - V_{SS}}{R_L}\right) e^{-\frac{R_L}{L_H} t} - \frac{V_{OK} - V_{SS}}{R_L} ;$$

$$I_P = \frac{V_{SS}}{R_L}\left(1 - e^{-\frac{R_L}{L_H} * \frac{d}{f}}\right) ;$$

Note: Although the internal clamp is at 37V, the actual measured clamp voltage (37V in his case) is used for the value V_{OK}.

37.2mJ is a safe operating condition based on the TPIC2801's 40mJ maximum unclamped energy rating.

Power Calculation

$$P_{OFF} = E_T * f ;$$
$$= 37.2mJ * 43Hz ;$$
$$= 1.61W ;$$

$$P_{T(av)} = P_{OFF} * n + P_{(quies)} + P_{on} * d * n ;$$
$$= (1.61W) * 8 + (0.15A) * 5V + (0.15W) * 0.5 * 8$$
$$= \underline{14.23W}$$

Where,

E_T	=	Total turn-off transient energy absorbed by each switch	= 37.2mJ
f	=	Switching frequency	= 43Hz
d	=	Duty cycle	= 0.5
L_H	=	Load inductance	= 250mH
I_P	=	Peak output load current	= 0.5A
n	=	Number of output switches operating	= 8
P_{OFF}	=	Turn-off power dissipation each switch	= 1.58W
P_{ON}	=	On-state power dissipation each switch	= 0.15W
$P_{(quies)}$	=	TPIC2801 quiescent bias power dissipation	= 1.25W
$P_{T(av)}$	=	Average total power dissipation	= 14.49W
R_L	=	Resistance of inductor	= 30Ω
V_{OK}	=	Measured clamp voltage	= 37V
V_{SS}	=	Load supply voltage	= 15.5V

Notes

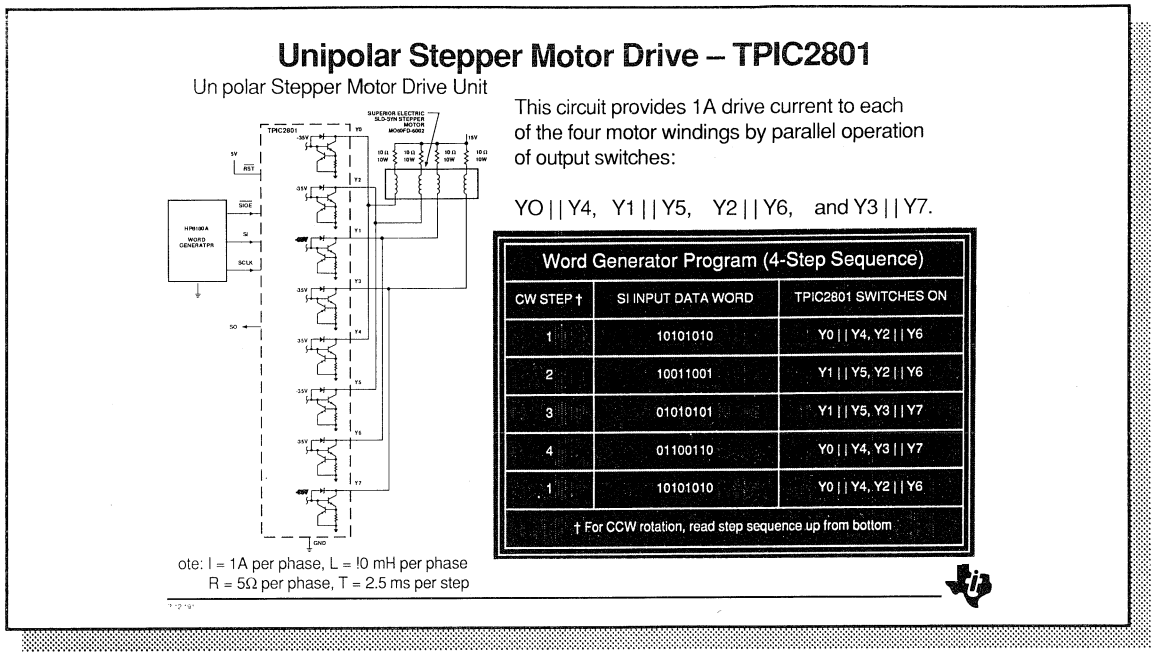


Figure 14 - Unipolar Stepper Motor Drive - TPIC2801

In this application, the drives for four windings of a stepper motor are provided by parallel operation of TPIC2801 output switches. The stepper motor requires 1A of drive per winding. Although it would be possible to get 1A output from each of four outputs of the TPIC2801, a significant reduction in power dissipation is possible by simply providing each winding's drive from two parallelled outputs. Comparing the device's on-state power dissipation for only four drivers operating at 1Aeach we find that the individual switch power dissipation is 740mW. If we parallel two switches, operating at 0.5A each, we find that their individual power dissipation is 160mW. The two parallelled switches would have a total on power dissipation of only 320mW for a 1A load resulting in a much cooler operating temperature and improved long term reliability.

The parallelled switches are Y0 & Y4, Y1 & Y5, Y2 & Y6, and Y3 & Y7.

The input logic for the TPIC2801 is normally provided by a microprocessor controller; however, for this application example a Hewlett Packard HP8180 Data Generator was programmed to generate the input step logic shown in the 4-step sequence table.

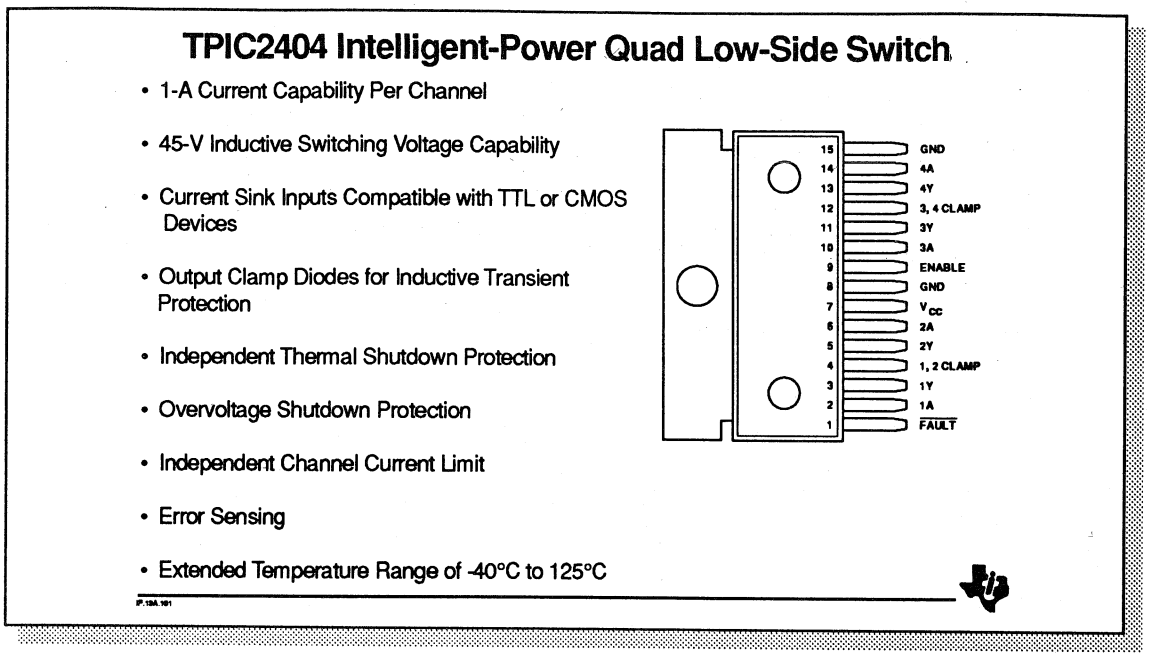


Figure 15 - TPIC2404 Intelligent Power Quad Low-Side Switch

The TPIC2404 is a monolithic, quadruple, low-side intelligent power switch packaged in a 15-pin Single-In-Line Package (SIP). It has been designed to operate in harsh electrical and thermal environments with several built-in protection features.

Features

Each of it's four outputs can switch 1A inductive loads while operating from up to 45V supply voltages. High impedance inputs allow operation from TTL or low-level CMOS with only 60μA maximum input current required. Each input has a current sink controlled by the ENABLE, which ensures that an open input is pulled low causing the output to be off.

Other built-in protection features include:

Notes

Error Sensing

The error sensing circuit monitors the outputs for open and short conditions by sensing and comparing the input logic state to the output state. An error condition is generated when the input voltage (V_I) and output voltage (V_O) are logically the same. This condition can also exist for other fault conditions such as overvoltage shutdown, and thermal shutdown. When any one of the fault conditions is sensed, the $\overline{\text{FAULT}}$ output will go on to a low state as its sink output is activated. An external filter capacitor is recommended to prevent a false fault output due to switching transients. Leave all unused outputs open and tie unused inputs high to prevent noise that could also cause false errors.

Thermal Shutdowm

Independent thermal shutdown circuits monitor and disable each output when the maximum temperature is reached, typically 155°C. A fault condition is then sensed and reported by the error sensing circuit. This condition remains until the temperature falls below 140°C and the thermal shutdown circuit allows the output to return to normal operation.

Overvoltage Shutdown

When the supply voltage exceeds the overvoltage condition, (25.5V to 31V), all outputs are disabled and a fault condition is sensed. When the supply voltage falls below 25.5V, the fault condition is removed and the outputs return to normal operation. There is a typical 0.25V hysteresis in the turn on, turn off thresholds to prevent noise problems.

Overcurrent Limit

The overcurrent limit is the maximum current each output is independently allowed to sink. The current limiting circuitry, at each output, monitors the output transistor's emitter current and limits its base drive when the maximum output current is reached. The output functionality is not affected nor is a fault condition reported.

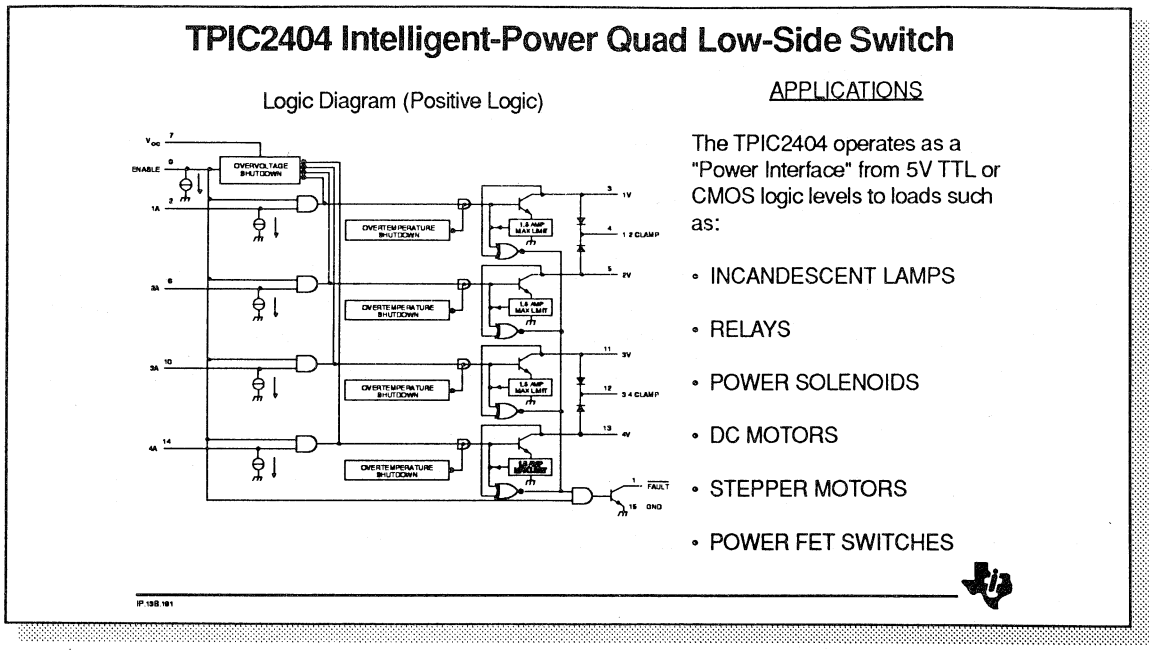


Figure 16 - TPIC2404 Intelligent Power Quad Low-Side Switch (continued)

Application Areas

The TPIC2404 is well suited for a wide variety of drive applications. As a result of its high impedance TTL level compatible inputs the TPIC2404 can operate from most of the microprocessors or microcontrollers available today. Output drive is suitable for a wide variety of loads such as:

- **Incandescent Lamps**
- **Relays**
- **Power Solenoids**

Notes

- **DC Motors**
- **Stepper Motors**
- **Power FET Switches**

Short-Circuit Safe Operating Area, SCSOA

When the TPIC 2404 is operating from a load supply voltage of less than 20V, its self protection features make it virtually indestructable. However, when the TPIC2404 is operating from a load supply between 20V and 45V (its maximum output voltage), the TPIC2404's $\overline{\text{FAULT}}$ output must be monitored to detect faults. This is especially true for shorted loads since the $\overline{\text{FAULT}}$ output must be used to detect the fault and signal the microprocessor controller to immediately turn off the output switches. The controller must provide the turn-off at supply voltages over 20V because the TPIC2404's thermal shutdown time is longer than its short circuit withstand time and an uninterrupted shorted load current will cause output switch secondary beakdown and device distributional.

Parallel Operation of Quad Outputs for Extended Output Capability

If all four output switches are not needed for an application and an output current of greater than 1A is required, the switches can be connected in parallel for extended current capability. Paralleling the outputs in pairs, when only two loads are to be driven, will also reduce the power dissipation in the switches to provide greater reliability.

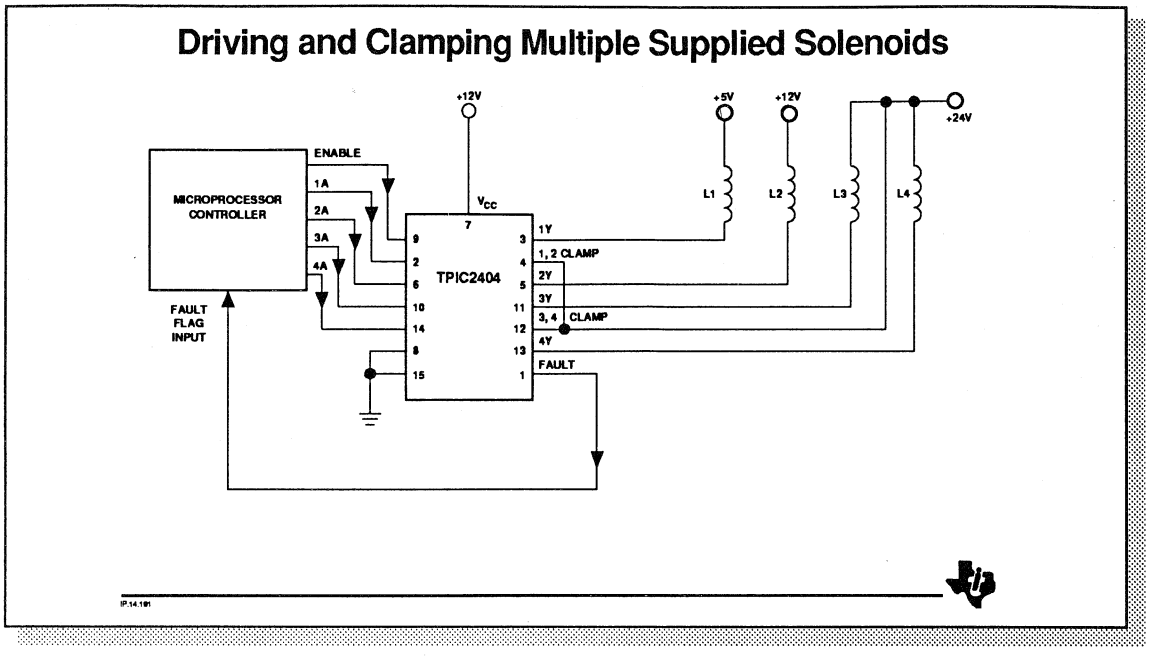


Figure 17 - Driving and Clamping Multiple Supplied Solenoids

Integral Clamp Circuit Capability

For clamping switched inductive loads, the TPIC2404 includes two pairs of integral transient suppression clamp diodes. One diode pair is connected to the open collectors of output switches 1 and 2, and the other diode pair is connected to the open collectors of output switches 3 and 4.

The absolute maximum voltage rating for the TPIC2404's output switches is 45V; therefore, the clamp diodes should never be connected to a supply voltage that exceeds 45V. In many applications the clamps may not be required as the TPIC2404 has a high 2.8mJ inductive energy capability. For example even when driving a large 100mH inductor with 73Ω resistance from a 15V power supply, the total inductive energy is only 2.1mJ.

Notes

$$E_L = \frac{L * I^2}{2}$$

$$= \frac{0.1H * (15V/73\Omega)^2}{2}$$

$$= \underline{2.1mJ}$$

The high unclamped inductive energy capability of the TPIC2404 should also protect it from reverse breakdown during the transient turn-on interval even if the slowest types of external clamp circuits are being used.

In this application inductors are operating from 5V, 12V, and 24V. With up to 45V output capability the diode clamps, pins 4 and 12, may both be returned to the 24V supply rail.

Fault Indication Design Hints

We are also using the $\overline{\text{FAULT}}$ (fault flag) output to feed back to the microprocessor controller's fault flag input providing it with error status. It is important to note that the $\overline{\text{FAULT}}$ output has a max sink current of only 75μA. A typical 10kΩ to 30kΩ pull-up resistor will "not" work, and in fact will disable the $\overline{\text{FAULT}}$ output. In this example a 270kΩ resistor to the V_{CC} = 12V supply rail provides the pull-up at less than 45μA. As previously mentioned, some filtering is required to keep noise pick-up low and prevent a false fault indication. A 0.1μF capacitor in parallel with the 270kΩ pull-up resistor will provide the required protection.

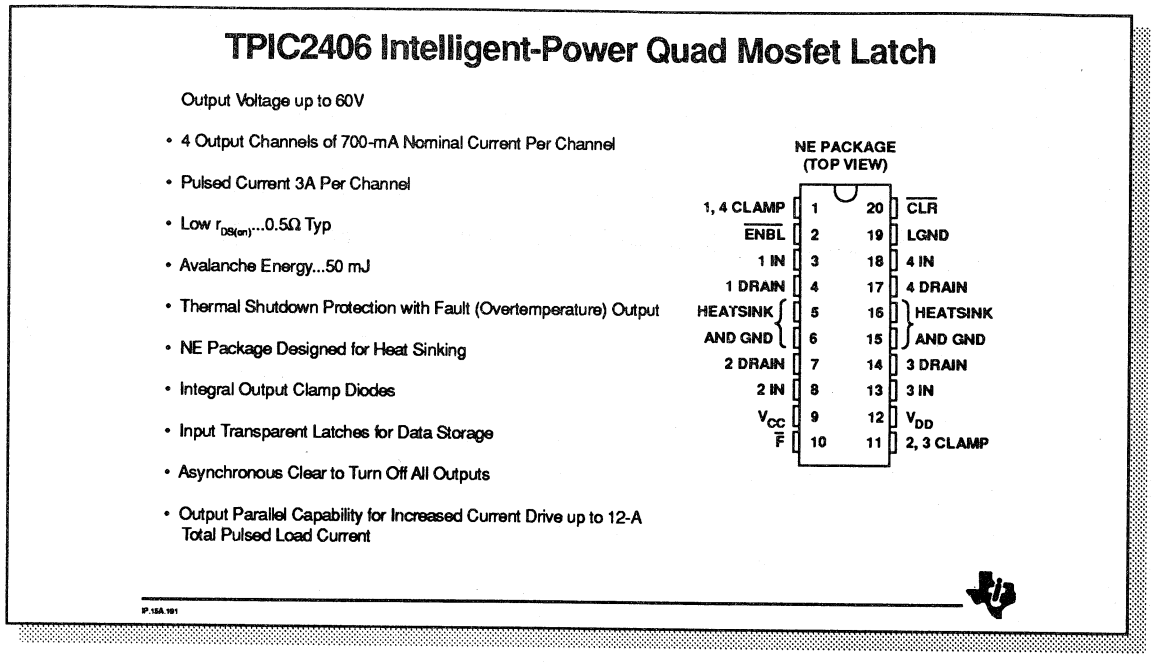


Figure 18 - TPIC2406 Intelligent Power Quad MOSFET Latch

The TPIC2406 is an intelligent power device that contains four self protected **low-side** power **MOSFET switches** packaged in a 20-pin NE DIP package. Each output can operate at up to 0.77A with supply voltages up to 60V and are controlled by an input storage latch with common clear and enable controls. All inputs accept standard TTL and CMOS logic levels.

Pulsed currents of up to 3A per channel are possible. Care must be taken to ensure pulse durations and operating duty cycles are consistent with the package thermal time constants and power handling capability. The 3A data sheet tests are done with 10ms max pulse duration at a 6% max duty cycle. This type of performance is possible due to the low (0.5Ω typ) on resistance of the output switches and the TPIC2406 package power handling capabilities. (6W total continuous dissipation at or below 100°C case temperature. For operation above 100°C case temperature derates linearly at the rate of 120mW/°C.)

Well matched driver output characteristics of the TPIC2406 also allows the designer to extend

Notes

the drive by **paralleling the outputs**. With the four outputs in parallel continuous currents of up to 3.0A and pulsed currents of up to 12A may be driven.

Driving inductive loads is easier with this device due to its high avalanche energy capability of 50mJ.

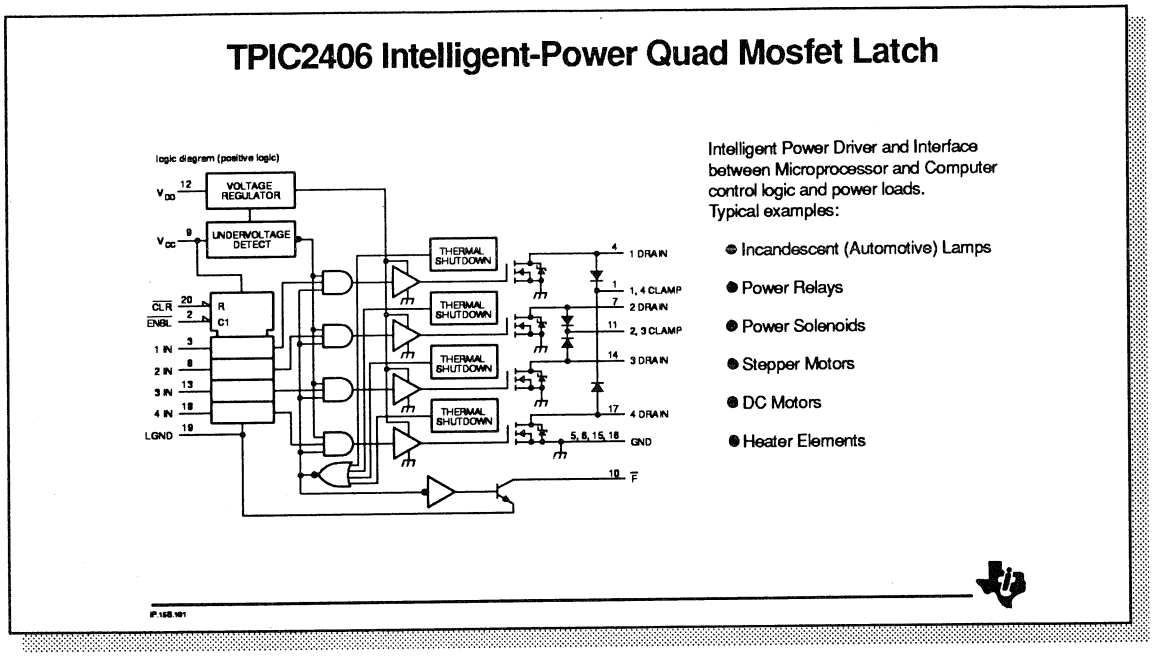


Figure 19 - Intelligent Power Quad MOSFET Latch (continued)

Additional TPIC2406 features include individual channel **thermal shutdown** shutdown circuits that **monitor each output** and disable all outputs when the maximum temperature of 155°C (typ) is reached.

Application Areas

The TPIC2406 intelligent power driver provides an easy interface from microprocessor, microcontroller, or discrete control logic to the power load requirements of applications such as:

- **Incandescent Lamps (automotive)**
- **Power Solenoids**
- **DC Motors**
- **Stepper motors**
- **Heater Elements**
- **Power Relays**

Control Features

Another input control feature, the $\overline{CLR}$ function, is asynchronous and turns all four outputs off regardless of data inputs. Taking $\overline{ENBL}$ low puts the input latch into a transparent mode, allowing the data inputs to affect the outputs. In this state, all four outputs will be held off while $\overline{CLR}$ is low, but will return to the stages on the data inputs when the $\overline{CLR}$ goes high. When $\overline{ENBL}$ is taken high, the latch is put into a storage mode and the last state of the data inputs is held in the latches. If the $\overline{CLR}$ input is taken low, the data in the latches is cleared, turning all outputs off. If $\overline{CLR}$ is taken high again, $\overline{ENBL}$ must be cycled low to read new data into the latch.

An internal voltage regulator provides the V_{CC} logic supply for internal control circuits. The internal "Undervoltage Detector" prevents improper operation due to low supply voltages by disabling the outputs when an undervoltage condition exists.

Notes

Power Thermal Considerations - 1

Example 1. Using transient thermal impedance to determine the maximum current of a single output with "n" outputs simultaneously conducting.

$$I_D = \sqrt{\frac{T_J - T_A}{Z_{\theta JA} \times r_{DS(on)} \times 4}} \times K_n$$

Where:

K_n	=	Current coefficient for the current of a single output with n outputs simultaneously conducting equal current	See Table Kn
$Z_{\theta JA}$	=	Transient thermal impedance ($Z_{\theta JA}$ vs on time graph)	
$r_{DS(on)}$	=	Static drain-source on-state resistance at 150° C (worst case)	1.05Ω
T_J	=	Junction temperature (worst case)	150°C
T_A	=	Ambient temperature	
4	=	Maximum number of outputs conducting equal current	

Figure 20 - Power Thermal Considerations - 1

In this design, **example-1**, the maximum output current for the TPIC2406 when all four currents are on at the same level, will be determined.

The equation for I_D, the maximum individual output drive, is as shown on the Figure.

K_n = The current coefficient for an output current with "n" outputs *on* at the same current level. (Figure 21 shows a table of K_n values versus the number of outputs "n" that are *on*). For example: n = 4 therefore $K_n = 1$.

T_j	= The maximum (worse case) junction temperature	= 150°C.
T_A	= The Ambient operating temperature	= 25°C (typ)
$Z_{\theta jA}$	= The thermal impedance (junction to ambient)	= 50°C/W (Note 1)
$r_{DS(on)}$	= Static drain-source on state resistance at 150°C	= 1.05Ω

Note 1: For transient conditions use the table in Figure 21 of transient impedance versus on time. This takes into account thermal time delays, output on times and the on time duty cycle.

It is important to note the value for a continuous current I_D under these conditions, with no heatsink, is about 770mA per output. Therefore any operation of all four outputs on continuously above the max rated current levels of 770mA would require some type of heat sink. More detailed information on this is given in the TPIC2406 Application Report - 1991.

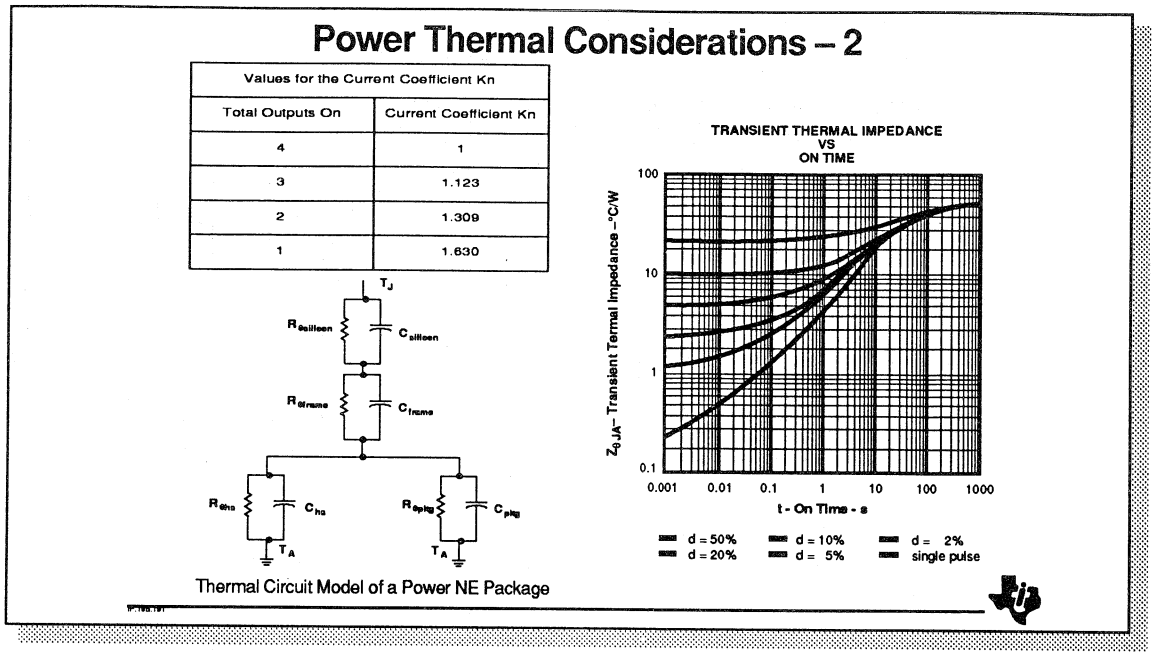


Figure 21 - Power Thermal Considerations - 2

The switching requirement of many applications is characterized by either single current pulses of short on time or by pulses of repetitive duration. For many of these applications, the large thermal capacitance of the 20-pin NE package limits the junction temperature to within the maximum ratings, even in the presence of large current pulses. For these applications the figure on "Transient Thermal Impedance versus On Time" may be used to determine the peak junction temperature.

The "Thermal Circuit Model of a Power NE Package defines the complete thermal impedance of the TPIC2406 by combining the two elements, thermal resistance and thermal capacitance. The top cell represents the silicon wafer, which has a time constant of about 30ms. The next cell represents the lead frame, which has a time constant of about 2s. The bottom two cells connected in parallel account for the external heat sink on the circuit board in parallel with the cell corresponding to the package molding compound. The time constant of the molding compound alone is about 200s.

Notes

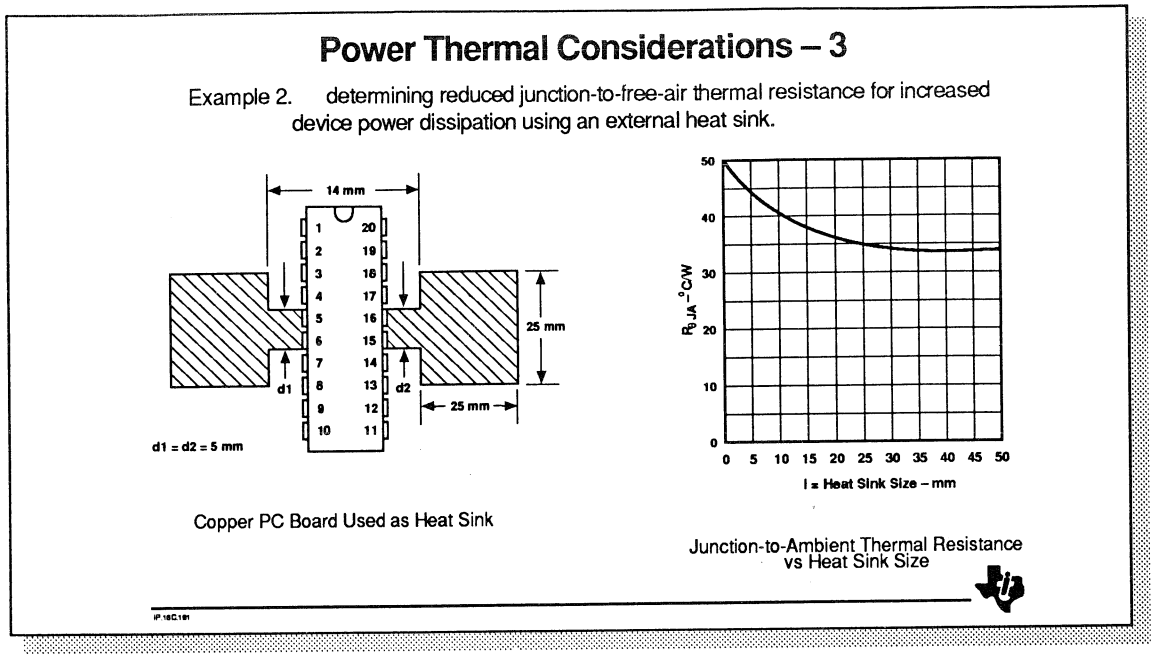


Figure 22 - Power Thermal Considerations - 3

Determining Junction-Ambient Thermal Resistance Requirements

In this **example - 2**, the junction to ambient thermal impedance ($R_{\theta JA}$) of the TPIC2406 can be reduced by soldering ground pins 5, 6, 15, and 16 to a copper area on the printed circuit board or to an external heat sink.

Using the two 1 inch square copper patterns, illustrated in our example, gives a total of 2 square inches. From the graph, of heat sink size, a two square inch area will give us a junction to ambient thermal impedance of 34°C/W. Using the formula for I_D, we find that each output could operate at a continuous current of up to 935mA if we are using the copper pattern heat sinks on the PC board.

Modifying the formula for I_D allows for solving of the junction to ambient thermal resistance "$R_{\theta JA}$" required in terms of the output currents and thermal conditions.

$$Z_{\theta JA} = \frac{T_J - T_A}{I_D^2 * r_{DSon} * n} * K_n^2 ;$$

For an example: I_D = 0.65A (each output), T_J = 150°C, T_A = 100°C, r_{DSon} = 1.05Ω, n = 4, and K_n = 1, gives:

$$Z_{\theta JA} = \frac{150°C - 100°C}{(0.65A)^2 * 1.05\Omega * 4} * 1^2 = 28.17°C/W ;$$

This value is less than what can be obtained with a copper PC board areas shown on the graph. Thus a suitable external heat sink would be required.

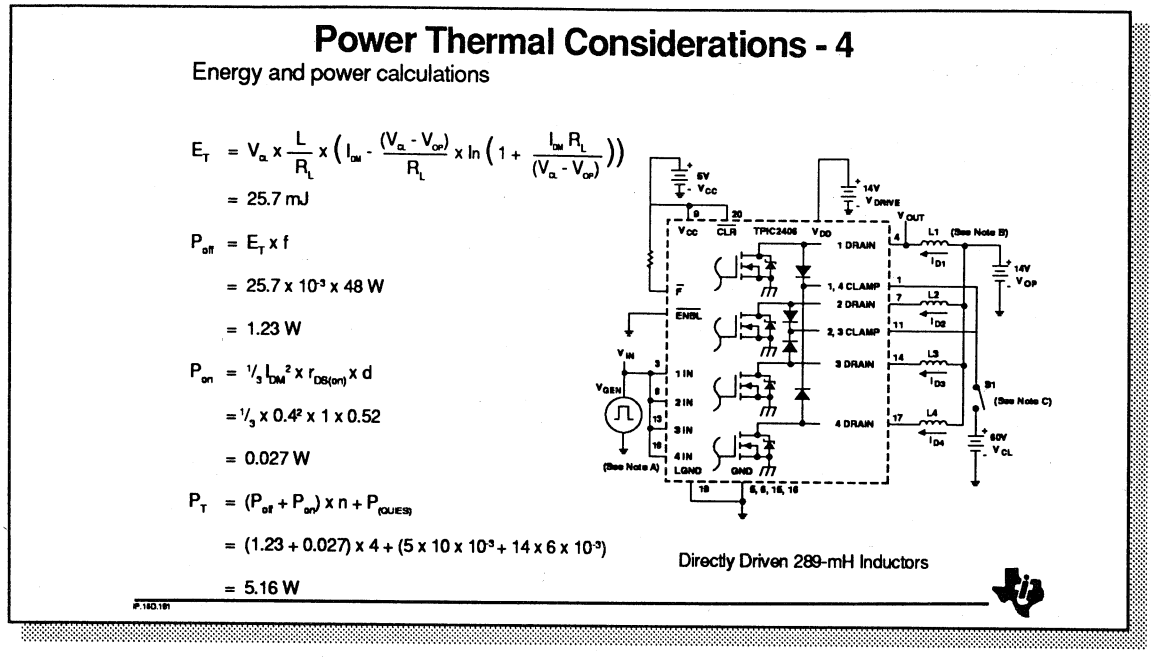


Figure 23 - Power Thermal Considerations - 4

Determining the Maximum Energy of an Inductive Load

The TPIC2406 avalanche energy rating of 50mJ per output switch greatly enhances its value as an inductive load driver. Therefore, for inductive loads equal to or less than 50mJ, an external voltage clamp may not be required depending on the device's power dissipation, heat sinking, and operating temperature. If an external clamp is required, included in the TPIC2406 are two pairs of integral transient suppression clamp diodes. One diode pair is connected to the open drains of output MOSFETs 1 and 4, and one diode pair is connected to the open drains of output MOSFETs 2 and 3 as seen in the circuit showing outputs driving 289mH inductors.

Notes

Example -3

Calculations using the values given for the 289mH inductors shows that the output drivers must handle 25.7mJ if no external clamp is used. This is well within the 50mJ capability of the device. However, further calculations for the device's total power dissipation, P_T, reveal that it is 5.25W. Therefore, external heat sinking will be required, or an external clamp must be used if external heat sinking is not available.

Test Circuit Notes

A. The pulse generator has the following characteristics:
t_r < 10ns, t_f < 10 ns, t_w = 11ms, PRR = 48Hz, V_{out} = 5V, Z_o = 50Ω. The input pulse duration, t_w, is increased until the peak load current, I_{DM} = 0.4A.

B. Inductors
L1 = L2 = L3 = L4 = 289mH/150Ω.

C. External Voltage Clamp
If the TPIC2406 is operated on a heat sink capable of maintaining a case temperature of less than 107°C, no external voltage clamp will be required and S_1 remains open. If the case temperature cannot be maintained at or below 107°C, an external voltage clamp is required and S_1 must be closed.

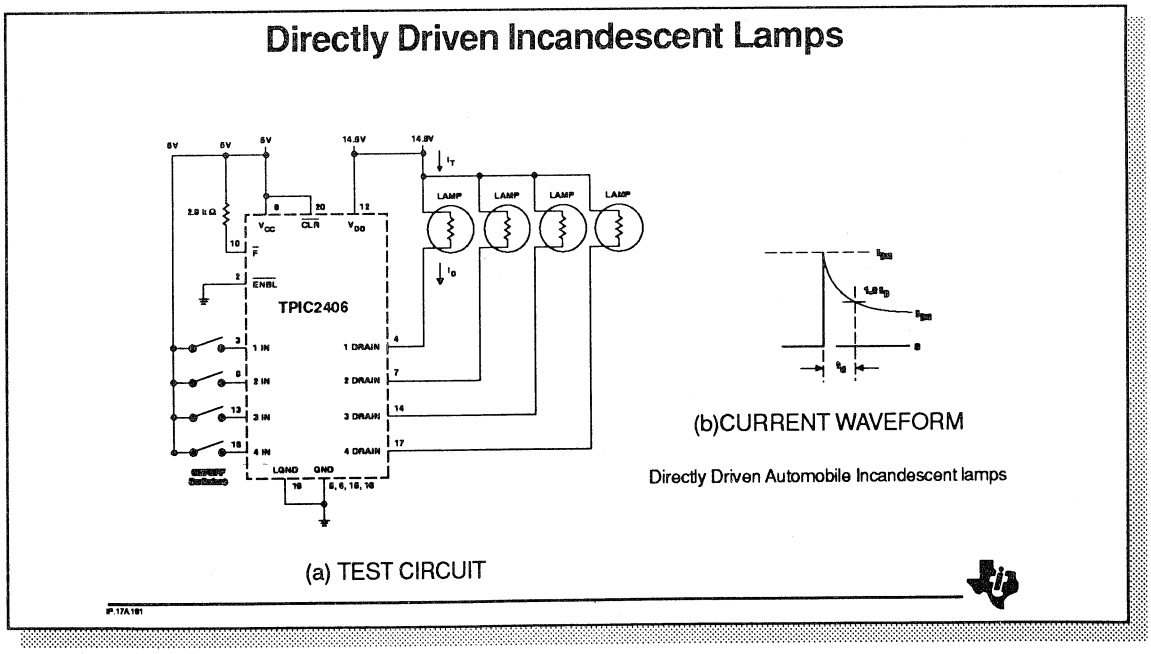


Figure 24 - Directly Driven Incandescent Lamps

The often over-looked problem of driving incandescent lamps is their low cold filament resistance that produce large surge currents anywhere from 8 to 10 times their steady state current ratings. In the past this has often resulted in poor longtime reliability of the IC drivers due to their inabilityto handle the high surge currents without device deterioration.

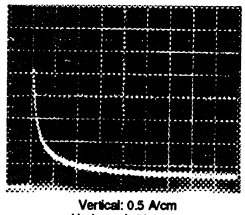
The TPIC2406's internal protection circuitry allows it to be used to drive many of the automotive types of incandescent lamps with high reliability.

This application circuit was used to test drive several types of popular incandescent lamps. Most of these lamp types are used in the automotive industry. Tests were run with the maximum of all four TPIC2406 outputs on, or with as many outputs as possible on without causing thermal shutdown.

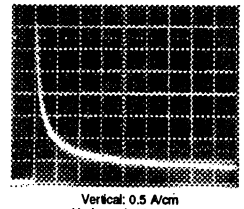
Evaluation of TPIC2406 Switching Incandescent Lamps

Lamp Type	Single Output Lamp Current (A)		td (ms)	TPIC2406 Case Temperature (°C) Number of Outputs Simultaneously Turned On			
	IDM	ID		1	2	3	4
194	2.6	0.284	50	25	26	27.5	30
168	3.5	0.345	50	26	28	31	34
631	5.5	0.677	50	35	47	58	70
1003	8.4	1.018	50	50	86	122	†
1004	8.8	0.992	50	49	82	124	†
211-2	8.8	1.032	50	50	82	129	†

† Thermal Shutdown



Vertical: 0.5 A/cm
Horizontal: 10 ms/cm
(C) LAMP TYPE 194
LAMP CURRENT TURN-ON WAVEFORM



Vertical: 0.5 A/cm
Horizontal: 10 ms/cm
(D) LAMP TYPE 168
LAMP CURRENT TURN-ON WAVEFORM

IP.178.191

Figure 25 - Evaluation of TPIC2406 Switching Incandescent Lamps

The table in the Figure lists the lamp types tested with their measured continuous current I_D and their peak, cold filament, surge current I_{DM}.

The TPIC2406 case temperature, T_C, is measured for each combination of outputs operating. Also listed in the table is peak current decay time, t_d. It is the time measured for the duration that it takes a peak current I_{DM} to decrease to a value of 1.2 I_D.

Notes

The TPIC's independent thermal shutdown circuits monitor each output and disable all outputs when the maximum junction temperature is reached, typically 155°C. At this point, a fault condition is sensed and reported by the error sensing circuit. This condition remains until the junction temperature falls below 140°C (typically), and the thermal shutdown circuit allows all outputs to return to normal operation.

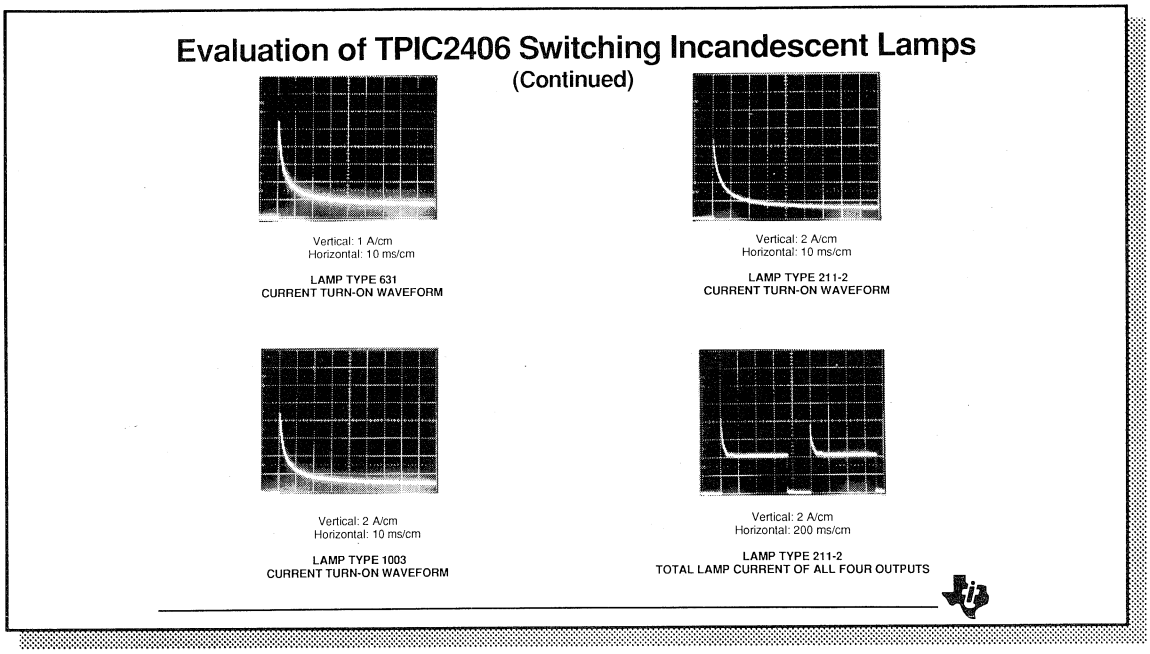


Figure 26 - Evaluation of TPIC2406 Switching Incandescent Lamps (Continued)

The highest current in the test group was a 211-2 type bulb as seen in the table. The last waveform in our test samples shows the results of thermal shutdown due to the high current requirements when driving type 211-2 lamps.

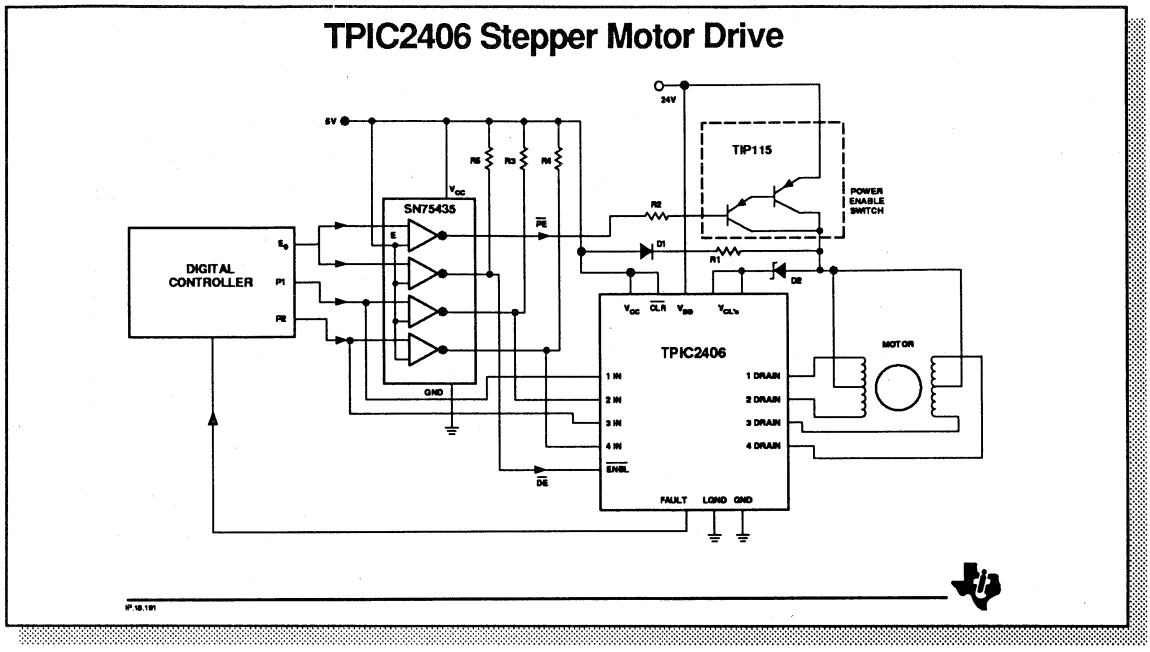


Figure 27 - TPIC2406 Stepper Motor Drive

Stepper motors, due to their digital drive requirements, are natural motion providers for microprocessor, computer or ASIC-based systems. The TPIC2406 provides a simple solution to the problem of translating logic level timing to the high-voltage and current requirements of stepping motors.

Driving Unipolar Stepper Motors

The permanent magnet rotor stepping motor has two forms of stator winding. The bipolar stepping motor has a single winding on each stator pole and uses a full bridge to drive each phase winding. Whereas, in the unipolar stepping motor, the flux reversal is accomplished by individually driving a bifilar winding on each pole. The windings are phased such that when current is passed through one winding, a given flux direction is generated. By passing current through the other winding, the opposite flux polarity is produced. Thus, the overall magnetic effect is the same as the bipolar motor, but the phase windings can be more economically driven by devices with open-drain outputs such as the TPIC2406.

Notes

Printer Paper Feeding Application

Printers are a major application of stepper motors because the stepping motor is ideally matched to the needs of paper feeding. In this application, the paper is required to be moved in well defined increments, which, through gearing, will equate to a fixed number of motor steps. Also, there is no need for positional feedback as the paper position is initialized by the user at paper loading. Therefore, the motion system is open loop; the paper being advanced by stepping the motor's rotor a given amount.

In our example, a TPIC2406 replaces a collection of discrete components used to drive the paper-feed motor in an existing printer. By virtue of their permanent magnet rotor, stepper motors have a degree of detent; that is, the motor will naturally align to one of its step positions. For small external torques, this detent is sufficient to hold the rotor in position, but in printer applications the motor's detent needs to be increased. This increase is to avoid paper movement when printing by feeding current through the appropriate windings. Only a low level current is required, about 30mA, which is most efficiently sourced from the 5V logic rail via diode D_1 and resistor R_1. Obviously to provide the return path, the outputs of the TPIC2406 have to be left in the same state that caused the last rotor step. In this particular design, the $\overline{CLR}$ (which turns all outputs off) and $\overline{ENBL}$ functions are not used and they are logically strapped high and low, respectively.

Two things must happen to cause the motor to step. The first is to supply 24V to the winding centre tap and then to toggle the four TPIC2406 outputs to step the motor in the appropriate direction. One pin of the digital controller switches on the output of an inverting open-drain buffer, IC_{1a}.

This in turn switches on the Darlington transistor TR_1, via resistor R_2, to apply the 24V supply to the motor. When this happens, the low current to supplement the motor's detent is terminated by diode D_1 that becomes reverse biased.

When the motor is stepping, the four outputs of the TPIC2406 produce "square wave" type waveforms. These waveforms consist of two square waves, one displaced by 90 degrees from the other, in both true and inverted forms.

Pin count is often at a premium on digital controllers and in this solution only two pins are used to provide the basic square waves that are applied to the TPIC2406 inputs 1 and 3. Two inverting buffers provide the drive for inputs 2 and 4.

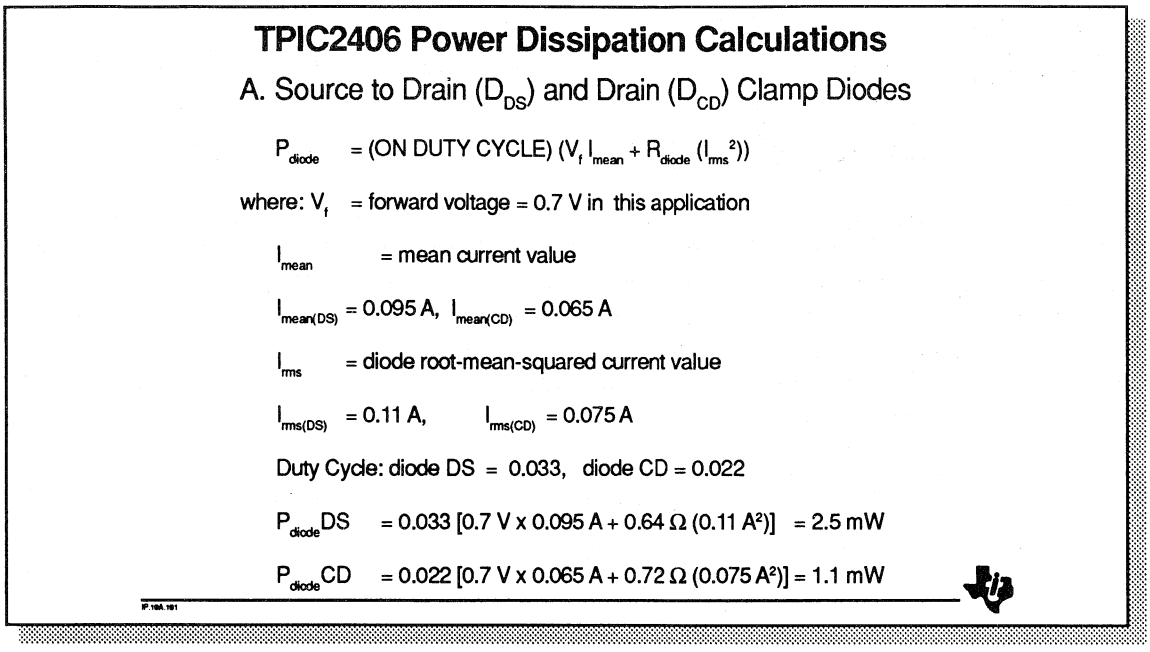


Figure 28 - TPIC2406 Power Dissipation Calculations

When the motor stalls or starts rotation, the peak winding current is limited by the winding resistance. In our sample application the peak current is about 400mA and well within the TPIC2406's output current capability.

Assessing the maximum possible power dissipation in the TPIC2406 output involves summing the source-drain diode loss (when the current is negative), the $r_{DS(on)}$ loss (when the current is positive), and the clamp-diode loss when the voltage overshoot is limited. The peak output drain voltageis limited by connecting the clamp diodes back to the motor centre tap via a 27V zener diode, D_2. As the average current in this diode is only 6mA, a 250mW component could be used.

By linearizing the diode V_I characteristic to a fixed starting voltage, V_T, and a slope resistance, R_d, the diode power loss can easily be derived. Considering the current flowing during the conduction period, it can be shown that the power loss at a fixed voltage, V_T, is the

Notes

voltage multiplied by the mean current, Imean, plus the mean square current, I_{rms}^2, multiplied by the resistance, R_d. Therefore the calculation for power loss of the diode is:

$$P_{diode} = (\text{conduction duty cycle}) * (V_T * I_{mean} + R_{diode} * I_{rms}^2) ;$$

At 1.25A, the source-drain and clamp diodes of the TPIC2406 have maximum forward-voltage values of 1.5V and 1.6V, respectively. Choosing a V_T value of 0.7V gives slope resistances for the source-drain and clamp diodes of 0.64Ω and 0.72Ω respectively 0.095A, and an rms current of 0.11A. The power loss for the drain-source diode is about 2.5mW. Similarly for the clamp diode, the mean current is 0.065A, the rms current is 0.075A, and a duty cycle of 0.022, which leads to a clamp-diode power loss of about 1.1mW. As can be seen, the diode losses in this application are extremely small.

TPIC2406 Power Dissipation Calculations

B. Power of MOSFET, $P_{MF} = R_{DS(ON)} \times I_{rms}^2$, $R_{DS(ON)} = 1\ \Omega$, $I_{rms} = 0.23$ A

$P_{MF} = 0.053$ W $= 53$ mW

Total for 4 drivers $= P_{DT} = 4 (P_{MF} + P_{DS} + P_{DC}) = 4 (0.053 + 0.0025 + 0.0011)$

$P_{DT} = 227$ mW

Total Power, $P_T = P_{DT} + P_{LV} + P_{HV}$ where: $P_{LV} = P_{VCC \times ICC}$, $P_{HV} = P_{VDD \times IDD}$

$I_{CC} = 100$ mA, $I_{DD} = 6$ mA

Power is reduced by 30% due to high temperature, therefore

$P_T = 227$ mW + (5 V) (10 mA) (0.7) + (24 V) (6 mA) (0.7)

$P_T = 227$ mW + 35 mW + 101 mW

$P_T = 363$ mW

C. MAXIMUM AMBIENT TEMPERATURE (T_{Amax}) FOR $P_T = 363$ mW.

$T_{Amax} = T_{Jmax} - (R\emptyset_{JC} \times P_T) = 125°\text{ C} - (50°\text{ C/W} \times 0.363\text{ W})$

$T_{Amax} = 107°$ C (approx)

Figure 29 - TPIC2406 Power Dissipation Calculations (Continued)

The last output loss to be considered is that due to $r_{DS(on)}$. At 125°C and 1.25A, the maximum value of $r_{DS(on)}$ is 1Ω. Graphically, integrating the square of the drain current values gives a mean square current of 0.053 A^2 (equal to 0.23A rms), which leads to a power loss of about 53mW. The total loss will be about 230mW.

Finally, the power loss of the logic and driver circuits need to be added to arrive at the total worst-case power loss of the TPIC2406. The data sheet maximums of 10mA and 6mA, respectively, are measured at 25°C. These values will fall by about 30% at high temperatures, hence the worst-case high temperature power loss, P_T, becomes about 363mW.

As the junction to ambient thermal resistance is 50°C/W, the maximum permissible ambient temperature, T_A, for the above dissipation is about 107°C. This example illustrates the extremely low operating losses of the TPIC2406.

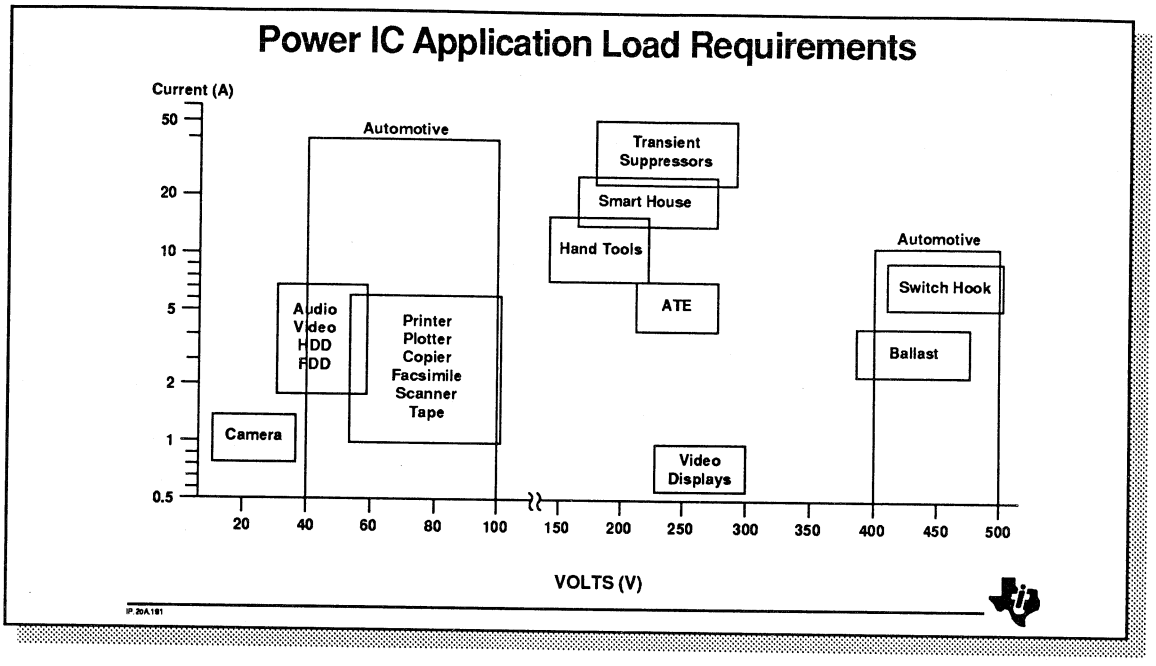


Figure 30 - Power IC Application Load Requirements

Power IC application load requirements range from 40V to 500V and from 1A to 50A. Automotive technology requirements are among the most demanding in the electronics industry with respect to fault tolerance and operating environment. Synergy exists between the automotive industry's needs and the needs of many other consumer, industrial and military applications.

Built-in fault detection, system protection, and logic control are key features of any "Intelligent Power Integrated Circuit".

Notes

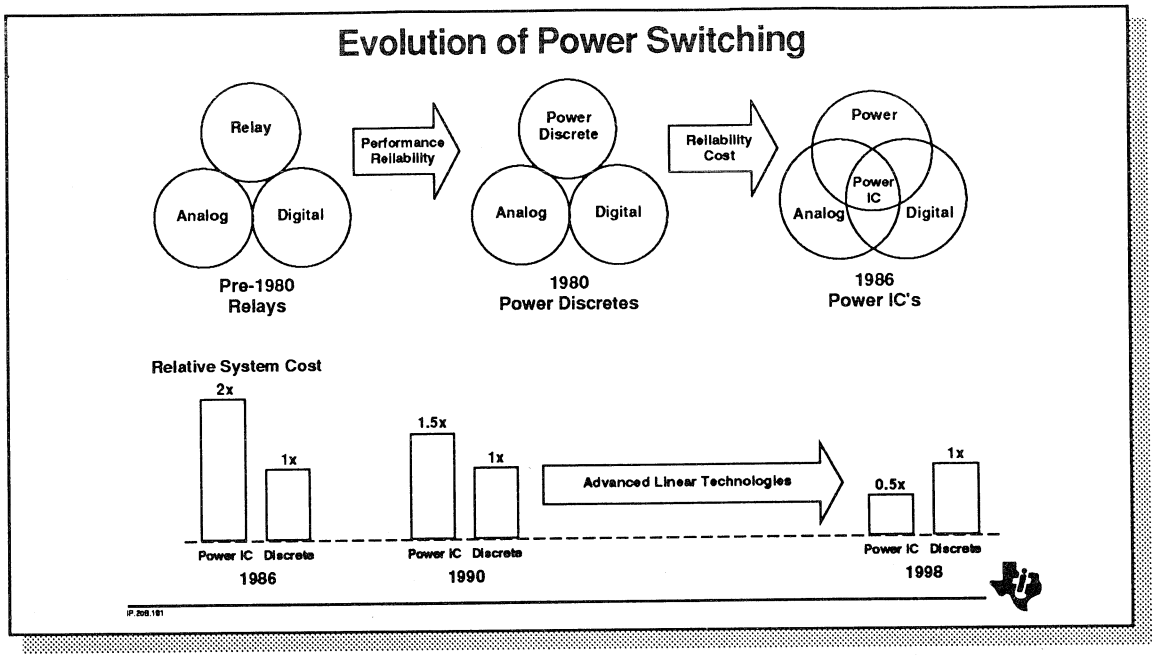


Figure 31 - Evolution of Power Switching

- Power discrete transistors replaced mechanical relays to improve system performance and reliability in the early 1980s.
- Power ICs further the reliability improvement and offer the opportunity for significant system cost reductions. (classic up-integration argument).
- Power ICs merge Analog, Digital, and Power functions into one monolithic IC.
- Advanced Linear Technologies are required to make power IC based systems more cost effective than discretes.

The cost comparisons between Power ICs and Discretes refers to their system costs. The cost effectiveness of Power IC based systems is driven by increasing system complexity and reduced unit costs for the Power IC itself.

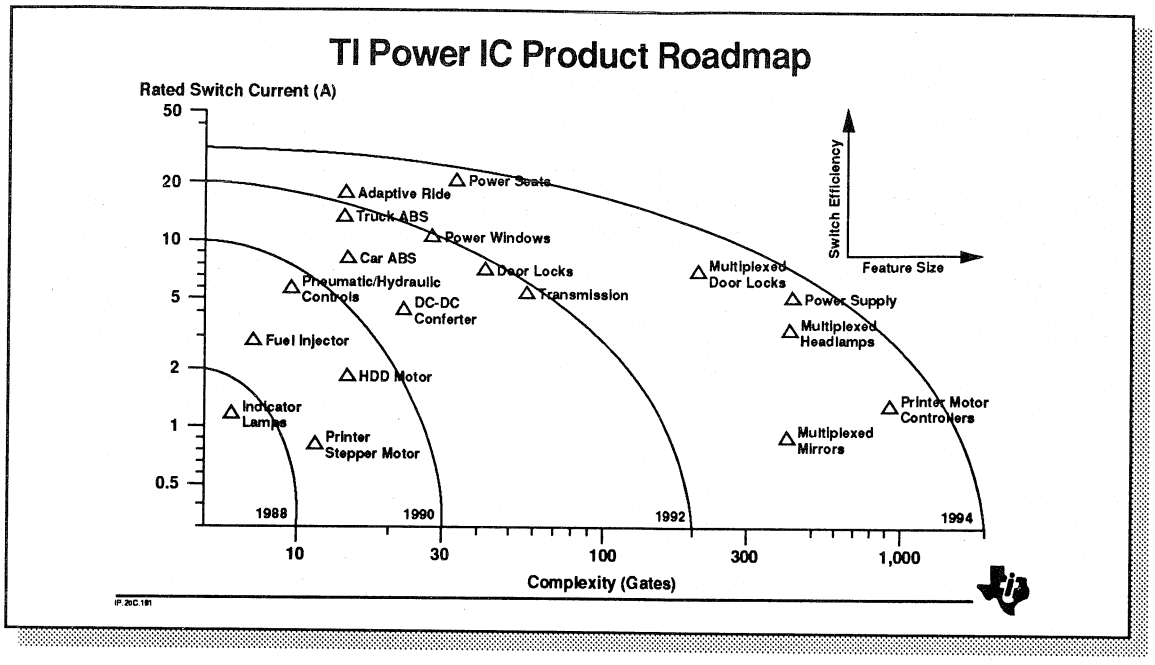


Figure 32 - T.I. Power IC Product Roadmap

As technology advances Power ICs support applications requiring higher current, higher voltage and higher logic complexity.

- Improvements in switch efficiency is enabling higher current applications to use Power ICs.
- Reduction in feature size is allowing higher complexity applications to use Power ICs.
- The higher power and complexity of volume automotive applications is driving future power IC systems.

The growth of the Power IC market depends on the continued technology advancements enabling their use in more and more applications.

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